



M29F512B

512 Kbit (64Kb x8, Bulk) Single Supply Flash Memory

PRELIMINARY DATA

- SINGLE $5V \pm 10\%$ SUPPLY VOLTAGE for PROGRAM, ERASE and READ OPERATIONS
- ACCESS TIME: 45ns
- PROGRAMMING TIME
 - 8 μ s per Byte typical
- PROGRAM/ERASE CONTROLLER
 - Embedded Byte Program algorithm
 - Embedded Chip Erase algorithm
 - Status Register Polling and Toggle Bits
- UNLOCK BYPASS PROGRAM COMMAND
 - Faster Production/Batch Programming
- LOW POWER CONSUMPTION
 - Standby and Automatic Standby
- 100,000 PROGRAM/ERASE CYCLES
- 20 YEARS DATA RETENTION
 - Defectivity below 1 ppm/year
- ELECTRONIC SIGNATURE
 - Manufacturer Code: 20h
 - Device Code: 24h

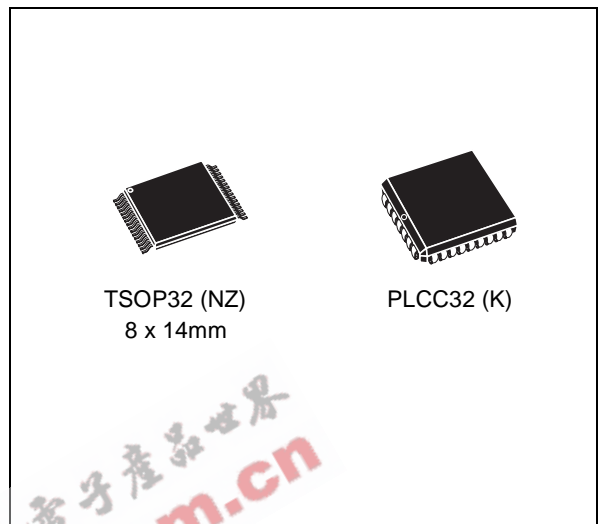


Figure 1. Logic Diagram

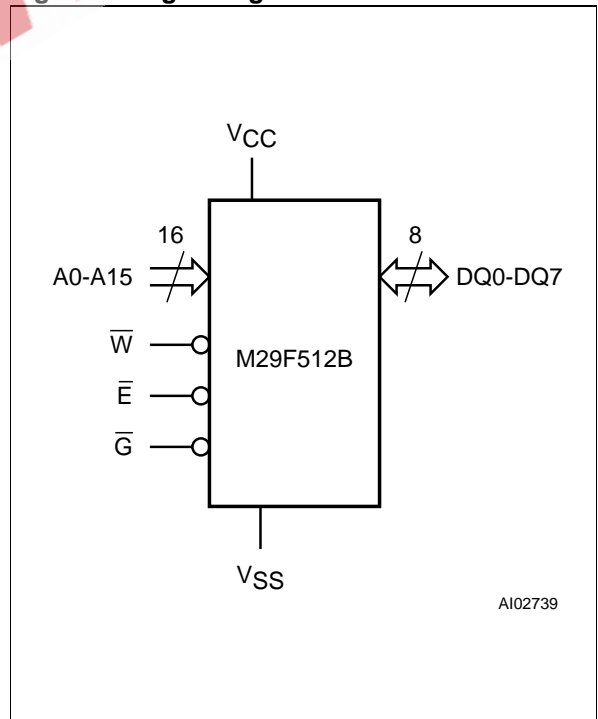


Figure 2A. TSOPConnections

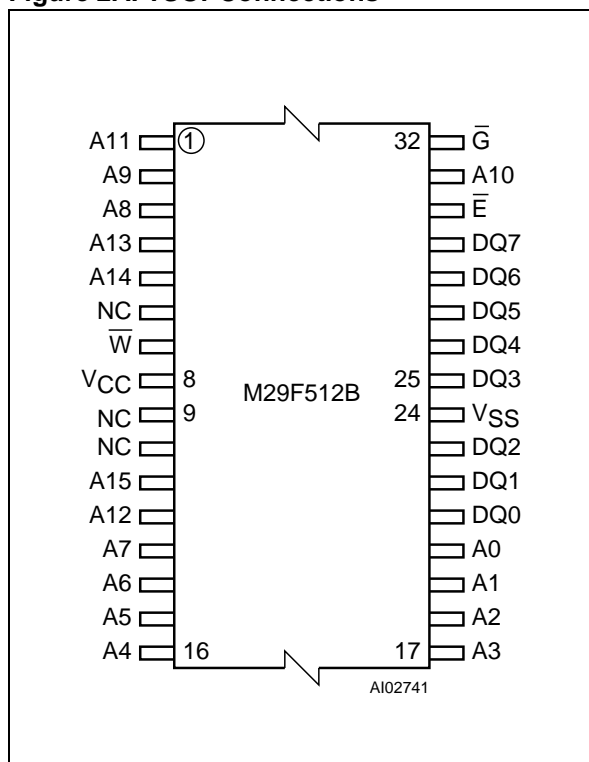


Figure 2B. PLCC Connections

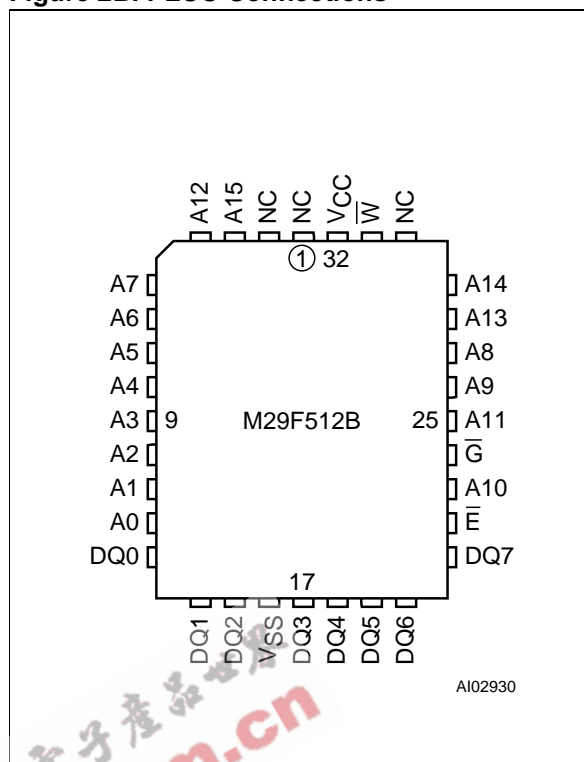


Table 1. Signal Names

| | |
|-----------|--------------------------|
| A0-A15 | Address Inputs |
| DQ0-DQ7 | Data Inputs/Outputs |
| \bar{E} | Chip Enable |
| \bar{G} | Output Enable |
| \bar{W} | Write Enable |
| Vcc | Supply Voltage |
| Vss | Ground |
| NC | Not Connected Internally |

SUMMARY DESCRIPTION

The M29F512B is a 512 Kbit (64Kb x8) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single 5V supply. On power-up the memory defaults to its Read mode where it can be read in the same way as a ROM or EPROM.

Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are re-

quired to update the memory contents. The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

The memory is offered in TSOP32 (8 x 14mm) and PLCC32 packages. Access times of 45ns and 70ns are available. The memory is supplied with all the bits erased (set to '1').

SIGNAL DESCRIPTIONS

See Figure 1, Logic Diagram, and Table 1, Signal Names, for a brief overview of the signals connected to this device.

Address Inputs (A0-A15). The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine.

Data Inputs/Outputs (DQ0-DQ7). The Data Inputs/Outputs output the data stored at the selected address during a Bus Read operation. During Bus Write operations they represent the commands sent to the Command Interface of the internal state machine.



Table 2. Absolute Maximum Ratings ⁽¹⁾

| Symbol | Parameter | Value | Unit |
|--------------------------------|-------------------------------|--------------|------|
| T _A | Ambient Operating Temperature | 0 to 70 | °C |
| T _{BIAS} | Temperature Under Bias | -50 to 125 | °C |
| T _{STG} | Storage Temperature | -65 to 150 | °C |
| V _{IO} ⁽²⁾ | Input or Output Voltage | -0.6 to 6 | V |
| V _{CC} | Supply Voltage | -0.6 to 6 | V |
| V _{ID} | Identification Voltage | -0.6 to 13.5 | V |

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

2. Minimum Voltage may undershoot to -2V during transition and for less than 20ns during transitions.

Chip Enable (\bar{E}). The Chip Enable, \bar{E} , activates the memory, allowing Bus Read and Bus Write operations to be performed. When Chip Enable is High, V_{IH}, all other pins are ignored.

Output Enable (\bar{G}). The Output Enable, \bar{G} , controls the Bus Read operation of the memory.

Write Enable (\bar{W}). The Write Enable, \bar{W} , controls the Bus Write operation of the memory's Command Interface.

V_{CC} Supply Voltage. The V_{CC} Supply Voltage supplies the power for all operations (Read, Program, Erase etc.).

The Command Interface is disabled when the V_{CC} Supply Voltage is less than the Lockout Voltage, V_{LKO}. This prevents Bus Write operations from accidentally damaging the data during power up, power down and power surges. If the Program/Erase Controller is programming or erasing during this time then the operation aborts and the memory contents being altered will be invalid.

A 0.1μF capacitor should be connected between the V_{CC} Supply Voltage pin and the V_{SS} Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations, I_{CC3}.

V_{SS} Ground. The V_{SS} Ground is the reference for all voltage measurements.

BUS OPERATIONS

There are five standard bus operations that control the device. These are Bus Read, Bus Write, Output Disable, Standby and Automatic Standby. See Table 3, Bus Operations, for a summary. Typically glitches of less than 5ns are ignored by the memory and do not affect bus operations.

Bus Read. Bus Read operations read from the memory cells, or specific registers in the Command Interface. A valid Bus Read operation involves setting the desired address on the Address Inputs, applying a Low signal, V_{IL}, to Chip Enable and Output Enable and keeping Write Enable High, V_{IH}. The Data Inputs/Outputs will output the value, see Figure 7, Read Mode AC Waveforms, and Table 10, Read AC Characteristics, for details of when the output becomes valid.

Bus Write. Bus Write operations write to the Command Interface. A valid Bus Write operation begins by setting the desired address on the Address Inputs. The Address Inputs are latched by the Command Interface on the falling edge of Chip Enable or Write Enable, whichever occurs last. The Data Inputs/Outputs are latched by the Command Interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Output Enable must remain High, V_{IH}, during the whole Bus Write operation. See Figures 8 and 9, Write AC Waveforms, and Tables 11 and 12, Write AC Characteristics, for details of the timing requirements.

Table 3. Bus Operations

| Operation | \bar{E} | \bar{G} | \bar{W} | Address Inputs | Data Inputs/Outputs |
|------------------------|-----------|-----------|-----------|--|---------------------|
| Bus Read | V_{IL} | V_{IL} | V_{IH} | Cell Address | Data Output |
| Bus Write | V_{IL} | V_{IH} | V_{IL} | Command Address | Data Input |
| Output Disable | X | V_{IH} | V_{IH} | X | Hi-Z |
| Standby | V_{IH} | X | X | X | Hi-Z |
| Read Manufacturer Code | V_{IL} | V_{IL} | V_{IH} | A0 = V_{IL} , A1 = V_{IL} , A9 = V_{ID} , Others V_{IL} or V_{IH} | 20h |
| Read Device Code | V_{IL} | V_{IL} | V_{IH} | A0 = V_{IH} , A1 = V_{IL} , A9 = V_{ID} , Others V_{IL} or V_{IH} | 24h |

Note: X = V_{IL} or V_{IH} .

Output Disable. The Data Inputs/Outputs are in the high impedance state when Output Enable is High, V_{IH} .

Standby. When Chip Enable is High, V_{IH} , the memory enters Standby mode and the Data Inputs/Outputs pins are placed in the high-impedance state. To reduce the Supply Current to the Standby Supply Current, I_{CC2} , Chip Enable should be held within $V_{CC} \pm 0.2V$. For the Standby current level see Table 9, DC Characteristics.

During program or erase operations the memory will continue to use the Program/Erase Supply Current, I_{CC3} , for Program or Erase operations until the operation completes.

Automatic Standby. If CMOS levels ($V_{CC} \pm 0.2V$) are used to drive the bus and the bus is inactive for 150ns or more the memory enters Automatic Standby where the internal Supply Current is reduced to the Standby Supply Current, I_{CC2} . The Data Inputs/Outputs will still output data if a Bus Read operation is in progress.

Special Bus Operations

Additional bus operations can be performed to read the Electronic Signature. These bus operations are intended for use by programming equipment and are not usually used in applications. They require V_{ID} to be applied to some pins.

Electronic Signature. The memory has two codes, the manufacturer code and the device code, that can be read to identify the memory. These codes can be read by applying the signals listed in Table 3, Bus Operations.

COMMAND INTERFACE

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. Failure to observe a valid sequence of Bus Write operations will result in the memory returning to Read mode. The long command sequences are imposed to maximize data security.

The commands are summarized in Table 4, Commands. Refer to Table 4 in conjunction with the text descriptions below.

Read/Reset Command. The Read/Reset command returns the memory to its Read mode where it behaves like a ROM or EPROM. It also resets the errors in the Status Register. Either one or three Bus Write operations can be used to issue the Read/Reset command.

If the Read/Reset command is issued during a Chip Erase operation the memory will take about 10 μ s to abort the Chip Erase. During the abort period no valid data can be read from the memory. Issuing a Read/Reset command during a Chip Erase operation will leave invalid data in the memory.

Auto Select Command. The Auto Select command is used to read the Manufacturer Code and the Device Code. Three consecutive Bus Write operations are required to issue the Auto Select command. Once the Auto Select command is issued the memory remains in Auto Select mode until another command is issued.

Table 4. Commands

| Command | Length | Bus Write Operations | | | | | | | | | | | |
|-----------------------|--------|----------------------|------|------|------|------|------|------|------|------|------|------|------|
| | | 1st | | 2nd | | 3rd | | 4th | | 5th | | 6th | |
| | | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data |
| Read/Reset | 1 | X | F0 | | | | | | | | | | |
| | 3 | 555 | AA | 2AA | 55 | X | F0 | | | | | | |
| Auto Select | 3 | 555 | AA | 2AA | 55 | 555 | 90 | | | | | | |
| Program | 4 | 555 | AA | 2AA | 55 | 555 | A0 | PA | PD | | | | |
| Unlock Bypass | 3 | 555 | AA | 2AA | 55 | 555 | 20 | | | | | | |
| Unlock Bypass Program | 2 | X | A0 | PA | PD | | | | | | | | |
| Unlock Bypass Reset | 2 | X | 90 | X | 00 | | | | | | | | |
| Chip Erase | 6 | 555 | AA | 2AA | 55 | 555 | 80 | 555 | AA | 2AA | 55 | 555 | 10 |

Note: X Don't Care, PA Program Address, PD Program Data.

All values in the table are in hexadecimal.

The Command Interface only uses address bits A0-A10 to verify the commands, the upper address bits are Don't Care.

Read/Reset. After a Read/Reset command, read the memory as normal until another command is issued.

Auto Select. After an Auto Select command, read Manufacturer ID or Device ID.

Program, Unlock Bypass Program, Chip Erase. After these commands read the Status Register until the Program/Erase Controller completes and the memory returns to Read Mode.

Unlock Bypass. After the Unlock Bypass command issue Unlock Bypass Program or Unlock Bypass Reset commands.

Unlock Bypass Reset. After the Unlock Bypass Reset command read the memory as normal until another command is issued.

From the Auto Select mode the Manufacturer Code can be read using a Bus Read operation with $A0 = V_{IL}$ and $A1 = V_{IL}$. The other address bits may be set to either V_{IL} or V_{IH} . The Manufacturer Code for STMicroelectronics is 20h.

The Device Code can be read using a Bus Read operation with $A0 = V_{IH}$ and $A1 = V_{IL}$. The other address bits may be set to either V_{IL} or V_{IH} . The Device Code for the M29F512B is 24h.

Program Command. The Program command can be used to program a value to one address in the memory array at a time. The command requires four Bus Write operations, the final write operation latches the address and data in the internal state machine and starts the Program/Erase Controller.

During the program operation the memory will ignore all commands. It is not possible to issue any command to abort or pause the operation. Typical program times are given in Table 5. Bus Read operations during the program operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the program operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

Note that the Program command cannot change a bit set at '0' back to '1' and attempting to do so will cause an error. The Chip Erase command must be used to set all the bits in the memory from '0' to '1'.

Unlock Bypass Command. The Unlock Bypass command is used in conjunction with the Unlock Bypass Program command to program the memory. When the access time to the device is long (as with some EPROM programmers) considerable time saving can be made by using these commands. Three Bus Write operations are required to issue the Unlock Bypass command.

Once the Unlock Bypass command has been issued the memory will only accept the Unlock Bypass Program command and the Unlock Bypass Reset command. The memory can be read as if in Read mode.

Table 5. Program, Erase Times and Program, Erase Endurance Cycles
($T_A = 0$ to 70°C)

| Parameter | Min | Typ ⁽¹⁾ | Typical after 100k W/E Cycles ⁽¹⁾ | Max | Unit |
|--|---------|--------------------|---|-----|---------------|
| Chip Erase (All bits in the memory set to '0') | | 0.4 | 0.4 | | sec |
| Chip Erase | | 0.8 | 0.8 | 4 | sec |
| Program | | 8 | 8 | 150 | μs |
| Chip Program | | 0.6 | 0.6 | 2.5 | sec |
| Program/Erase Cycles | 100,000 | | | | cycles |

Note: 1. $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$.

Unlock Bypass Program Command. The Unlock Bypass Program command can be used to program one address in memory at a time. The command requires two Bus Write operations, the final write operation latches the address and data in the internal state machine and starts the Program/Erase Controller.

The Program operation using the Unlock Bypass Program command behaves identically to the Program operation using the Program command. The operation cannot be aborted and the Status Register is read. Errors must be reset using the Read/Reset command, which leaves the device in Unlock Bypass Mode. See the Program command for details on the behavior.

Unlock Bypass Reset Command. The Unlock Bypass Reset command can be used to return to Read/Reset mode from Unlock Bypass Mode. Two Bus Write operations are required to issue the Unlock Bypass Reset command.

Chip Erase Command. The Chip Erase command can be used to erase the memory. Six Bus Write operations are required to issue the Chip Erase Command and start the Program/Erase Controller.

All Bus Read operations during the Chip Erase operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details. Typical chip erase times are given in Table 5.

After the Chip Erase operation has completed the memory will return to the Read Mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read Mode.

The Chip Erase command sets all of the bits in the memory to '1'. All previous data is lost.

STATUS REGISTER

Bus Read operations from any address always read the Status Register during Program and Erase operations.

The bits in the Status Register are summarized in Table 6, Status Register Bits.

Data Polling Bit (DQ7). The Data Polling Bit can be used to identify whether the Program/Erase Controller has successfully completed its operation. The Data Polling Bit is output on DQ7 when the Status Register is read.

During Program operations the Data Polling Bit outputs the complement of the bit being programmed to DQ7. After successful completion of the Program operation the memory returns to Read mode and Bus Read operations from the address just programmed output DQ7, not its complement.

During Erase operations the Data Polling Bit outputs '0', the complement of the erased state of DQ7. After successful completion of the Erase operation the memory returns to Read Mode.

Figure 3, Data Polling Flowchart, gives an example of how to use the Data Polling Bit. A Valid Address is the address being programmed or any address while erasing the chip.

Toggle Bit (DQ6). The Toggle Bit can be used to identify whether the Program/Erase Controller has successfully completed its operation. The Toggle Bit is output on DQ6 when the Status Register is read.

During Program and Erase operations the Toggle Bit changes from '0' to '1' to '0', etc., with successive Bus Read operations at any address. After successful completion of the operation the memory returns to Read mode.

Figure 4, Data Toggle Flowchart, gives an example of how to use the Data Toggle Bit.

Table 6. Status Register Bits

| Operation | Address | DQ7 | DQ6 | DQ5 |
|---------------|-------------|------------------|--------|-----|
| Program | Any Address | $\overline{DQ7}$ | Toggle | 0 |
| Program Error | Any Address | $\overline{DQ7}$ | Toggle | 1 |
| Chip Erase | Any Address | 0 | Toggle | 0 |
| Erase Error | Any Address | 0 | Toggle | 1 |

Note: Unspecified data bits should be ignored.

Figure 3. Data Polling Flowchart

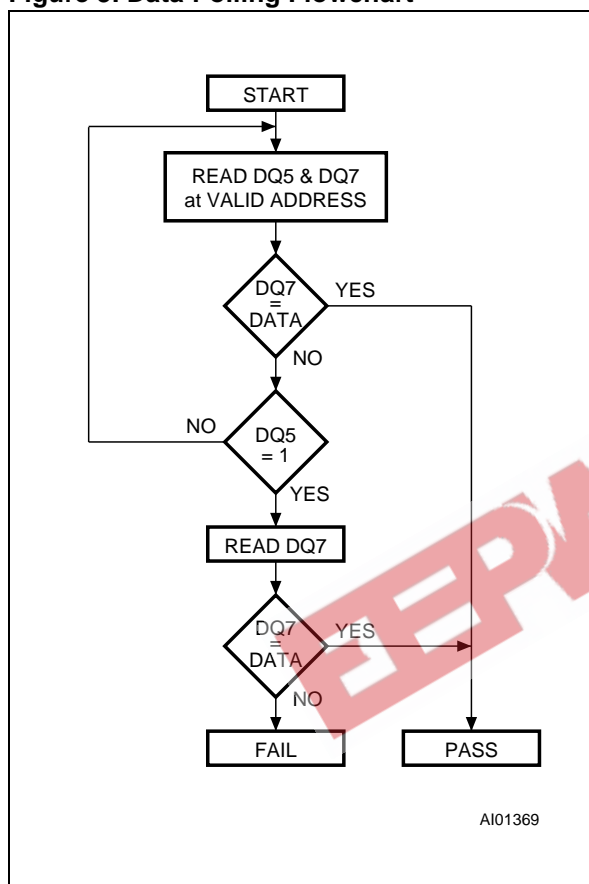
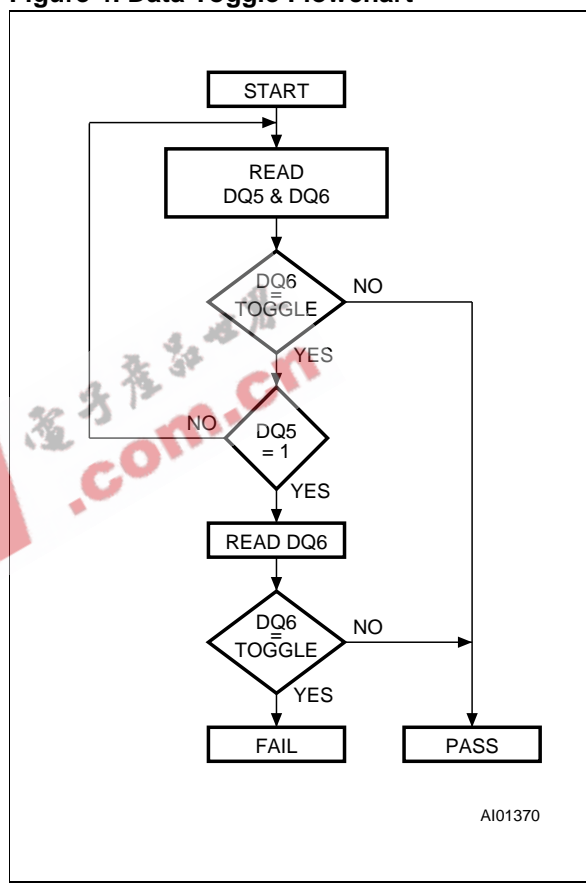


Figure 4. Data Toggle Flowchart



Error Bit (DQ5). The Error Bit can be used to identify errors detected by the Program/Erase Controller. The Error Bit is set to '1' when a Program or Chip Erase operation fails to write the correct data to the memory. If the Error Bit is set a Read/Reset command must be issued before oth-

er commands are issued. The Error bit is output on DQ5 when the Status Register is read.

Note that the Program command cannot change a bit set at '0' back to '1' and attempting to do so will cause an error. The Chip Erase command must be used to set all the bits the memory from '0' to '1'.

Table 7. AC Measurement Conditions

| | |
|---------------------------------------|--------------------|
| Load Capacitance (C_L) | 30pF |
| Input Rise and Fall Times | $\leq 10\text{ns}$ |
| Input Pulse Voltages | 0 to 3V |
| Input and Output Timing Ref. Voltages | 1.5V |

Figure 5. AC Testing Input Output Waveform

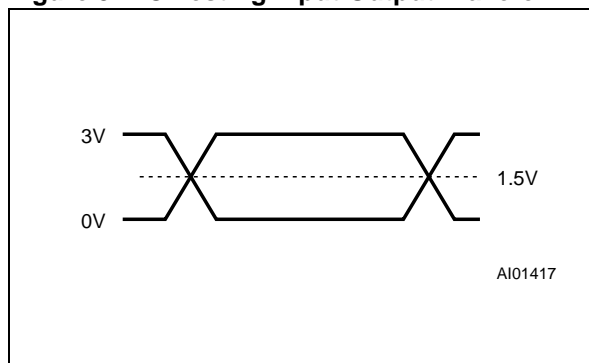


Figure 6. AC Testing Load Circuit

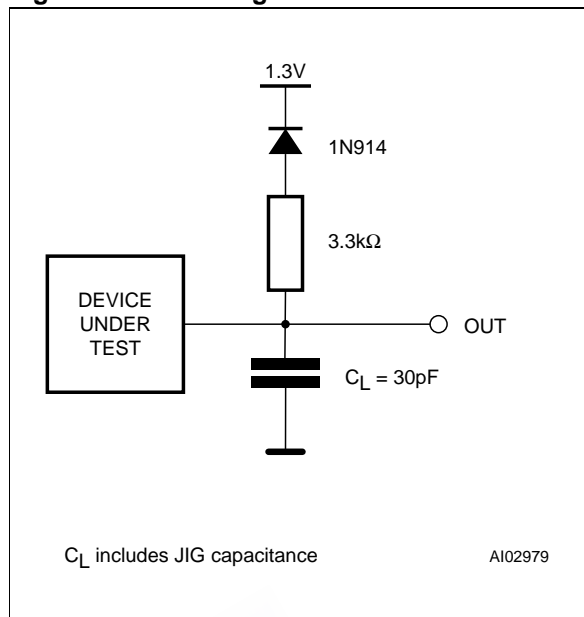


Table 8. Capacitance
($T_A = 25\text{ }^\circ\text{C}$, $f = 1\text{ MHz}$)

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|-----------|--------------------|----------------|-----|-----|------|
| C_{IN} | Input Capacitance | $V_{IN} = 0V$ | | 6 | pF |
| C_{OUT} | Output Capacitance | $V_{OUT} = 0V$ | | 12 | pF |

Note: Sampled only, not 100% tested.

Table 9. DC Characteristics(T_A = 0 to 70°C)

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|---------------------------------|--------------------------------------|---|-----------------------|-----------------------|------|
| I _{LI} | Input Leakage Current | 0V ≤ V _{IN} ≤ V _{CC} | | ±1 | μA |
| I _{LO} | Output Leakage Current | 0V ≤ V _{OUT} ≤ V _{CC} | | ±1 | μA |
| I _{CC1} | Supply Current (Read) | $\bar{E} = V_{IL}, \bar{G} = V_{IH}, f = 6\text{MHz}$ | | 15 | mA |
| I _{CC2} | Supply Current (Standby) | $\bar{E} = V_{CC} \pm 0.2\text{V}$ | | 100 | μA |
| I _{CC3} ⁽¹⁾ | Supply Current (Program/Erase) | Program/Erase Controller active | | 20 | mA |
| V _{IL} | Input Low Voltage | | -0.5 | 0.8 | V |
| V _{IH} | Input High Voltage | | 2 | V _{CC} + 0.5 | V |
| V _{OL} | Output Low Voltage | I _{OL} = 5.8mA | | 0.45 | V |
| V _{OH} | Output High Voltage | I _{OH} = -100μA | V _{CC} - 0.4 | | V |
| V _{ID} | Identification Voltage | | 11.5 | 12.5 | V |
| I _{ID} | Identification Current | A9 = V _{ID} | | 100 | μA |
| V _{LKO} ⁽¹⁾ | Program/Erase Lockout Supply Voltage | | 3.2 | 4.2 | V |

Note: 1. Sampled only, not 100% tested.

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Table 10. Read AC Characteristics

(TA = 0 to 70°C)

| Symbol | Alt | Parameter | Test Condition | | M29F512B | | Unit |
|---|------------------|---|--|-----|----------|----|------|
| | | | | | 45 | 70 | |
| t _{AVAV} | t _{RC} | Address Valid to Next Address Valid | $\bar{E} = V_{IL}$, $\bar{G} = V_{IL}$ | Min | 45 | 70 | ns |
| t _{AVQV} | t _{ACC} | Address Valid to Output Valid | $\bar{E} = V_{IL}$, $\bar{G} = V_{IL}$ | Max | 45 | 70 | ns |
| t _{ELQX} ⁽¹⁾ | t _{LZ} | Chip Enable Low to Output Transition | $\bar{G} = V_{IL}$ | Min | 0 | 0 | ns |
| t _{ELQV} | t _{CE} | Chip Enable Low to Output Valid | $\bar{G} = V_{IL}$ | Max | 45 | 70 | ns |
| t _{GLQX} ⁽¹⁾ | t _{OLZ} | Output Enable Low to Output Transition | $\bar{E} = V_{IL}$ | Min | 0 | 0 | ns |
| t _{GLQV} | t _{OE} | Output Enable Low to Output Valid | $\bar{E} = V_{IL}$ | Max | 25 | 30 | ns |
| t _{EHQZ} ⁽¹⁾ | t _{HZ} | Chip Enable High to Output Hi-Z | $\bar{G} = V_{IL}$ | Max | 15 | 20 | ns |
| t _{GHQZ} ⁽¹⁾ | t _{DF} | Output Enable High to Output Hi-Z | $\bar{E} = V_{IL}$ | Max | 15 | 20 | ns |
| t _{EHQX} t _{GHQX} t _{AXQX} | t _{OH} | Chip Enable, Output Enable or Address Transition to Output Transition | | Min | 0 | 0 | ns |

Note: 1. Sampled only, not 100% tested.

Figure 7. Read Mode AC Waveforms

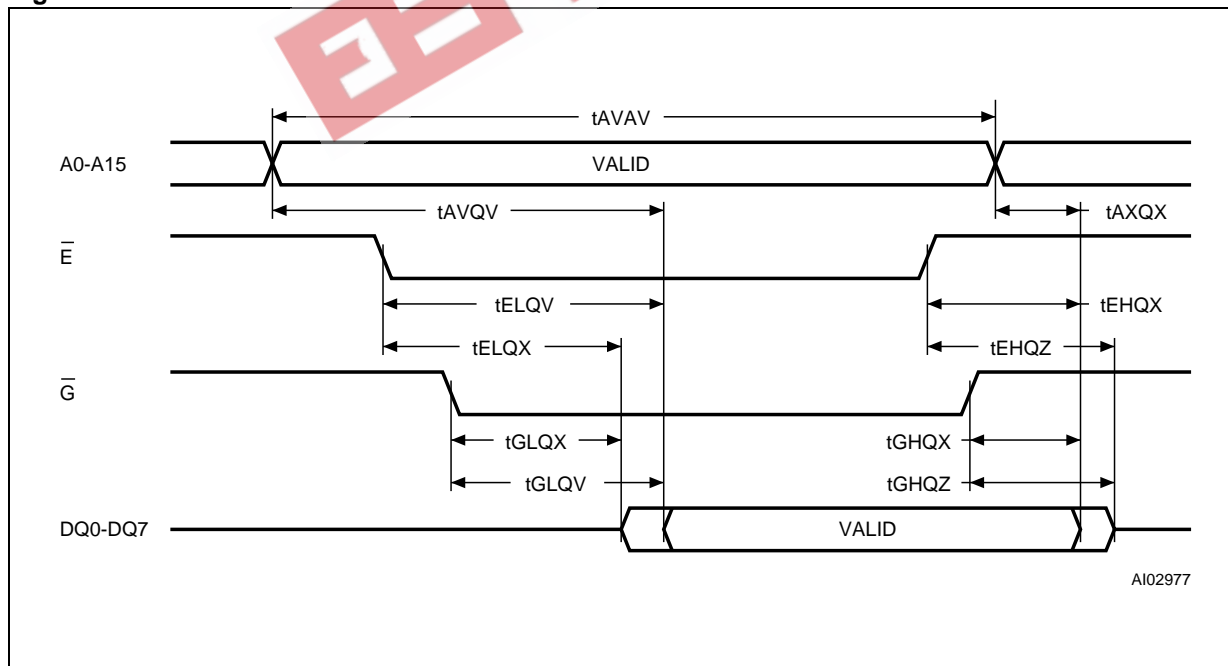
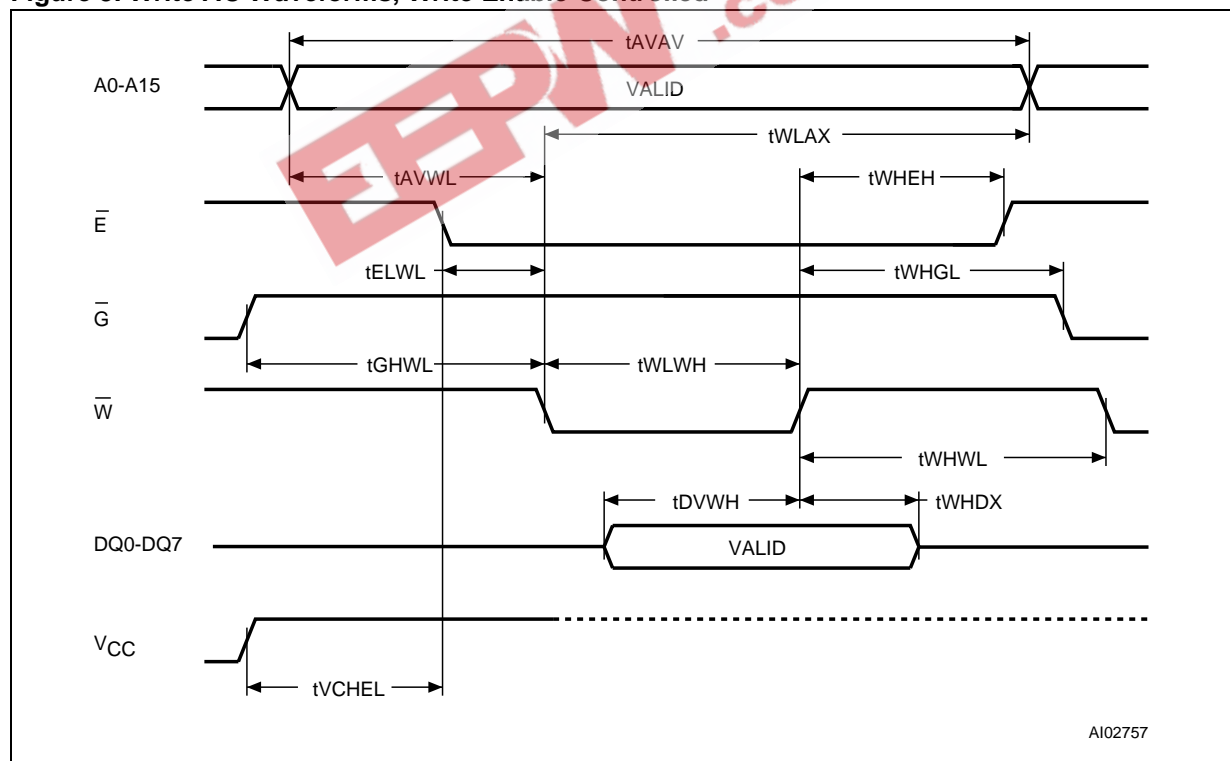


Table 11. Write AC Characteristics, Write Enable Controlled
($T_A = 0$ to 70 °C)

| Symbol | Alt | Parameter | | M29F512B | | Unit |
|-------------|------------|--|-----|----------|----|---------|
| | | | | 45 | 70 | |
| t_{AVAV} | t_{WC} | Address Valid to Next Address Valid | Min | 45 | 70 | ns |
| t_{ELWL} | t_{CS} | Chip Enable Low to Write Enable Low | Min | 0 | 0 | ns |
| t_{WLWH} | t_{WP} | Write Enable Low to Write Enable High | Min | 40 | 45 | ns |
| t_{DVWH} | t_{DS} | Input Valid to Write Enable High | Min | 25 | 30 | ns |
| t_{WHDX} | t_{DH} | Write Enable High to Input Transition | Min | 0 | 0 | ns |
| t_{WHEH} | t_{CH} | Write Enable High to Chip Enable High | Min | 0 | 0 | ns |
| t_{WHWL} | t_{WPH} | Write Enable High to Write Enable Low | Min | 20 | 20 | ns |
| t_{AVWL} | t_{AS} | Address Valid to Write Enable Low | Min | 0 | 0 | ns |
| t_{WLAX} | t_{AH} | Write Enable Low to Address Transition | Min | 40 | 45 | ns |
| t_{GHWL} | | Output Enable High to Write Enable Low | Min | 0 | 0 | ns |
| t_{WHGL} | t_{OEHL} | Write Enable High to Output Enable Low | Min | 0 | 0 | ns |
| t_{VCHEL} | t_{VCS} | V_{CC} High to Chip Enable Low | Min | 50 | 50 | μ s |

Figure 8. Write AC Waveforms, Write Enable Controlled



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Table 12. Write AC Characteristics, Chip Enable Controlled
($T_A = 0$ to 70 °C)

| Symbol | Alt | Parameter | | M29F512B | | Unit |
|-------------|------------|---------------------------------------|-----|----------|----|---------|
| | | | | 45 | 70 | |
| t_{AVAV} | t_{WC} | Address Valid to Next Address Valid | Min | 45 | 70 | ns |
| t_{WLEL} | t_{WS} | Write Enable Low to Chip Enable Low | Min | 0 | 0 | ns |
| t_{ELEH} | t_{CP} | Chip Enable Low to Chip Enable High | Min | 40 | 45 | ns |
| t_{DVEH} | t_{DS} | Input Valid to Chip Enable High | Min | 25 | 30 | ns |
| t_{EHDX} | t_{DH} | Chip Enable High to Input Transition | Min | 0 | 0 | ns |
| t_{EHWH} | t_{WH} | Chip Enable High to Write Enable High | Min | 0 | 0 | ns |
| t_{EHEL} | t_{CPH} | Chip Enable High to Chip Enable Low | Min | 20 | 20 | ns |
| t_{AVEL} | t_{AS} | Address Valid to Chip Enable Low | Min | 0 | 0 | ns |
| t_{ELAX} | t_{AH} | Chip Enable Low to Address Transition | Min | 40 | 45 | ns |
| t_{GHEL} | | Output Enable High Chip Enable Low | Min | 0 | 0 | ns |
| t_{EHGL} | t_{OEHL} | Chip Enable High to Output Enable Low | Min | 0 | 0 | ns |
| t_{VCHWL} | t_{VCS} | V_{CC} High to Write Enable Low | Min | 50 | 50 | μ s |

Figure 9. Write AC Waveforms, Chip Enable Controlled

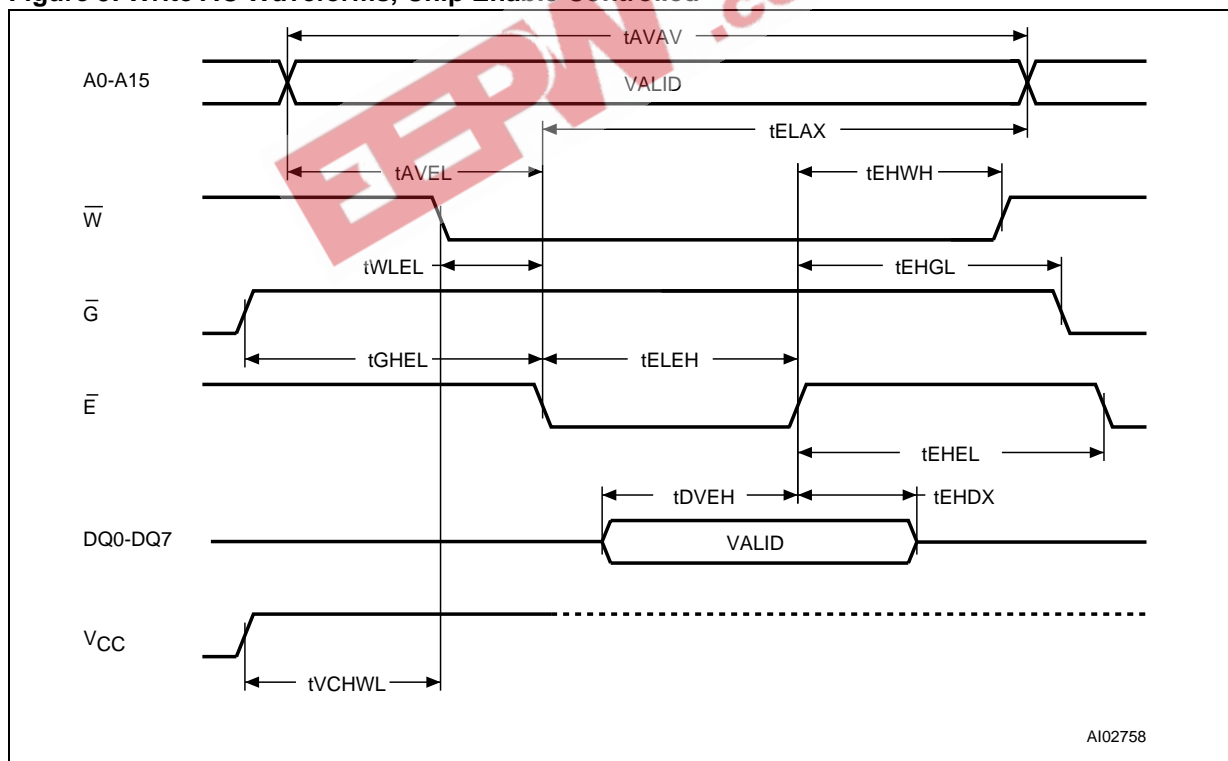


Table 13. Ordering Information Scheme

| Example: | M29F512B | 70 | NZ | 1 | T |
|--------------------------|--------------------------------------|----|----|---|---|
| Device Type | M29 | | | | |
| Operating Voltage | F = $V_{CC} = 5V \pm 10\%$ | | | | |
| Device Function | 512B = 512 Kbit (64Kb x8), Bulk | | | | |
| Speed | 45 = 45 ns 70 = 70 ns | | | | |
| Package | NZ = TSOP32: 8 x 14 mm K = PLCC32 | | | | |
| Temperature Range | 1 = 0 to 70 °C | | | | |
| Option | T = Tape & Reel Packing | | | | |

Note: The last two characters of the ordering code may be replaced by a letter code for preprogrammed parts, otherwise devices are shipped from the factory with the memory content erased (to FFh).

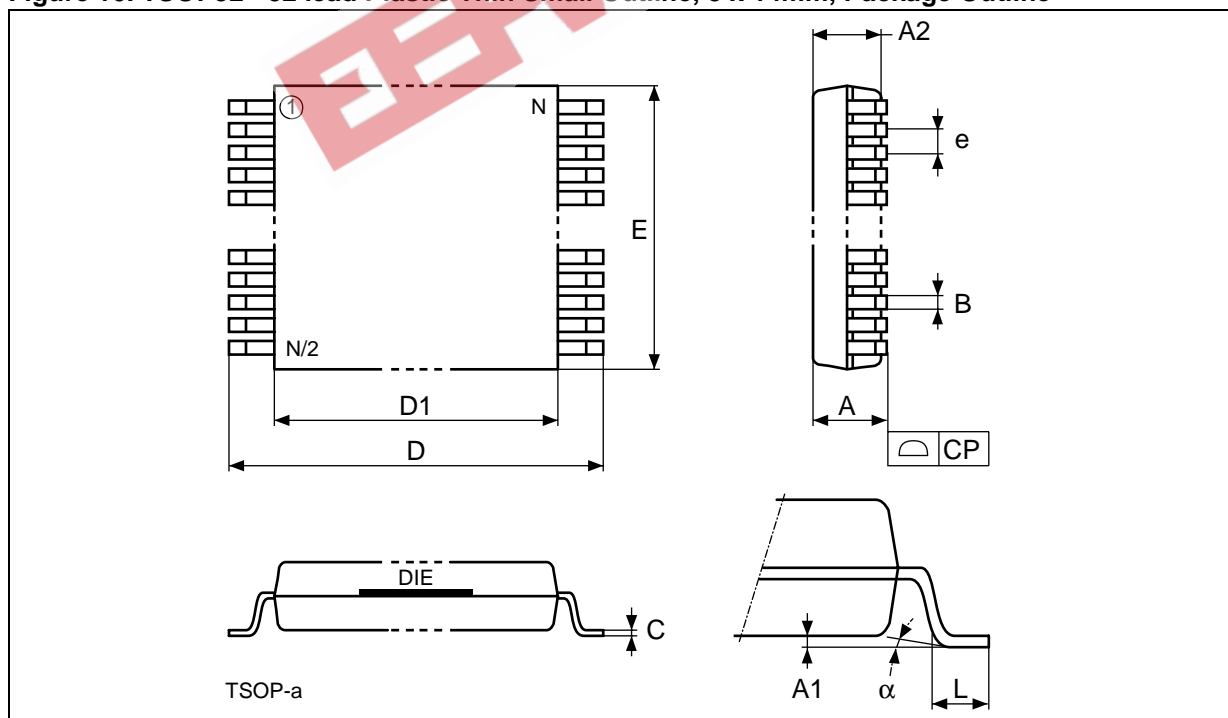
For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

M29F512B

Table 14. TSOP32 - 32 lead Plastic Thin Small Outline, 8 x 14mm, Package Mechanical Data

| Symbol | mm | | | inches | | |
|----------|------|-------|-------|--------|-------|-------|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 1.20 | | | 0.047 |
| A1 | | 0.05 | 0.15 | | 0.002 | 0.006 |
| A2 | | 0.95 | 1.05 | | 0.037 | 0.041 |
| B | | 0.17 | 0.27 | | 0.007 | 0.011 |
| C | | 0.10 | 0.21 | | 0.004 | 0.008 |
| D | | 13.80 | 14.20 | | 0.543 | 0.559 |
| D1 | | 12.30 | 12.50 | | 0.484 | 0.492 |
| E | | 7.90 | 8.10 | | 0.311 | 0.319 |
| e | 0.50 | - | - | 0.020 | - | - |
| L | | 0.50 | 0.70 | | 0.020 | 0.028 |
| α | | 0° | 5° | | 0° | 5° |
| N | 32 | | | 32 | | |
| CP | | | 0.10 | | | 0.004 |

Figure 10. TSOP32 - 32 lead Plastic Thin Small Outline, 8 x 14mm, Package Outline

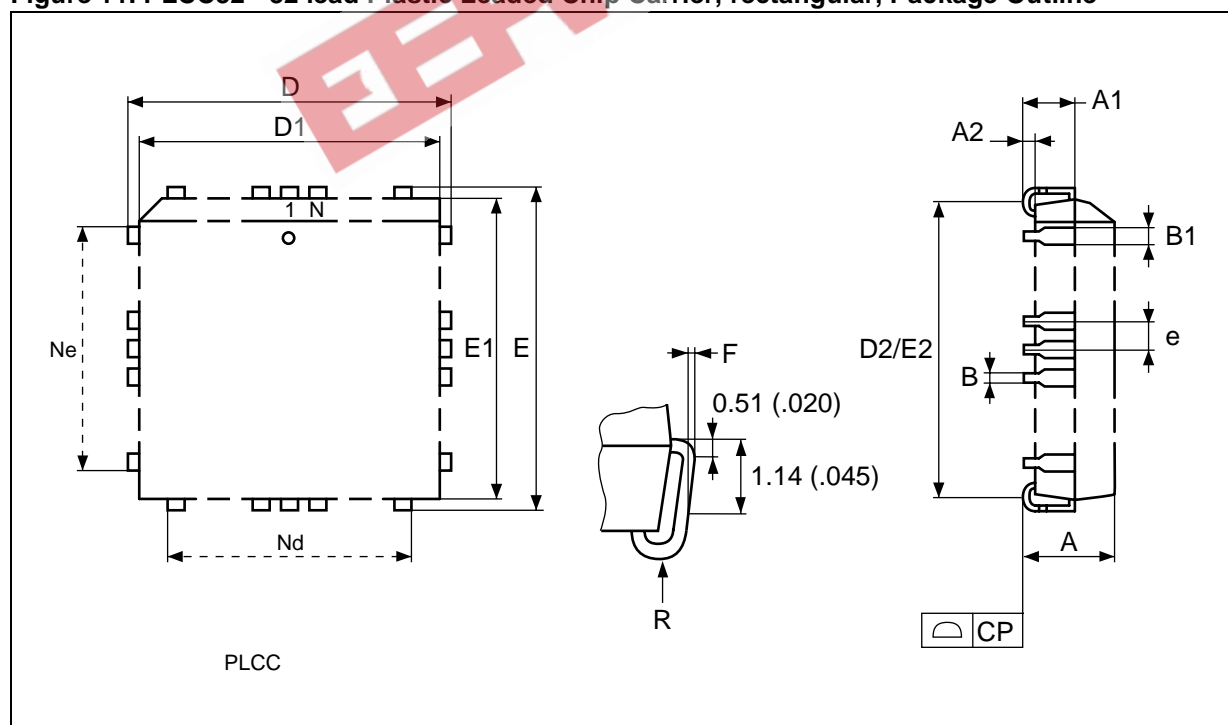


Drawing is not to scale.

Table 15. PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular, Package Mechanical Data

| Symbol | mm | | | inches | | |
|--------|------|-------|-------|--------|-------|-------|
| | Typ | Min | Max | Typ | Min | Max |
| A | | 2.54 | 3.56 | | 0.100 | 0.140 |
| A1 | | 1.52 | 2.41 | | 0.060 | 0.095 |
| A2 | | | 0.38 | | | 0.015 |
| B | | 0.33 | 0.53 | | 0.013 | 0.021 |
| B1 | | 0.66 | 0.81 | | 0.026 | 0.032 |
| D | | 12.32 | 12.57 | | 0.485 | 0.495 |
| D1 | | 11.35 | 11.56 | | 0.447 | 0.455 |
| D2 | | 9.91 | 10.92 | | 0.390 | 0.430 |
| E | | 14.86 | 15.11 | | 0.585 | 0.595 |
| E1 | | 13.89 | 14.10 | | 0.547 | 0.555 |
| E2 | | 12.45 | 13.46 | | 0.490 | 0.530 |
| e | 1.27 | – | – | 0.050 | – | – |
| F | | 0.00 | 0.25 | | 0.000 | 0.010 |
| R | 0.89 | – | – | 0.035 | – | – |
| N | | 32 | | | 32 | |
| Nd | | 7 | | | 7 | |
| Ne | | 9 | | | 9 | |
| CP | | | 0.10 | | | 0.004 |

Figure 11. PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular, Package Outline



Drawing is not to scale.



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