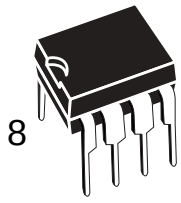
M93S66, M93S56
M93S46

4Kbit, 2Kbit and 1Kbit (16-bit wide)
MICROWIRE Serial Access EEPROM with Block Protection

FEATURES SUMMARY

- Industry Standard MICROWIRE Bus
- Single Supply Voltage:
  - 4.5 to 5.5V for M93Sx6
  - 2.5 to 5.5V for M93Sx6-W
  - 1.8 to 5.5V for M93Sx6-R
- Single Organization: by Word (x16)
- Programming Instructions that work on: Word or Entire Memory
- Self-timed Programming Cycle with Auto-Erase
- User Defined Write Protected Area
- Page Write Mode (4 words)
- Ready/$\overline{\text{Busy}}$ Signal During Programming
- Speed:
  - 1MHz Clock Rate, 10ms Write Time (Current product, identified by process identification letter F or M)
  - 2MHz Clock Rate, 5ms Write Time (New Product, identified by process identification letter W or G)
- Sequential Read Operation
- Enhanced ESD/Latch-Up Behavior
- More than 1 Million Erase/Write Cycles
- More than 40 Year Data Retention

Figure 1. Packages



PDIP8 (BN)

SO8 (MN)
150 mil width

TSSOP8 (DS)
3x3mm body size

TSSOP8 (DW)
169 mil width

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SUMMARY DESCRIPTION

This specification covers a range of 4K, 2K, 1K bit serial Electrically Erasable Programmable Memory (EEPROM) products (respectively for M93S66, M93S56, M93S46). In this text, these products are collectively referred to as M93Sx6.

Figure 2. Logic Diagram

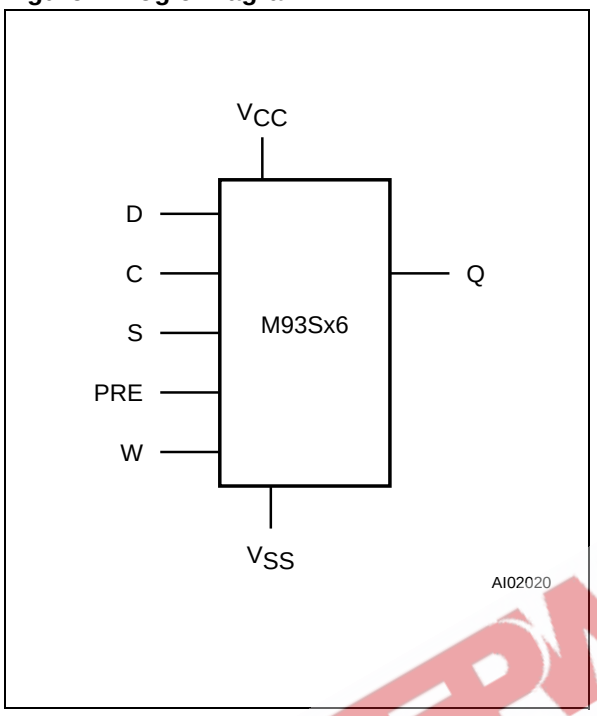


Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
PRE	Protection Register Enable
W	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

The M93Sx6 is accessed through a serial input (D) and output (Q) using the MICROWIRE bus protocol. The memory is divided into 256, 128, 64 x16 bit words (respectively for M93S66, M93S56, M93S46).

The M93Sx6 is accessed by a set of instructions which includes Read, Write, Page Write, Write All and instructions used to set the memory protection. These are summarized in Table 2. and Table 3.).

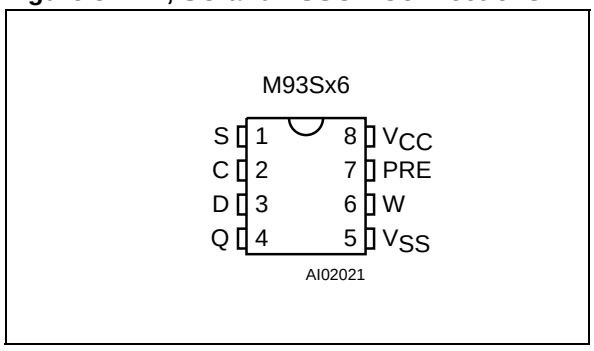
A Read Data from Memory (READ) instruction loads the address of the first word to be read into an internal address pointer. The data contained at this address is then clocked out serially. The address pointer is automatically incremented after the data is output and, if the Chip Select Input (S) is held High, the M93Sx6 can output a sequential stream of data words. In this way, the memory can be read as a data stream from 16 to 4096 bits (for the M93S66), or continuously as the address counter automatically rolls over to 00h when the highest address is reached.

Within the time required by a programming cycle (t_W), up to 4 words may be written with help of the Page Write instruction. the whole memory may also be erased, or set to a predetermined pattern, by using the Write All instruction.

Within the memory, a user defined area may be protected against further Write instructions. The size of this area is defined by the content of a Protection Register, located outside of the memory array. As a final protection step, data may be permanently protected by programming a One Time Programming bit (OTP bit) which locks the Protection Register content.

Programming is internally self-timed (the external clock signal on Serial Clock (C) may be stopped or left running after the start of a Write cycle) and does not require an erase cycle prior to the Write instruction. The Write instruction writes 16 bits at a time into one of the word locations of the M93Sx6, the Page Write instruction writes up to 4 words of 16 bits to sequential locations, assuming in both cases that all addresses are outside the Write Protected area. After the start of the programming cycle, a Busy/Ready signal is available on Serial Data Output (Q) when Chip Select Input (S) is driven High.

Figure 3. DIP, SO and TSSOP Connections



Note: See PACKAGE MECHANICAL section for package dimensions, and how to identify pin-1.

An internal Power-on Data Protection mechanism in the M93Sx6 inhibits the device when the supply is too low.

POWER-ON DATA PROTECTION

To prevent data corruption and inadvertent write operations during power-up, a Power-On Reset (POR) circuit resets all internal programming circuitry, and sets the device in the Write Disable mode.

– At Power-up and Power-down, the device must *not* be selected (that is, Chip Select Input (S) must be driven Low) until the supply voltage reaches the operating value V_{CC} specified in Table 5. to Table 6..

– When V_{CC} reaches its valid level, the device is properly reset (in the Write Disable mode) and is ready to decode and execute incoming instructions.

For the M93Sx6 devices (5V range) the POR threshold voltage is around 3V. For the M93Sx6-W (3V range) and M93Sx6-R (2V range) the POR threshold voltage is around 1.5V.

INSTRUCTIONS

The instruction set of the M93Sx6 devices contains seven instructions, as summarized in Table 2. to Table 3.. Each instruction consists of the following parts, as shown in Figure 4.:

- Each instruction is preceded by a rising edge on Chip Select Input (S) with Serial Clock (C) being held Low.
- A start bit, which is the first '1' read on Serial Data Input (D) during the rising edge of Serial Clock (C).
- Two op-code bits, read on Serial Data Input (D) during the rising edge of Serial Clock (C). (Some instructions also use the first two bits of the address to define the op-code).
- The address bits of the byte or word that is to be accessed. For the M93S46, the address is made up of 6 bits (see Table 2.). For the M93S56 and M93S66, the address is made up of 8 bits (see Table 3.).

The M93Sx6 devices are fabricated in CMOS technology and are therefore able to run as slow as 0 Hz (static input signals) or as fast as the maximum ratings specified in Table 16. to Table 19..

Table 2. Instruction Set for the M93S46

Instruction	Description	W	PRE	Start bit	Op-Code	Address[1]	Data	Required Clock Cycles	Additional Comments
READ	Read Data from Memory	X	0	1	10	A5-A0	Q15-Q0		
WRITE	Write Data to Memory	1	0	1	01	A5-A0	D15-D0	25	Write is executed if the address is not inside the Protected area
PAWRITE	Page Write to Memory	1	0	1	11	A5-A0	N x D15-D0	9 + N x 16	Write is executed if all the N addresses are not inside the Protected area
WRAL	Write All Memory with same Data	1	0	1	00	01 XXXX	D15-D0	25	Write all data if the Protection Register is cleared
WEN	Write Enable	1	0	1	00	11 XXXX		9	
WDS	Write Disable	X	0	1	00	00 XXXX		9	
PRREAD	Protection Register Read	X	1	1	10	XXXXXX	Q5-Q0 + Flag		Data Output = Protection Register content + Protection Flag bit
PRWRITE	Protection Register Write	1	1	1	01	A5-A0		9	Data above specified address A5-A0 are protected
PRCLEAR	Protection Register Clear	1	1	1	11	111111		9	Protect Flag is also cleared (cleared Flag = 1)
PREN	Protection Register Enable	1	1	1	00	11XXXX		9	
PRDS	Protection Register Disable	1	1	1	00	000000		9	OTP bit is set permanently

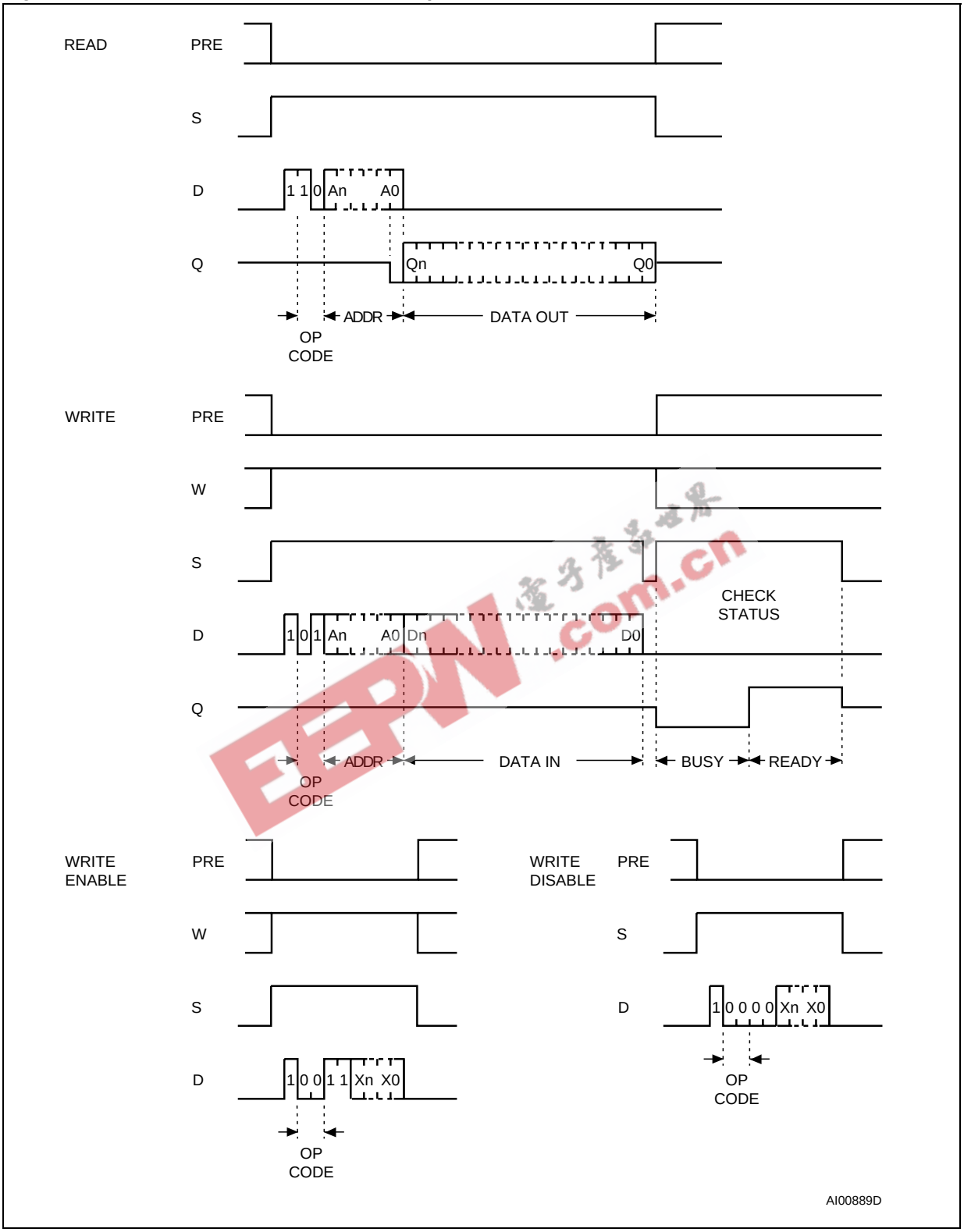
Note: 1. X = Don't Care bit.

Table 3. Instruction Set for the M93S66, M93S56

Instruction	Description	W	PRE	Start bit	Op-Code	Address[1,2]	Data	Required Clock Cycles	Additional Comments
READ	Read Data from Memory	X	0	1	10	A7-A0	Q15-Q0		
WRITE	Write Data to Memory	1	0	1	01	A7-A0	D15-D0	27	Write is executed if the address is not inside the Protected area
PAWRITE	Page Write to Memory	1	0	1	11	A7-A0	N x D15-D0	11 + N x 16	Write is executed if all the N addresses are not inside the Protected area
WRAL	Write All Memory with same Data	1	0	1	00	01XXXXXX	D15-D0	27	Write all data if the Protection Register is cleared
WEN	Write Enable	1	0	1	00	11XXXXXX		11	
WDS	Write Disable	X	0	1	00	00XXXXXX		11	
PRREAD	Protection Register Read	X	1	1	10	XXXXXXXX	Q7-Q0 + Flag		Data Output = Protection Register content + Protection Flag bit
PRWRITE	Protection Register Write	1	1	1	01	A7-A0		11	Data above specified address A7-A0 are protected
PRCLEAR	Protection Register Clear	1	1	1	11	11111111		11	Protect Flag is also cleared (cleared Flag = 1)
PREN	Protection Register Enable	1	1	1	00	11XXXXXX		11	
PRDS	Protection Register Disable	1	1	1	00	00000000		11	OTP bit is set permanently

Note: 1. X = Don't Care bit.
2. Address bit A7 is not decoded by the M93S56.

Figure 4. READ, WRITE, WEN and WDS Sequences



Note: For the meanings of An, Xn, Qn and Dn, see Table 2. and Table 3..

Read

The Read Data from Memory (READ) instruction outputs serial data on Serial Data Output (Q). When the instruction is received, the op-code and address are decoded, and the data from the memory is transferred to an output shift register. A dummy 0 bit is output first, followed by the 16-bit word, with the most significant bit first. Output data changes are triggered by the rising edge of Serial Clock (C). The M93Sx6 automatically increments the internal address register and clocks out the next byte (or word) as long as the Chip Select Input (S) is held High. In this case, the dummy 0 bit is *not* output between bytes (or words) and a continuous stream of data can be read.

Write Enable and Write Disable

The Write Enable (WEN) instruction enables the future execution of write instructions, and the Write Disable (WDS) instruction disables it. When power is first applied, the M93Sx6 initializes itself so that write instructions are disabled. After an Write Enable (WEN) instruction has been executed, writing remains enabled until an Write Disable (WDS) instruction is executed, or until V_{CC} falls below the power-on reset threshold voltage. To protect the memory contents from accidental corruption, it is advisable to issue the Write Disable (WDS) instruction after every write cycle. The Read Data from Memory (READ) instruction is not affected by the Write Enable (WEN) or Write Disable (WDS) instructions.

Write

The Write Data to Memory (WRITE) instruction is composed of the Start bit plus the op-code followed by the address and the 16 data bits to be written.

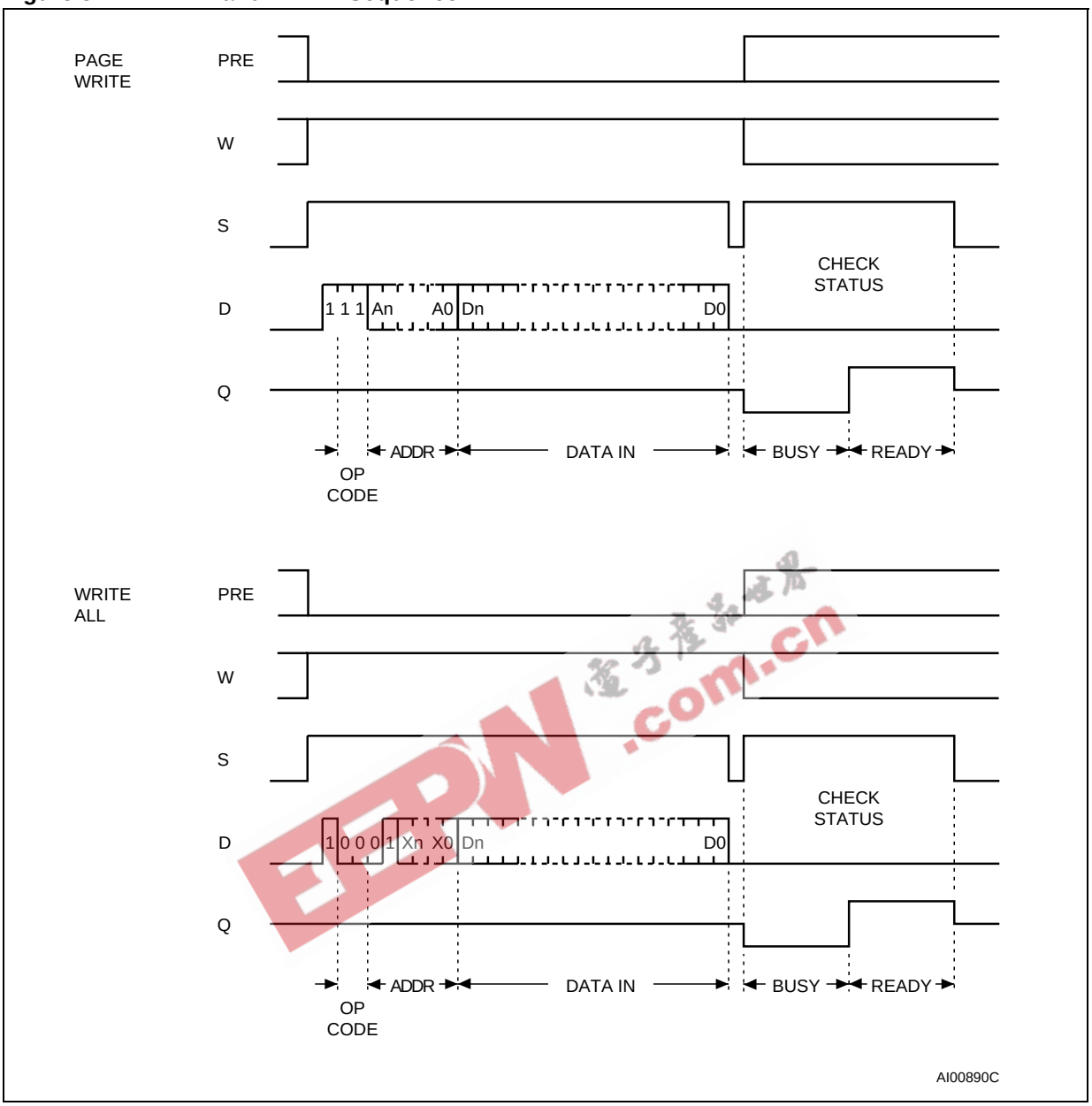
Write Enable (W) must be held High before and during the instruction. Input address and data, on Serial Data Input (D) are sampled on the rising edge of Serial Clock (C).

After the last data bit has been sampled, *the Chip Select Input (S) must be taken Low before the next rising edge of Serial Clock (C).* If Chip Select Input (S) is brought Low before or after this specific time frame, the self-timed programming cycle will not be started, and the addressed location will not be programmed.

While the M93Sx6 is performing a write cycle, but after a delay (t_{SLSH}) before the status information becomes available, Chip Select Input (S) can be driven High to monitor the status of the write cycle: Serial Data Output (Q) is driven Low while the M93Sx6 is still busy, and High when the cycle is complete, and the M93Sx6 is ready to receive a new instruction. The M93Sx6 ignores any data on the bus while it is busy on a write cycle. Once the M93Sx6 is Ready, Serial Data Output (Q) is driven High, and remains in this state until a new start bit is decoded or the Chip Select Input (S) is brought Low.

Programming is internally self-timed, so the external Serial Clock (C) may be disconnected or left running after the start of a write cycle.

Figure 5. PAWRITE and WRAL Sequence



Note: For the meanings of An, Xn and Dn, please see Table 2. and Table 3..

Page Write

A Page Write to Memory (PAWRITE) instruction contains the first address to be written, followed by up to 4 data words.

After the receipt of each data word, bits A1-A0 of the internal address register are incremented, the high order bits remaining unchanged (A7-A2 for M93S66, M93S56; A5-A2 for M93S46). Users must take care, in the software, to ensure that the last word address has the same upper order address bits as the initial address transmitted to avoid address roll-over.

The Page Write to Memory (PAWRITE) instruction will not be executed if any of the 4 words addresses the protected area.

Write Enable (W) must be held High before and during the instruction. Input address and data, on Serial Data Input (D) are sampled on the rising edge of Serial Clock (C).

After the last data bit has been sampled, *the Chip Select Input (S) must be taken Low before the next rising edge of Serial Clock (C).* If Chip Select Input (S) is brought Low before or after this specific time frame, the self-timed programming cycle will not

be started, and the addressed location will not be programmed.

While the M93Sx6 is performing a write cycle, but after a delay (t_{SLSH}) before the status information becomes available, Chip Select Input (S) can be driven High to monitor the status of the write cycle: Serial Data Output (Q) is driven Low while the M93Sx6 is still busy, and High when the cycle is complete, and the M93Sx6 is ready to receive a new instruction. The M93Sx6 ignores any data on the bus while it is busy on a write cycle. Once the M93Sx6 is Ready, Serial Data Output (Q) is driven High, and remains in this state until a new start bit is decoded or the Chip Select Input (S) is brought Low.

Programming is internally self-timed, so the external Serial Clock (C) may be disconnected or left running after the start of a write cycle.

Write All

The Write All Memory with same Data (WRAL) instruction is valid only after the Protection Register has been cleared by executing a Protection Register Clear (PRCLEAR) instruction. The Write All Memory with same Data (WRAL) instruction simultaneously writes the whole memory with the same data word given in the instruction.

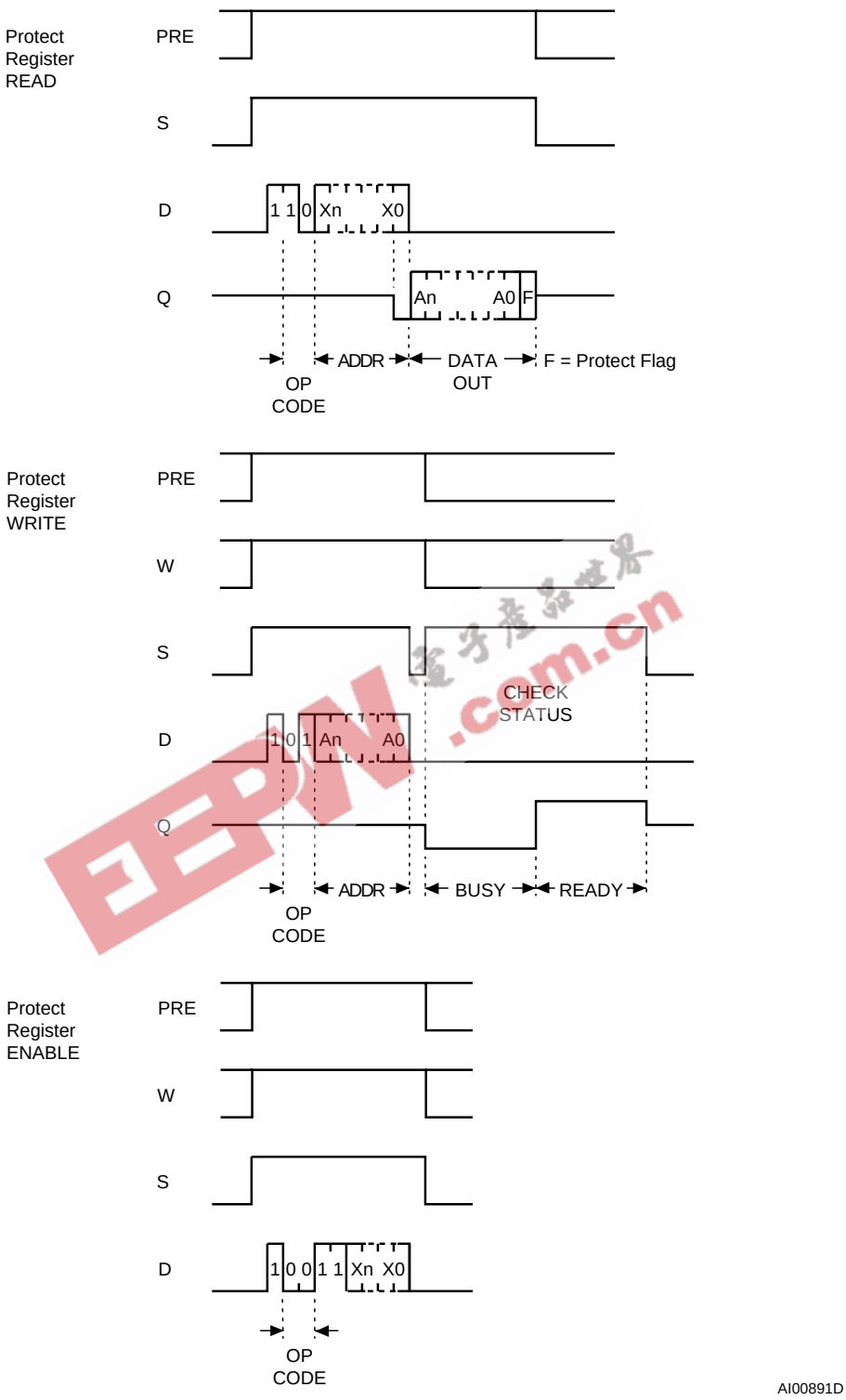
Write Enable (W) must be held High before and during the instruction. Input address and data, on Serial Data Input (D) are sampled on the rising edge of Serial Clock (C).

After the last data bit has been sampled, *the Chip Select Input (S) must be taken Low before the next rising edge of Serial Clock (C).* If Chip Select Input (S) is brought Low before or after this specific time frame, the self-timed programming cycle will not be started, and the addressed location will not be programmed.

While the M93Sx6 is performing a write cycle, but after a delay (t_{SLSH}) before the status information becomes available, Chip Select Input (S) can be driven High to monitor the status of the write cycle: Serial Data Output (Q) is driven Low while the M93Sx6 is still busy, and High when the cycle is complete, and the M93Sx6 is ready to receive a new instruction. The M93Sx6 ignores any data on the bus while it is busy on a write cycle. Once the M93Sx6 is Ready, Serial Data Output (Q) is driven High, and remains in this state until a new start bit is decoded or the Chip Select Input (S) is brought Low.

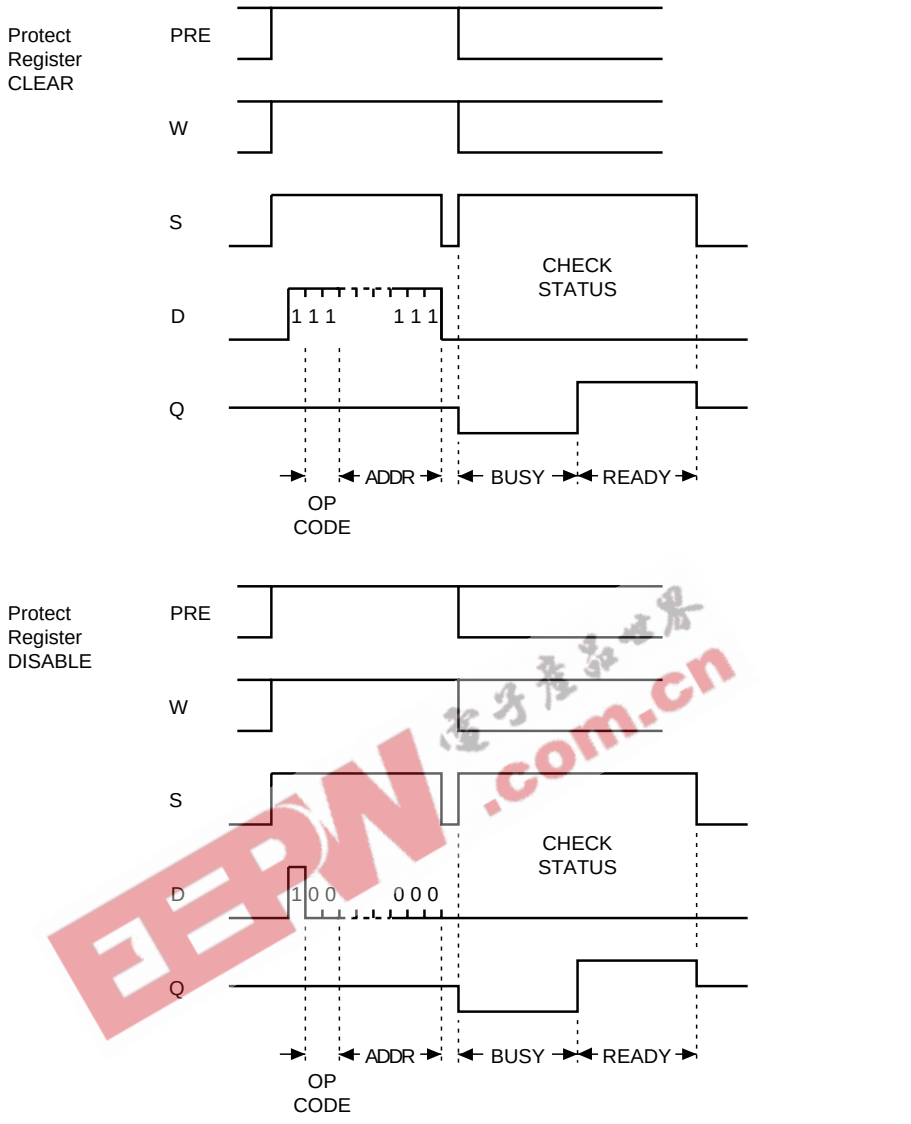
Programming is internally self-timed, so the external Serial Clock (C) may be disconnected or left running after the start of a write cycle.

Figure 6. PREAD, PRWRITE and PREN Sequences



Note: For the meanings of An, Xn and Dn, please see Table 2. and Table 3..

Figure 7. PRCLEAR and PRDS Sequences



Note: For the meanings of An, Xn and Dn, please see Table 2. and Table 3..

WRITE PROTECTION AND THE PROTECTION REGISTER

The Protection Register on the M93Sx6 is used to adjust the amount of memory that is to be write protected. The write protected area extends from the address given in the Protection Register, up to the top address in the M93Sx6 device.

Two flag bits are used to indicate the Protection Register status:

– Protection Flag: this is used to enable/disable protection of the write-protected area of the M93Sx6 memory

– OTP bit: when set, this disables access to the Protection Register, and thus prevents any further modifications to the value in the Protection Register.

The lower-bound memory address is written to the Protection Register using the Protection Register Write (PRWRITE) instruction. It can be read using the Protection Register Read (PRREAD) instruction.

The Protection Register Enable (PREN) instruction must be executed before any PRCLEAR, PRWRITE or PRDS instruction, and with appropriate levels applied to the Protection Enable (PRE) and Write Enable (W) signals.

Write-access to the Protection Register is achieved by executing the following sequence:

– Execute the Write Enable (WEN) instruction

– Execute the Protection Register Enable (PREN) instruction

– Execute one PRWRITE, PRCLEAR or PRDS instructions, to set a new boundary address in the Protection Register, to clear the protection address (to all 1s), or permanently to freeze the value held in the Protection Register.

Protection Register Read

The Protection Register Read (PRREAD) instruction outputs, on Serial Data Output (Q), the content of the Protection Register, followed by the Protection Flag bit. The Protection Enable (PRE) signal must be driven High before and during the instruction.

As with the Read Data from Memory (READ) instruction, a dummy 0 bit is output first. Since it is not possible to distinguish between the Protection Register being cleared (all 1s) or having been written with all 1s, the user must check the Protection Flag status (and not the Protection Register content) to ascertain the setting of the memory protection.

Protection Register Enable

The Protection Register Enable (PREN) instruction is used to authorize the use of instructions that modify the Protection Register (PRWRITE, PRCLEAR, PRDS). The Protection Register Enable (PREN) instruction does not modify the Protection Flag bit value.

Note: A Write Enable (WEN) instruction must be executed before the Protection Register Enable (PREN) instruction. Both the Protection Enable (PRE) and Write Enable (W) signals must be driven High during the instruction execution.

Protection Register Clear

The Protection Register Clear (PRCLEAR) instruction clears the address stored in the Protection Register to all 1s, so that none of the memory is write-protected by the Protection Register. However, it should be noted that all the memory remains protected, in the normal way, using the Write Enable (WEN) and Write Disable (WDS) instructions.

The Protection Register Clear (PRCLEAR) instruction clears the Protection Flag to 1. Both the Protection Enable (PRE) and Write Enable (W) signals must be driven High during the instruction execution.

Note: A Protection Register Enable (PREN) instruction must immediately precede the Protection Register Clear (PRCLEAR) instruction.

Protection Register Write

The Protection Register Write (PRWRITE) instruction is used to write an address into the Protection Register. This is the address of the first word to be protected. After the Protection Register Write (PRWRITE) instruction has been executed, all memory locations equal to and above the specified address are protected from writing.

The Protection Flag bit is set to 0, and can be read with Protection Register Read (PRREAD) instruction. Both the Protection Enable (PRE) and Write Enable (W) signals must be driven High during the instruction execution.

Note: A Protection Register Enable (PREN) instruction must immediately precede the Protection Register Write (PRWRITE) instruction, but it is not necessary to execute first a Protection Register Clear (PRCLEAR).

Protection Register Disable

The Protection Register Disable (PRDS) instruction sets the One Time Programmable (OTP) bit. This instruction is a ONE TIME ONLY instruction which latches the Protection Register content, this content is therefore unalterable in the future. Both the Protection Enable (PRE) and Write Enable (W) signals must be driven High during the instruction execution. The OTP bit cannot be directly read, it can be checked by reading the content of the Protection Register, using the Protection Register Read (PRREAD) instruction, then by writing this same value back into the Protection Register, us-

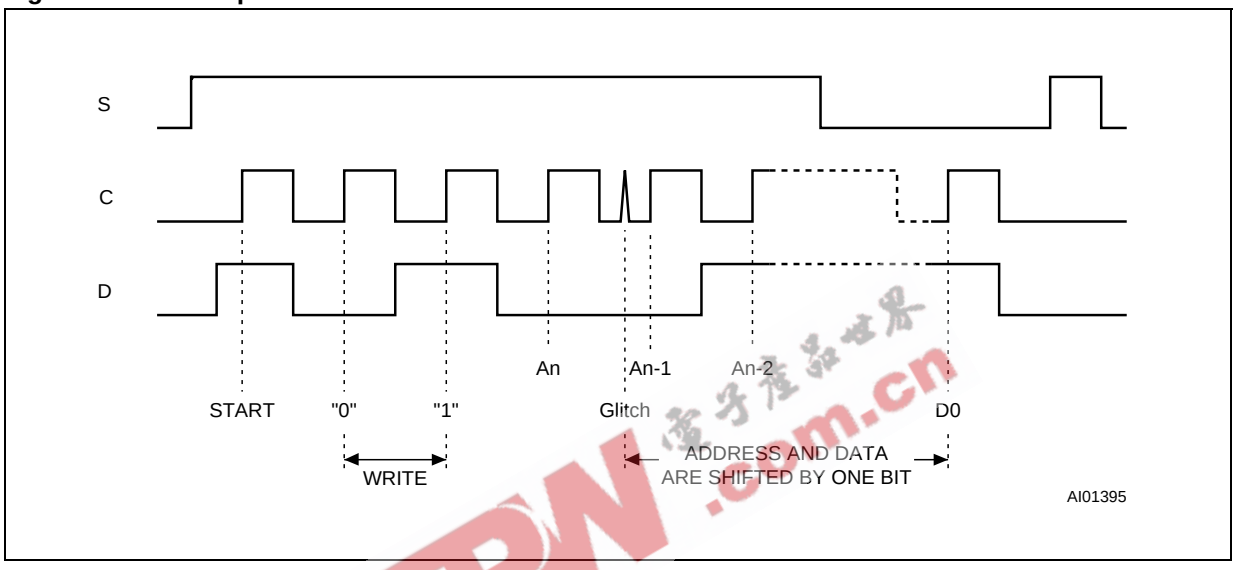
ing the Protection Register Write (PRWRITE) instruction. When the OTP bit is set, the Ready/Busy status cannot appear on Serial Data Output (Q). When the OTP bit is not set, the Busy status appears on Serial Data Output (Q).

Note: A Protection Register Enable (PREN) instruction must immediately precede the Protection Register Disable (PRDS) instruction.

COMMON I/O OPERATION

Serial Data Output (Q) and Serial Data Input (D) can be connected together, through a current limiting resistor, to form a common, single-wire data bus. Some precautions must be taken when operating the memory in this way, mostly to prevent a short circuit current from flowing when the last address bit (A0) clashes with the first data bit on Serial Data Output (Q). Please see the application note *AN394* for details.

Figure 8. Write Sequence with One Clock Glitch



CLOCK PULSE COUNTER

In a noisy environment, the number of pulses received on Serial Clock (C) may be greater than the number delivered by the Bus Master (the microcontroller). This can lead to a misalignment of the instruction of one or more bits (as shown in Figure 8.) and may lead to the writing of erroneous data at an erroneous address.

To combat this problem, the M93Sx6 has an on-chip counter that counts the clock pulses from the start bit until the falling edge of the Chip Select Input (S). If the number of clock pulses received is not the number expected, the WRITE, PAWRITE, WRALL, PRWRITE or PRCLEAR instruction is aborted, and the contents of the memory are not modified.

The number of clock cycles expected for each instruction, and for each member of the M93Sx6 family, are summarized in Table 2. to Table 3.. For example, a Write Data to Memory (WRITE) instruction on the M93S56 (or M93S66) expects 27 clock cycles from the start bit to the falling edge of Chip Select Input (S). That is:

1 Start bit
+ 2 Op-code bits
+ 8 Address bits
+ 16 Data bits

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage Temperature	–65	150	°C
T_{LEAD}	Lead Temperature during Soldering	See note [1]		°C
V_{OUT}	Output range (Q = V_{OH} or Hi-Z)	–0.50	V_{CC}+0.5	V
V_{IN}	Input range	–0.50	V_{CC}+1	V
V_{CC}	Supply Voltage	–0.50	6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]	–4000	4000	V

Note: 1. Compliant with JEDEC Std J-STD-020B (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU
2. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 5. Operating Conditions (M93Sx6)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
T_A	Ambient Operating Temperature (Device Grade 6)	–40	85	°C
	Ambient Operating Temperature (Device Grade 3)	–40	125	°C

Table 6. Operating Conditions (M93Sx6-W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.5	5.5	V
T_A	Ambient Operating Temperature (Device Grade 6)	–40	85	°C

Table 7. Operating Conditions (M93Sx6-R)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	1.8	5.5	V
T_A	Ambient Operating Temperature (Device Grade 6)	–40	85	°C

Table 8. AC Measurement Conditions (M93Sx6)

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	100		pF
	Input Rise and Fall Times		50	ns
	Input Pulse Voltages	0.4 V to 2.4 V		V
	Input Timing Reference Voltages	1.0 V and 2.0 V		V
	Output Timing Reference Voltages	0.8 V and 2.0 V		V

Note: Output Hi-Z is defined as the point where data out is no longer driven.

Table 9. AC Measurement Conditions (M93Sx6-W and M93Sx6-R)

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	100		pF
	Input Rise and Fall Times		50	ns
	Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V
	Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V

Note: Output Hi-Z is defined as the point where data out is no longer driven.

Figure 9. AC Testing Input Output Waveforms

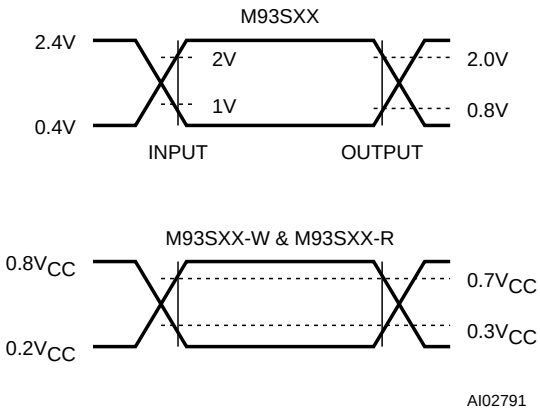


Table 10. Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF

Note: Sampled only, not 100% tested, at T_A=25°C and a frequency of 1 MHz.

Table 11. DC Characteristics (M93Sx6, Device Grade 6)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply Current	V_{CC} = 5V, S = V_{IH}, f = 1 MHz, Current Product [1]		1.5	mA
		V_{CC} = 5V, S = V_{IH}, f = 2 MHz, New Product [2]		2	mA
I_{CC1}	Supply Current (Stand-by)	V_{CC} = 5V, S = V_{SS}, C = V_{SS}, Current Product [1]		50	µA
		V_{CC} = 5V, S = V_{SS}, C = V_{SS}, New Product [2]		15	µA
V_{IL}	Input Low Voltage	V_{CC} = 5V ± 10%	–0.45	0.8	V
V_{IH}	Input High Voltage	V_{CC} = 5V ± 10%	2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	V_{CC} = 5V, I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	V_{CC} = 5V, I_{OH} = –400µA	2.4		V

Note: 1. Current product: identified by Process Identification letter F or M.
2. New product: identified by Process Identification letter W or G.

Table 12. DC Characteristics (M93Sx6, Device Grade 3)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply Current	V_{CC} = 5V, S = V_{IH}, f = 1 MHz, Current Product [1]		1.5	mA
		V_{CC} = 5V, S = V_{IH}, f = 2 MHz, New Product [2]		2	mA
I_{CC1}	Supply Current (Stand-by)	V_{CC} = 5V, S = V_{SS}, C = V_{SS}, Current Product [1]		50	µA
		V_{CC} = 5V, S = V_{SS}, C = V_{SS}, New Product [2]		15	µA
V_{IL}	Input Low Voltage	V_{CC} = 5V ± 10%	–0.45	0.8	V
V_{IH}	Input High Voltage	V_{CC} = 5V ± 10%	2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	V_{CC} = 5V, I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	V_{CC} = 5V, I_{OH} = –400µA	2.4		V

Note: 1. Current product: identified by Process Identification letter F or M.
2. New product: identified by Process Identification letter W or G.

Table 13. DC Characteristics (M93Sx6-W, Device Grade 6)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply Current (CMOS Inputs)	V_{CC} = 5V, S = V_{IH}, f = 1 MHz, Current Product [1]		1.5	mA
		V_{CC} = 2.5V, S = V_{IH}, f = 1 MHz, Current Product [1]		1	mA
		V_{CC} = 5V, S = V_{IH}, f = 2 MHz, New Product [2]		2	mA
		V_{CC} = 2.5V, S = V_{IH}, f = 2 MHz, New Product [2]		1	mA
I_{CC1}	Supply Current (Stand-by)	V_{CC} = 2.5V, S = V_{SS}, C = V_{SS}, Current Product [1]		10	µA
		V_{CC} = 2.5V, S = V_{SS}, C = V_{SS}, New Product [2]		5	µA
V_{IL}	Input Low Voltage (D, C, S)		–0.45	0.2 V_{CC}	V
V_{IH}	Input High Voltage (D, C, S)		0.7 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage (Q)	V_{CC} = 5V, I_{OL} = 2.1mA		0.4	V
		V_{CC} = 2.5V, I_{OL} = 100µA		0.2	V
V_{OH}	Output High Voltage (Q)	V_{CC} = 5V, I_{OH} = –400µA	2.4		V
		V_{CC} = 2.5V, I_{OH} = –100µA	V_{CC}–0.2		V

Note: 1. Current product: identified by Process Identification letter F or M.
2. New product: identified by Process Identification letter W or G.

Table 14. DC Characteristics (M93Sx6-W, Device Grade 3)

Symbol	Parameter	Test Condition	Min [1].	Max. [1]	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply Current (CMOS Inputs)	V_{CC} = 5V, S = V_{IH}, f = 2 MHz		2	mA
		V_{CC} = 2.5V, S = V_{IH}, f = 2 MHz		1	mA
I_{CC1}	Supply Current (Stand-by)	V_{CC} = 2.5V, S = V_{SS}, C = V_{SS}		5	µA
V_{IL}	Input Low Voltage (D, C, S)		–0.45	0.2 V_{CC}	V
V_{IH}	Input High Voltage (D, C, S)		0.7 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage (Q)	V_{CC} = 5V, I_{OL} = 2.1mA		0.4	V
		V_{CC} = 2.5V, I_{OL} = 100µA		0.2	V
V_{OH}	Output High Voltage (Q)	V_{CC} = 5V, I_{OH} = –400µA	2.4		V
		V_{CC} = 2.5V, I_{OH} = –100µA	V_{CC}–0.2		V

Note: 1. New product: identified by Process Identification letter W or G.

Table 15. DC Characteristics (M93Sx6-R)

Symbol	Parameter	Test Condition	Min. [1]	Max. [1]	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply Current (CMOS Inputs)	V_{CC} = 5V, S = V_{IH}, f = 2 MHz		2	mA
		V_{CC} = 1.8V, S = V_{IH}, f = 1 MHz		1	mA
I_{CC1}	Supply Current (Stand-by)	V_{CC} = 1.8V, S = V_{SS}, C = V_{SS}		2	µA
V_{IL}	Input Low Voltage (D, C, S)		–0.45	0.2 V_{CC}	V
V_{IH}	Input High Voltage (D, C, S)		0.8 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage (Q)	V_{CC} = 1.8V, I_{OL} = 100µA		0.2	V
V_{OH}	Output High Voltage (Q)	V_{CC} = 1.8V, I_{OH} = –100µA	V_{CC}–0.2		V

Note: 1. Preliminary Data: this product is under development. For more infomation, please contact your nearest ST sales office.

Table 16. AC Characteristics (M93Sx6, Device Grade 6 or 3)

Test conditions specified in Table 8. and Table 5.							
Symbol	**Alt.**	**Parameter**	**Min.[3]**	**Max.[3]**	**Min.[4]**	**Max.[4]**	**Unit**
f_C	f_{SK}	Clock Frequency	D.C.	1	D.C.	2	MHz
t_{PRVCH}	t_{PRES}	Protect Enable Valid to Clock High	50		50		ns
t_{WVCH}	t_{PES}	Write Enable Valid to Clock High	50		50		ns
t_{CLPRX}	t_{PREH}	Clock Low to Protect Enable Transition	0		0		ns
t_{SLWX}	t_{PEH}	Chip Select Low to Write Enable Transition	250		250		ns
t_{SLCH}		Chip Select Low to Clock High	250		50		ns
t_{SHCH}	t_{CSS}	Chip Select Set-up Time M93C46, M93C56, M93C66	50		50		ns
		Chip Select Set-up time M93C76, M93C86	100		50		ns
t_{SLSH}[2]	t_{CS}	Chip Select Low to Chip Select High	250		200		ns
t_{CHCL}[1]	t_{SKH}	Clock High Time	250		200		ns
t_{CLCH}[1]	t_{SKL}	Clock Low Time	250		200		ns
t_{DVCH}	t_{DIS}	Data In Set-up Time	100		50		ns
t_{CHDX}	t_{DIH}	Data In Hold Time	100		50		ns
t_{CLSH}	t_{SKS}	Clock Set-up Time (relative to S)	100		50		ns
t_{CLSL}	t_{CSH}	Chip Select Hold Time	0		0		ns
t_{SHQV}	t_{SV}	Chip Select to Ready/Busy Status		400		200	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z		200		100	ns
t_{CHQL}	t_{PD0}	Delay to Output Low		400		200	ns
t_{CHQV}	t_{PD1}	Delay to Output Valid		400		200	ns
t_W	t_{WP}	Erase/Write Cycle time		10		5	ms

Note: 1. $t_{CHCL} + t_{CLCH} \geq 1 / f_C$.
2. Chip Select Input (S) must be brought Low for a minimum of tSLSH between consecutive instruction cycles.
3. Current product: identified by Process Identification letter F or M.
4. New product: identified by Process Identification letter W or G.

Table 17. AC Characteristics (M93Sx6-W, Device Grade 6)

Test conditions specified in Table 9. and Table 6.							
Symbol	**Alt.**	**Parameter**	**Min.[3]**	**Max.[3]**	**Min.[4]**	**Max.[4]**	**Unit**
f_C	f_{SK}	Clock Frequency	D.C.	1	D.C.	2	MHz
t_{PRVCH}	t_{PRES}	Protect Enable Valid to Clock High	50		50		ns
t_{WVCH}	t_{PES}	Write Enable Valid to Clock High	50		50		ns
t_{CLPRX}	t_{PREH}	Clock Low to Protect Enable Transition	0		0		ns
t_{SLWX}	t_{PEH}	Chip Select Low to Write Enable Transition	250		250		ns
t_{SLCH}		Chip Select Low to Clock High	250		50		ns
t_{SHCH}	t_{CSS}	Chip Select Set-up Time	100		50		ns
t_{SLSH}[2]	t_{CS}	Chip Select Low to Chip Select High	1000		200		ns
t_{CHCL}[1]	t_{SKH}	Clock High Time	350		200		ns
t_{CLCH}[1]	t_{SKL}	Clock Low Time	250		200		ns
t_{DVCH}	t_{DIS}	Data In Set-up Time	100		50		ns
t_{CHDX}	t_{DIH}	Data In Hold Time	100		50		ns
t_{CLSH}	t_{SKS}	Clock Set-up Time (relative to S)	100		50		ns
t_{CLSL}	t_{CSH}	Chip Select Hold Time	0		0		ns
t_{SHQV}	t_{SV}	Chip Select to Ready/Busy Status		400		200	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z		200		100	ns
t_{CHQL}	t_{PD0}	Delay to Output Low		400		200	ns
t_{CHQV}	t_{PD1}	Delay to Output Valid		400		200	ns
t_W	t_{WP}	Erase/Write Cycle time		10		5	ms

Note: 1. $t_{CHCL} + t_{CLCH} \geq 1 / f_C$.
2. Chip Select Input (S) must be brought Low for a minimum of tSLSH between consecutive instruction cycles.
3. Current product: identified by Process Identification letter F or M.
4. New product: identified by Process Identification letter W or G.

Table 18. AC Characteristics (M93Sx6-W, Device Grade 3)

Test conditions specified in Table 9. and Table 6.					
Symbol	**Alt.**	**Parameter**	**Min.[3]**	**Max.[3]**	**Unit**
f_C	f_{SK}	Clock Frequency	D.C.	2	MHz
t_{PRVCH}	t_{PRES}	Protect Enable Valid to Clock High	50		ns
t_{WVCH}	t_{PES}	Write Enable Valid to Clock High	50		ns
t_{CLPRX}	t_{PREH}	Clock Low to Protect Enable Transition	0		ns
t_{SLWX}	t_{PEH}	Chip Select Low to Write Enable Transition	250		ns
t_{SLCH}		Chip Select Low to Clock High	50		ns
t_{SHCH}	t_{CSS}	Chip Select Set-up Time	50		ns
t_{SLSH}[2]	t_{CS}	Chip Select Low to Chip Select High	200		ns
t_{CHCL}[1]	t_{SKH}	Clock High Time	200		ns
t_{CLCH}[1]	t_{SKL}	Clock Low Time	200		ns
t_{DVCH}	t_{DIS}	Data In Set-up Time	50		ns
t_{CHDX}	t_{DIH}	Data In Hold Time	50		ns
t_{CLSH}	t_{SKS}	Clock Set-up Time (relative to S)	50		ns
t_{CLSL}	t_{CSH}	Chip Select Hold Time	0		ns
t_{SHQV}	t_{SV}	Chip Select to Ready/Busy Status		200	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z		100	ns
t_{CHQL}	t_{PD0}	Delay to Output Low		200	ns
t_{CHQV}	t_{PD1}	Delay to Output Valid		200	ns
t_W	t_{WP}	Erase/Write Cycle time		5	ms

Note: 1. $t_{CHCL} + t_{CLCH} \geq 1 / f_C$.
2. Chip Select Input (S) must be brought Low for a minimum of tSLSH between consecutive instruction cycles.
3. New product: identified by Process Identification letter W or G.

Table 19. AC Characteristics (M93Sx6-R)

Test conditions specified in Table 9. and Table 7.					
Symbol	**Alt.**	**Parameter**	**Min.[3]**	**Max.[3]**	**Unit**
f_C	f_{SK}	Clock Frequency	D.C.	1	MHz
t_{PRVCH}	t_{PRES}	Protect Enable Valid to Clock High	50		ns
t_{WVCH}	t_{PES}	Write Enable Valid to Clock High	50		ns
t_{CLPRX}	t_{PREH}	Clock Low to Protect Enable Transition	0		ns
t_{SLWX}	t_{PEH}	Chip Select Low to Write Enable Transition	250		ns
t_{SLCH}		Chip Select Low to Clock High	250		ns
t_{SHCH}	t_{CSS}	Chip Select Set-up Time	50		ns
t_{SLSH}[2]	t_{CS}	Chip Select Low to Chip Select High	250		ns
t_{CHCL}[1]	t_{SKH}	Clock High Time	250		ns
t_{CLCH}[1]	t_{SKL}	Clock Low Time	250		ns
t_{DVCH}	t_{DIS}	Data In Set-up Time	100		ns
t_{CHDX}	t_{DIH}	Data In Hold Time	100		ns
t_{CLSH}	t_{SKS}	Clock Set-up Time (relative to S)	100		ns
t_{CLSL}	t_{CSH}	Chip Select Hold Time	0		ns
t_{SHQV}	t_{SV}	Chip Select to Ready/Busy Status		400	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z		200	ns
t_{CHQL}	t_{PD0}	Delay to Output Low		400	ns
t_{CHQV}	t_{PD1}	Delay to Output Valid		400	ns
t_W	t_{WP}	Erase/Write Cycle time		10	ms

Note: 1. $t_{CHCL} + t_{CLCH} \geq 1 / f_C$.
2. Chip Select Input (S) must be brought Low for a minimum of tSLSH between consecutive instruction cycles.
3. Preliminary Data: this product is under development. For more infomation, please contact your nearest ST sales office.

Figure 10. Synchronous Timing (Start and Op-Code Input)

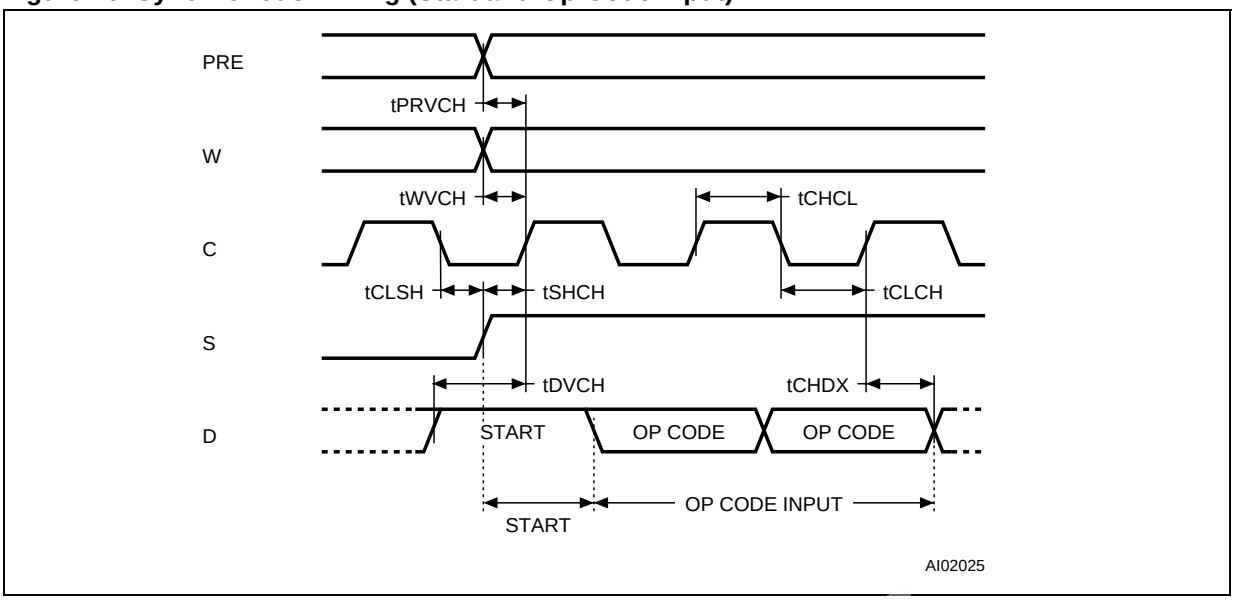


Figure 11. Synchronous Timing (Read or Write)

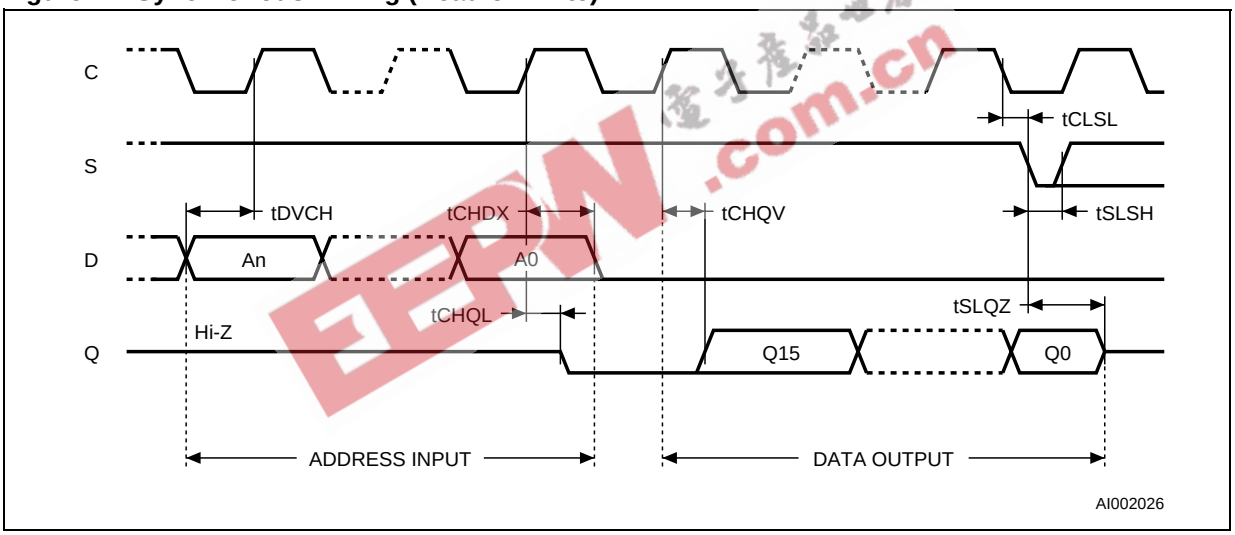
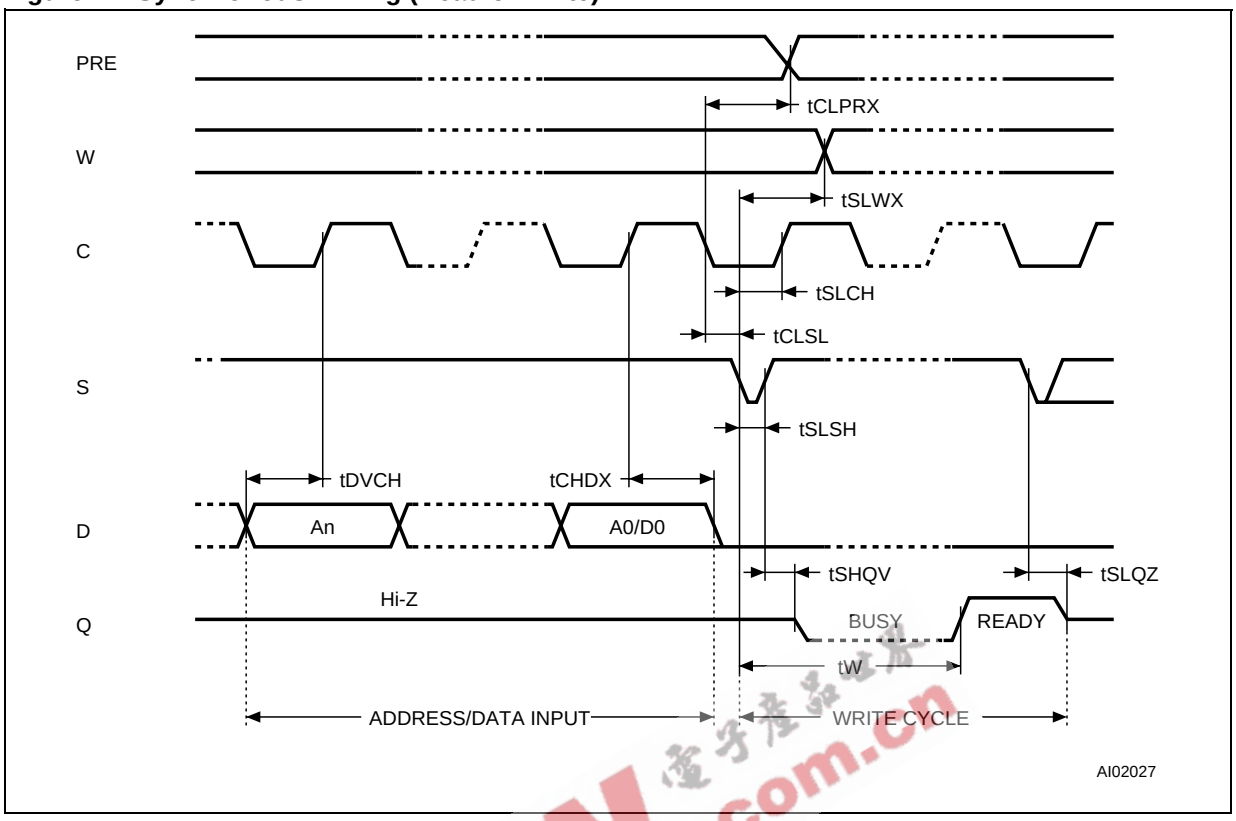
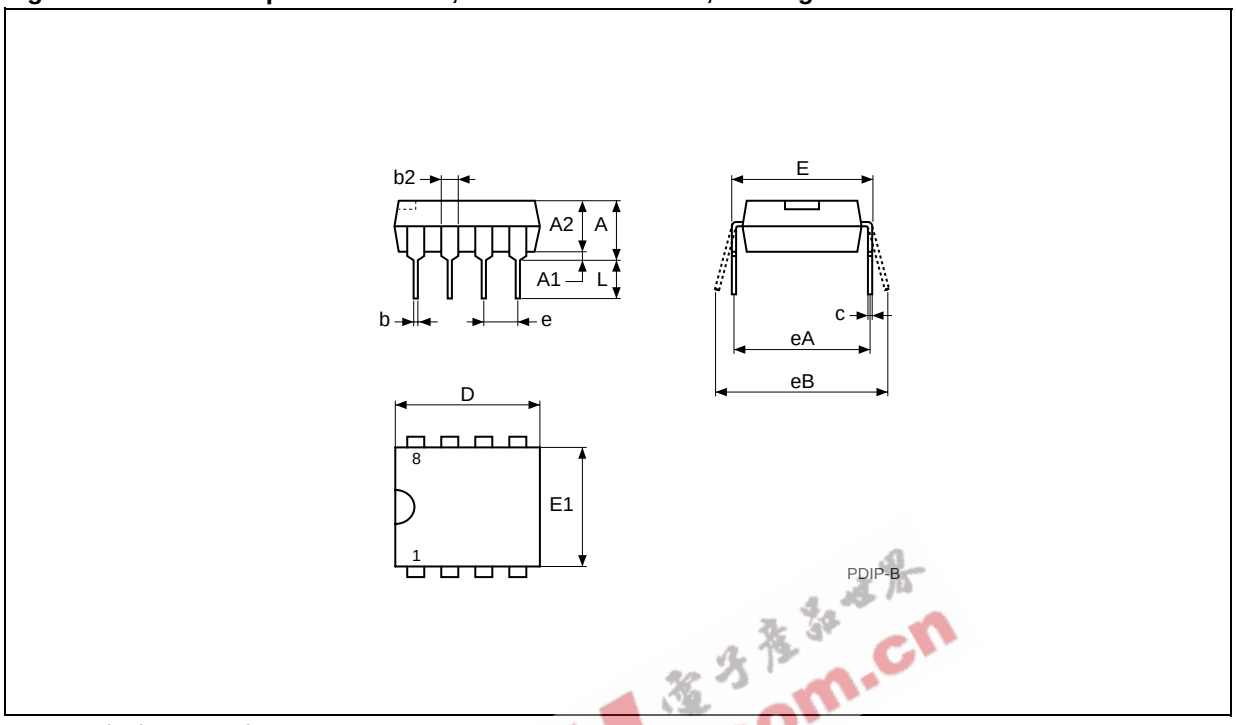


Figure 12. Synchronous Timing (Read or Write)



PACKAGE MECHANICAL

Figure 13. PDIP8 – 8 pin Plastic DIP, 0.25mm lead frame, Package Outline

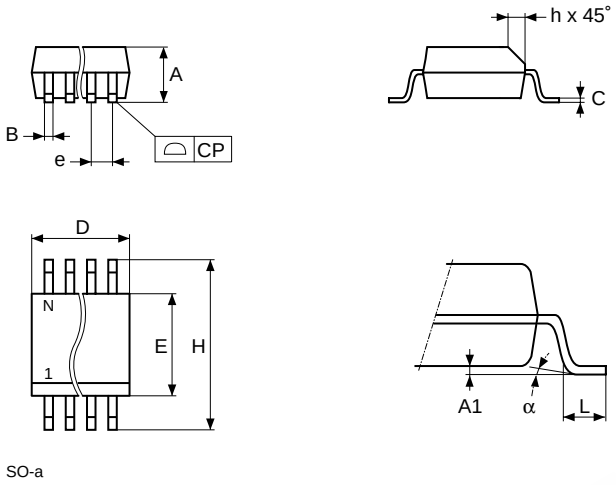


Note: Drawing is not to scale.

Table 20. PDIP8 – 8 pin Plastic DIP, 0.25mm lead frame, Package Mechanical Data

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			5.33			0.210
A1		0.38			0.015	
A2	3.30	2.92	4.95	0.130	0.115	0.195
b	0.46	0.36	0.56	0.018	0.014	0.022
b2	1.52	1.14	1.78	0.060	0.045	0.070
c	0.25	0.20	0.36	0.010	0.008	0.014
D	9.27	9.02	10.16	0.365	0.355	0.400
E	7.87	7.62	8.26	0.310	0.300	0.325
E1	6.35	6.10	7.11	0.250	0.240	0.280
e	2.54	–	–	0.100	–	–
eA	7.62	–	–	0.300	–	–
eB			10.92			0.430
L	3.30	2.92	3.81	0.130	0.115	0.150

Figure 14. SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width, Package Outline



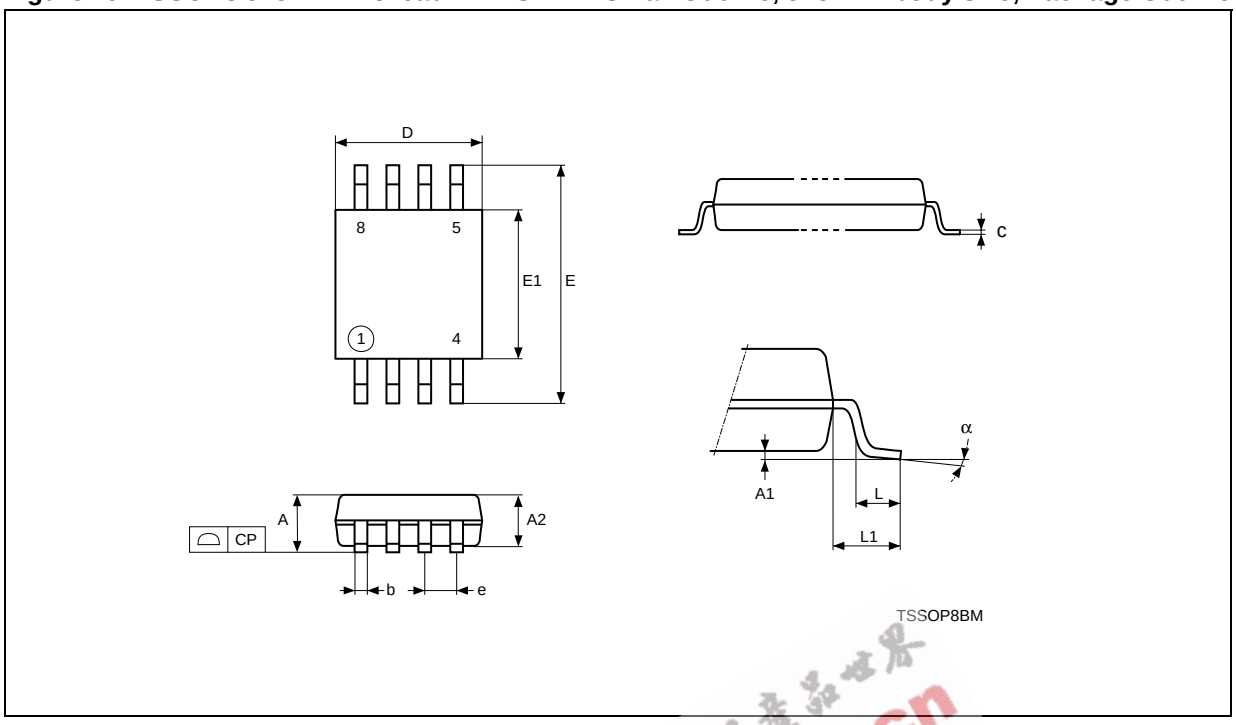
SO-a

Note: Drawing is not to scale.

Table 21. SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width, Package Mechanical Data

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

Figure 15. TSSOP8 3x3mm² – 8 lead Thin Shrink Small Outline, 3x3mm² body size, Package Outline

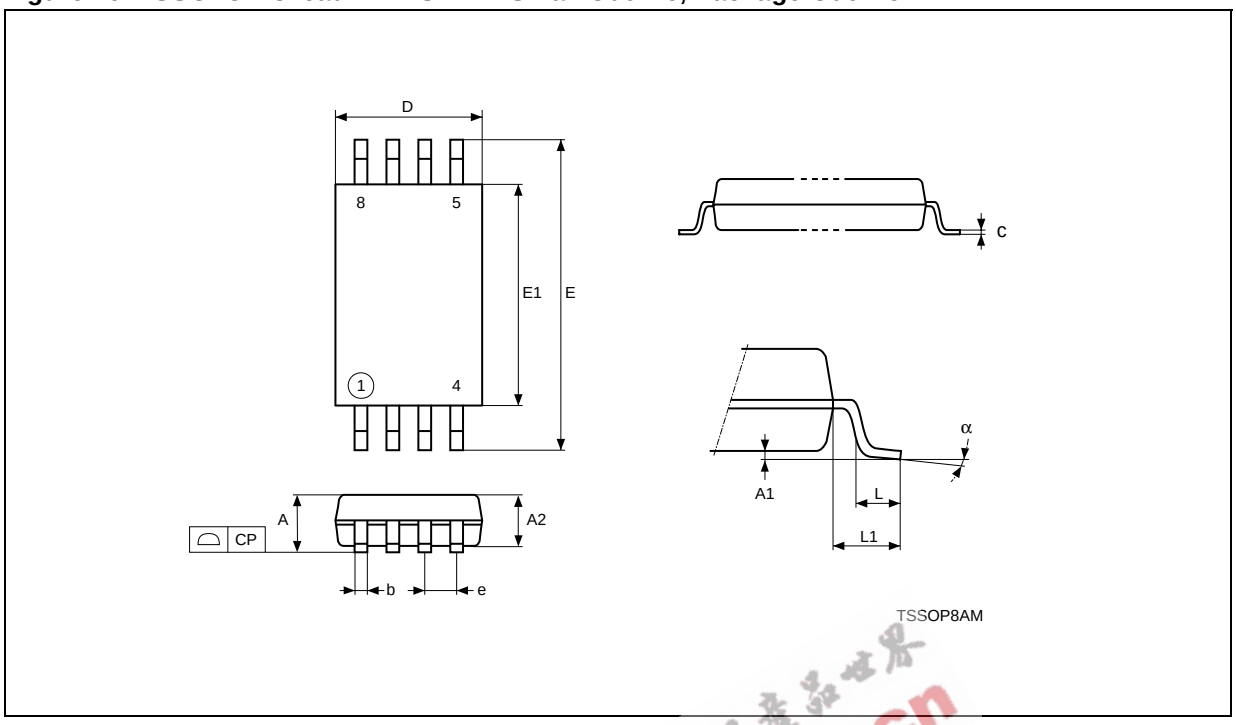


Note: Drawing is not to scale.

Table 22. TSSOP8 3x3mm² – 8 lead Thin Shrink Small Outline, 3x3mm² body size, Mechanical Data

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.100			0.0433
A1		0.050	0.150		0.0020	0.0059
A2	0.850	0.750	0.950	0.0335	0.0295	0.0374
b		0.250	0.400		0.0098	0.0157
c		0.130	0.230		0.0051	0.0091
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
E	4.900	4.650	5.150	0.1929	0.1831	0.2028
E1	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
CP			0.100			0.0039
L	0.550	0.400	0.700	0.0217	0.0157	0.0276
L1	0.950			0.0374		
α		0°	6°		0°	6°

Figure 16. TSSOP8 – 8 lead Thin Shrink Small Outline, Package Outline



Note: Drawing is not to scale.

Table 23. TSSOP8 – 8 lead Thin Shrink Small Outline, Package Mechanical Data

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
α		0°	8°		0°	8°

PART NUMBERING

Table 24. Ordering Information Scheme

Example: M93S66 – W MN 6 T P

Device Type

M93 = MICROWIRE serial access EEPROM (x16) with Block Protection

Device Function

66 = 4 Kbit (256 x 16)
56 = 2 Kbit (128 x 16)
46 = 1 Kbit (64 x 16)

Operating Voltage

blank = V_{CC} = 4.5 to 5.5V
W = V_{CC} = 2.5 to 5.5V
R = V_{CC} = 1.8 to 5.5V

Package

BN = PDIP8
MN = SO8 (150 mil width)
DW = TSSOP8 (169 mil width)
DS[2] = TSSOP8 (3x3mm body size)

Device Grade

6 = Industrial: device tested with standard test flow over –40 to 85 °C
3 = Automotive: device tested with High Reliability Certified Flow[1] over –40 to 125 °C

Option

blank = Standard Packing
T = Tape & Reel Packing

Plating Technology

blank = Standard SnPb plating
P = Lead-Free and RoHS compliant
G = Lead-Free, RoHS compliant, Sb_2O_3-free and TBBA-free

Note: 1. ST strongly recommends the use of the Automotive Grade devices for use in an automotive environment. The High Reliability Certified Flow (HRCF) is described in the quality note QNEE9801. Please ask your nearest ST sales office for a copy.
2. Available only on new products: identified by the Process Identification letter W or G.

Devices are shipped from the factory with the memory content set at all 1s (FFh).

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

Table 25. How to Identify Current and New Products by the Process Identification Letter

Markings on Current Products[1]	Markings on New Products[1]
M93S46W6 AYWW**F** (or AYWW**M**)	M93S46W6 AYWW**W** (or AYWW**G**)

Note: 1. This example comes from the S08 package. Other packages have similar information. For further information, please ask your ST Sales Office for Process Change Notice PCN MPG/EE/0059 (PCEE0059).

REVISION HISTORY

Table 26. Document Revision History

Date	Rev.	Description of Revision
07-Mar-2002	2.0	Document reformatted, and reworded, using the new template. Temperature range 1 removed. TSSOP8 (3x3mm) package added. New products, identified by the process letter W, added, with fc(max) increased to 1MHz for -R voltage range, and to 2MHz for all other ranges (and corresponding parameters adjusted).
26-Mar-2003	2.1	Value of standby current (max) corrected in DC characteristics tables for -W and -R ranges V_{OUT} and V_{IN} separated from V_{IO} in the Absolute Maximum Ratings table
14-Apr-2003	2.2	Values corrected in AC characteristics tables for -W range (tSLSH, tDVCH, tCLSL) for devices with Process Identification Letter W.
23-May-2003	2.3	Standby current corrected for -R range. Four missing parameters restored to all AC Characteristics tables
24-Nov-2003	3.0	Table of contents, and Pb-free options added. V_{IL}(min) improved to -0.45V.
19-Apr-2004	4.0	Absolute Maximum Ratings for V_{IO}(min) and V_{CC}(min) changed. Soldering temperature information clarified for RoHS compliant devices. Device Grade 3 clarified, with reference to HRCF and automotive environments. Process identification letter “G” information added