

MC14009AL
MC14009CL
MC14009CP
MC14010AL
MC14010CL
MC14010CP

HEX BUFFERS

The MC14009 hex inverter/buffer and MC14010 noninverting hex buffer are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. Both devices can be used as current "sink" or "source" drivers, as CMOS-to-CMOS or CMOS-to-bipolar (TTL or DTL) logic level converters, or as multiplexers (1-to-6). The MC14009 also provides the invert function.

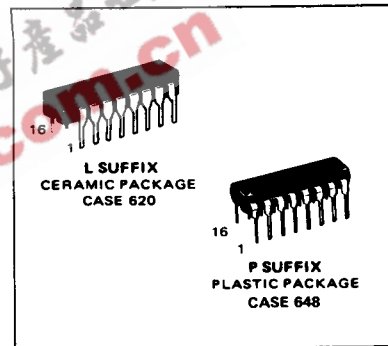
- Quiescent Power Dissipation = 50 nW/package typical
- High Current Sinking Capability
8.0 mA minimum @ $V_{OL} = 0.5\text{ V}$ and $V_{DD} = 10\text{ V}$
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14009/10 AL)
3.0 Vdc to 16 Vdc (MC14009/10CL/CP)
- Wide CMOS-to-Bipolar Conversion Range –
From MCMOS operating with specified supply voltage range to TTL or DTL operating with +3.0 V to +6.0 V supply. Conversion with logic output levels $> 6.0\text{ V}$ is permitted if $V_{CC} \leq V_{DD}$.
- Pin for Pin Replacement for CD4009A – MC14009
CD4010A – MC14010

McMOS

(LOW-POWER COMPLEMENTARY MOS)

HEX BUFFERS

Inverting – MC14009AL/CL/CP
 Noninverting – MC14010AL/CL/CP

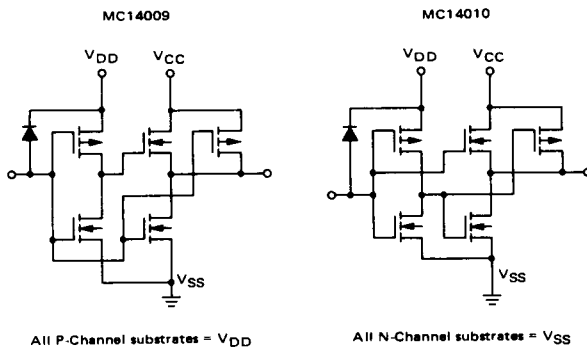


MAXIMUM RATINGS (Voltages referenced to V_{SS} , Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage ($V_{CC} \leq V_{DD}$) –AL Version CL,CP Version	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin*	I	10	mAdc
Operating Temperature Range –AL Version CL,CP Version	T_A	-55 to +125 -40 to +85	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^{\circ}\text{C}$

*Buffered Outputs may supply higher current.

CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)



LOGIC DIAGRAMS

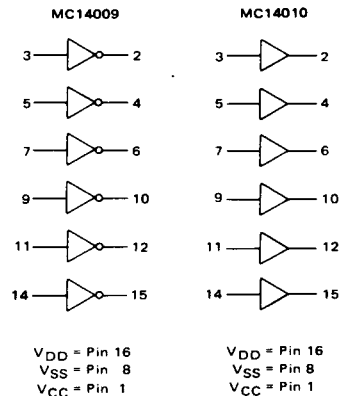


FIGURE 1 – CURRENT AND VOLTAGE TRANSFER CHARACTERISTICS TEST CIRCUIT

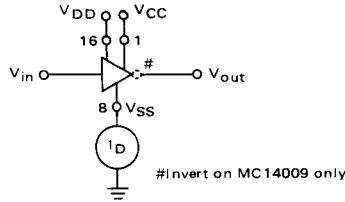


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS versus TEMPERATURE

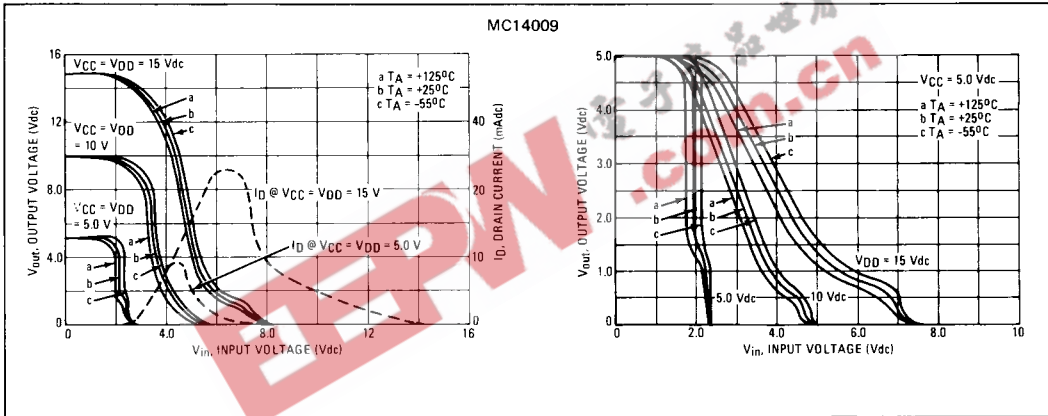


FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

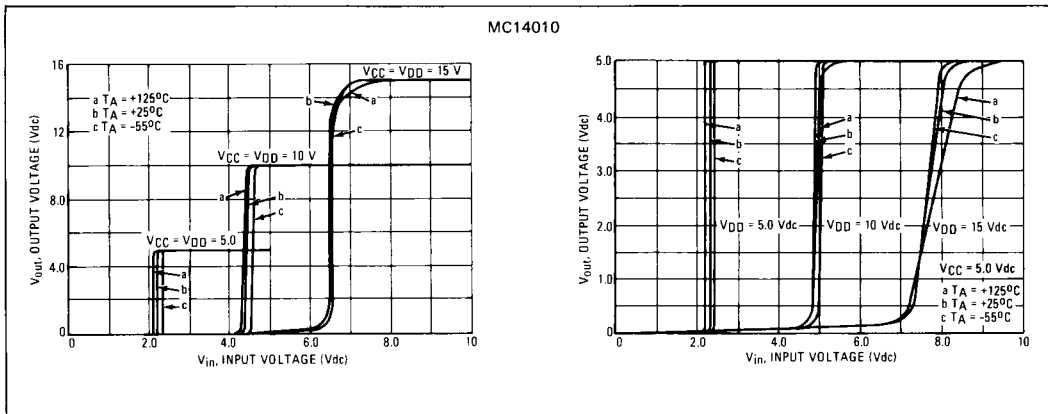


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

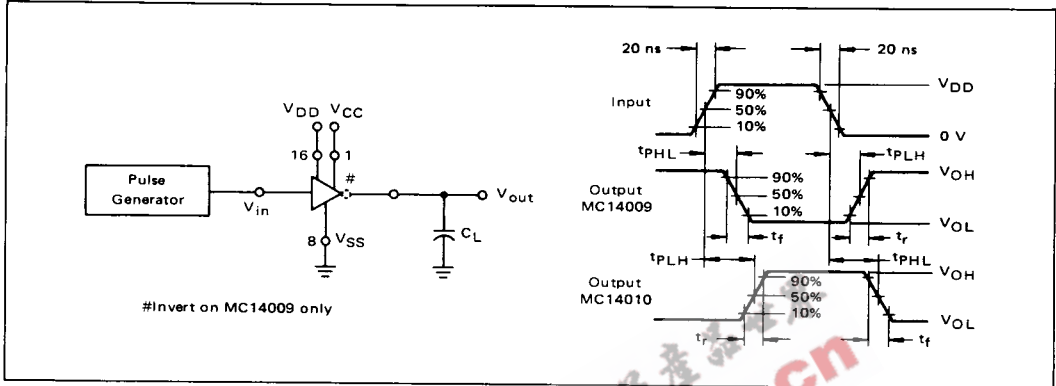


FIGURE 5 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

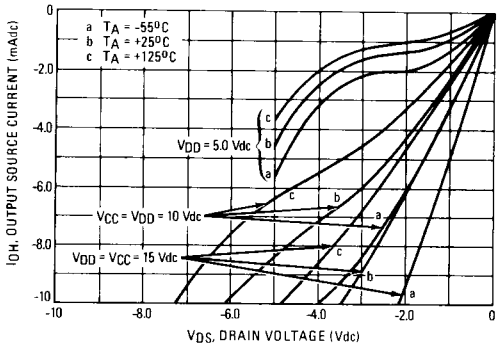
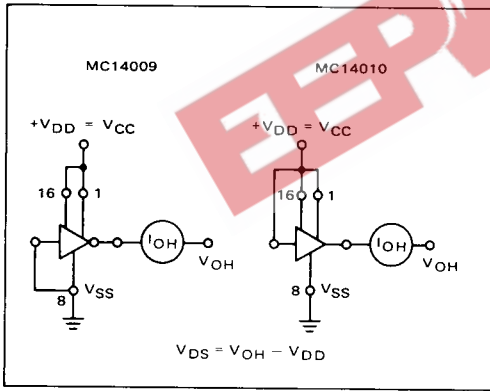


FIGURE 6 – TYPICAL OUTPUT SINK CHARACTERISTICS

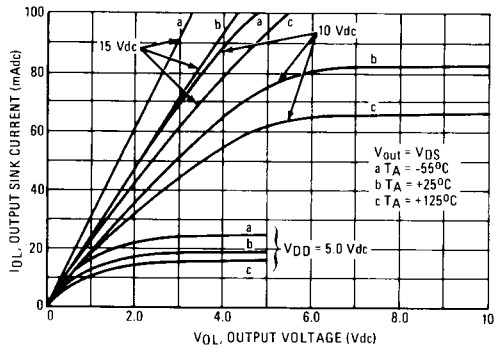
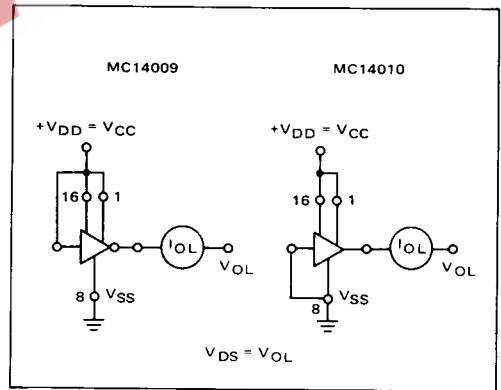
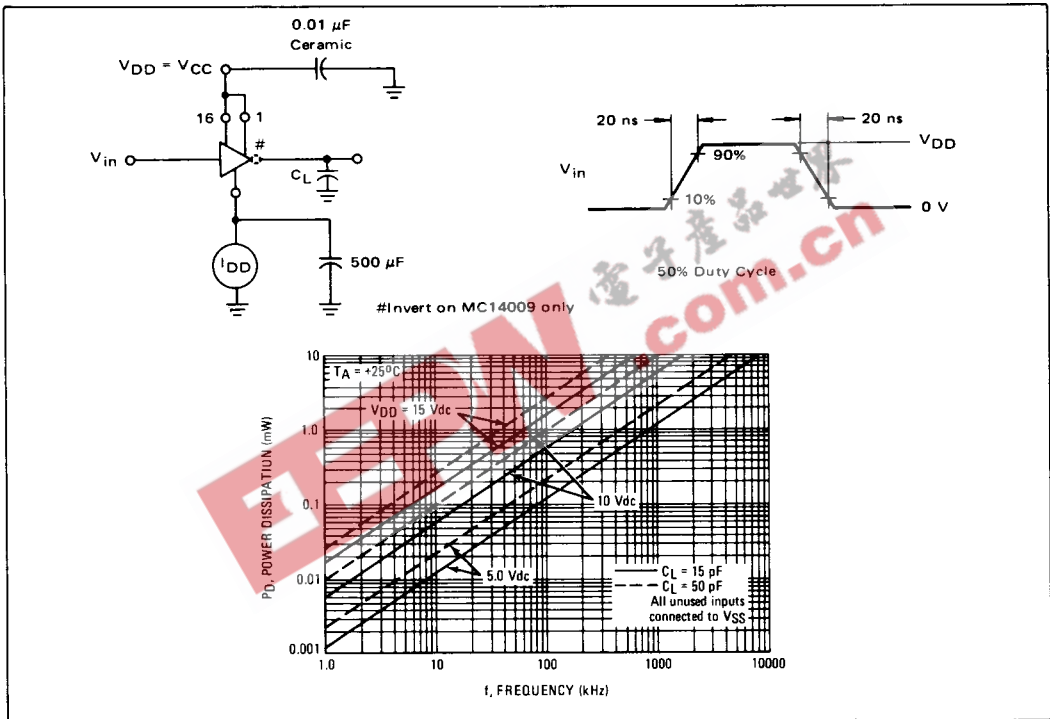


FIGURE 7 – TYPICAL DYNAMIC POWER DISSIPATION CHARACTERISTICS



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).