MC14066B

Quad Analog Switch/Quad Multiplexer

The MC14066B consists of four independent switches capable of controlling either digital or analog signals. This quad bilateral switch is useful in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

The MC14066B is designed to be pin−for−pin compatible with the MC14016B, but has much lower ON resistance. Input voltage swings as large as the full supply voltage can be controlled via each independent control input.

Features

- Triple Diode Protection on All Control Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linearized Transfer Characteristics
- Low Noise − 12 nV/√Cycle, f ≥ 1.0 kHz typical
- Pin−for−Pin Replacement for CD4016, CD4016, MC14016B
- For Lower R_{ON}, Use The HC4066 High−Speed CMOS Device
- Pb−Free Packages are Available

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}	Input Current (DC or Transient) per Control Pin	±10	mA
I_{SW}	Switch Through Current	±25	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating:
   Plastic “P and D/DW” Packages: − 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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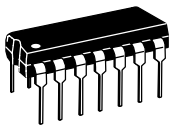
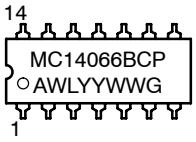
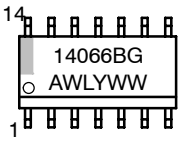
MARKING DIAGRAMS



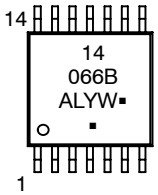
PDIP−14
P SUFFIX
CASE 646

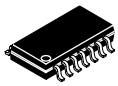


SOIC−14
D SUFFIX
CASE 751A

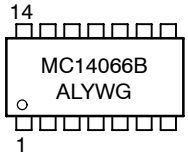


TSSOP−14
DT SUFFIX
CASE 948G





SOEIAJ−14
F SUFFIX
CASE 965

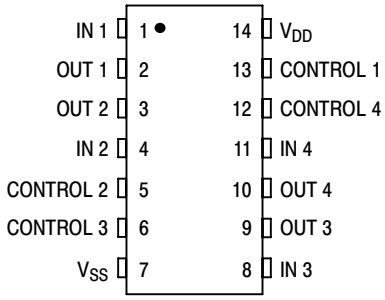


A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package
(Note: Microdot may be in either location)

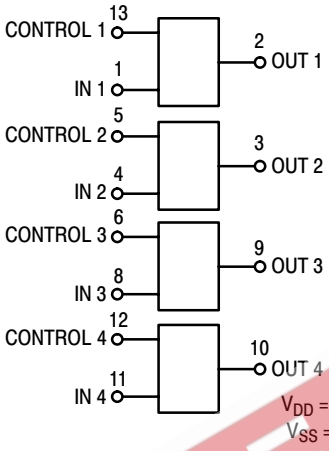
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

PIN ASSIGNMENT

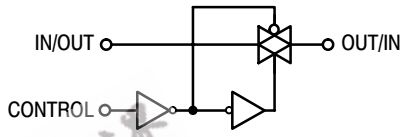


BLOCK DIAGRAM



LOGIC DIAGRAM AND TRUTH TABLE

(1/4 OF DEVICE SHOWN)



Control	Switch
0 = V_{SS}	OFF
1 = V_{DD}	ON

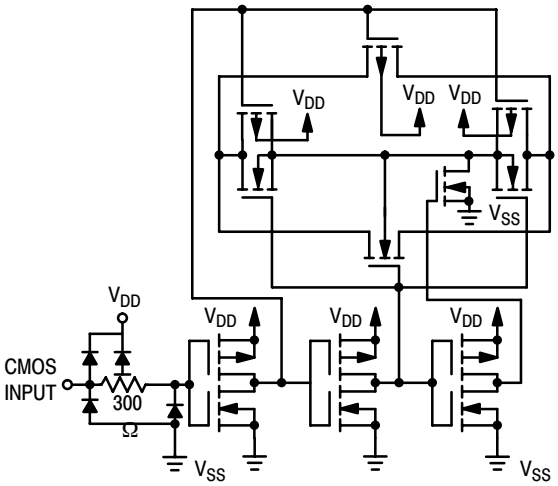
Logic Diagram Restrictions

$V_{SS} \le V_{in} \le V_{DD}$

$V_{SS} \le V_{out} \le V_{DD}$

CIRCUIT SCHEMATIC

(1/4 OF CIRCUIT SHOWN)



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	Test Conditions	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (2)	25°C Max	125°C Min	125°C Max	Unit
SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})											
Power Supply Voltage Range	V_{DD}	—		3.0	18	3.0	–	18	3.0	18	V
Quiescent Current Per Package	I_{DD}	5.0 10 15	Control Inputs: $V_{in} = V_{SS}$ or V_{DD}, Switch I/O: $V_{SS} \le V_{I/O} \le V_{DD}$, and $\Delta V_{switch} \le 500$ mV (3)	– – –	0.25 0.5 1.0	– – –	0.005 0.010 0.015	0.25 0.5 1.0	– – –	7.5 15 30	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package	$I_{D(AV)}$	5.0 10 15	$T_A = 25°C$ only The channel component, $(V_{in} - V_{out})/R_{on}$, is not included.)	Typical			(0.07 μA/kHz) f + I_{DD} (0.20 μA/kHz) f + I_{DD} (0.36 μA/kHz) f + I_{DD}				μA
CONTROL INPUTS (Voltages Referenced to V_{SS})											
Low–Level Input Voltage	V_{IL}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	– – –	1.5 3.0 4.0	– – –	2.25 4.50 6.75	1.5 3.0 4.0	– – –	1.5 3.0 4.0	V
High–Level Input Voltage	V_{IH}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	3.5 7.0 11	– – –	3.5 7.0 11	2.75 5.50 8.25	– – –	3.5 7.0 11	– – –	V
Input Leakage Current	I_{in}	15	V_{in} = 0 or V_{DD}	–	± 0.1	–	±0.00001	± 0.1	–	± 1.0	μA
Input Capacitance	C_{in}	–		–	–	–	5.0	7.5	–	–	pF
SWITCHES IN AND OUT (Voltages Referenced to V_{SS})											
Recommended Peak–to–Peak Voltage Into or Out of the Switch	$V_{I/O}$	–	Channel On or Off	0	V_{DD}	0	–	V_{DD}	0	V_{DD}	V_{p-p}
Recommended Static or Dynamic Voltage Across the Switch (3) (Figure 1)	ΔV_{switch}	–	Channel On	0	600	0	–	600	0	300	mV
Output Offset Voltage	V_{OO}	–	V_{in} = 0 V, No Load	–	–	–	10	–	–	–	μV
ON Resistance	R_{on}	5.0 10 15	$\Delta V_{switch} \le 500$ mV (3), $V_{in} = V_{IL}$ or V_{IH} (Control), and V_{in} = 0 to V_{DD} (Switch)	– – –	800 400 220	– – –	250 120 80	1050 500 280	– – –	1200 520 300	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR_{on}	5.0 10 15		– – –	70 50 45	– – –	25 10 10	70 50 45	– – –	135 95 65	Ω
Off–Channel Leakage Current (Figure 6)	I_{off}	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	–	±100	–	± 0.05	±100	–	±1000	nA
Capacitance, Switch I/O	$C_{I/O}$	–	Switch Off	–	–	–	10	15	–	–	pF
Capacitance, Feedthrough (Switch Off)	$C_{I/O}$	– –		–	–	–	0.47	–	–	–	pF

2. Data labeled “Typ” is not to be used for design purposes, but is intended as an indication of the IC’s potential performance.
3. For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

ELECTRICAL CHARACTERISTICS (Note 4) (C_L = 50 pF, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (5)	Max	Unit
Propagation Delay Times V_{SS} = 0 Vdc	t_{PLH}, t_{PHL}					ns
Input to Output (R_L = 10 kΩ)						
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 15.5 ns		5.0	–	20	40	
t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 6.0 ns		10	–	10	20	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 4.0 ns		15	–	7.0	15	
Control to Output (R_L = 1 kΩ) (Figure 2)	t_{PHZ}					ns
Output “1” to High Impedance		5.0	–	40	80	
		10	–	35	70	
		15	–	30	60	
Output “0” to High Impedance	t_{PLZ}	5.0	–	40	80	ns
		10	–	35	70	
		15	–	30	60	
High Impedance to Output “1”	t_{PZH}	5.0	–	60	120	ns
		10	–	20	40	
		15	–	15	30	
High Impedance to Output “0”	t_{PZL}	5.0	–	60	120	ns
		10	–	20	40	
		15	–	15	30	
Second Harmonic Distortion V_{SS} = – 5 Vdc (V_{in} = 1.77 Vdc, RMS Centered @ 0.0 Vdc, R_L = 10 kΩ, f = 1.0 kHz)	–	5.0	–	0.1	–	%
Bandwidth (Switch ON) (Figure 3) V_{SS} = – 5 Vdc (R_L = 1 kΩ, 20 Log (V_{out}/V_{in}) = – 3 dB, C_L = 50 pF, V_{in} = 5 V_{p-p})	–	5.0	–	65	–	MHz
Feedthrough Attenuation (Switch OFF) V_{SS} = – 5 Vdc (V_{in} = 5 V_{p-p}, R_L = 1 kΩ, f_{in} = 1.0 MHz) (Figure 3)	–	5.0	–	– 50	–	dB
Channel Separation (Figure 4) V_{SS} = – 5 Vdc (V_{in} = 5 V_{p-p}, R_L = 1 kΩ, f_{in} = 8.0 MHz) (Switch A ON, Switch B OFF)	–	5.0	–	– 50	–	dB
Crosstalk, Control Input to Signal Output (Figure 5) V_{SS} = – 5 Vdc (R_1 = 1 kΩ, R_L = 10 kΩ, Control t_{TLH} = t_{THL} = 20 ns)	–	5.0	–	300	–	mV_{p-p}

4. The formulas given are for the typical characteristics only at 25°C.
5. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

ORDERING INFORMATION

Device	Package	Shipping†
MC14066BCP	PDIP−14	25 Units / Rail
MC14066BCPG	PDIP−14 (Pb−Free)	
MC14066BD	SOIC−14	55 Units / Rail
MC14066BDG	SOIC−14 (Pb−Free)	
MC14066BDR2	SOIC−14	2500 / Tape & Reel
MC14066BDR2G	SOIC−14 (Pb−Free)	
MC14066BDTR2	TSSOP−14*	
MC14066BDTR2G	TSSOP−14*	
MC14066BF	SOEIAJ−14	50 Units / Rail
MC14066BFG	SOEIAJ−14 (Pb−Free)	
MC14066BFEL	SOEIAJ−14	2000 / Tape & Reel
MC14066BFELG	SOEIAJ−14 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

TEST CIRCUITS

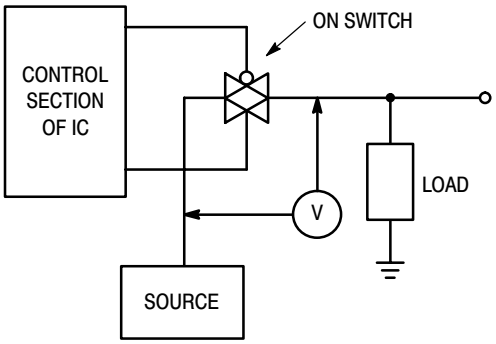


Figure 1. ΔV Across Switch

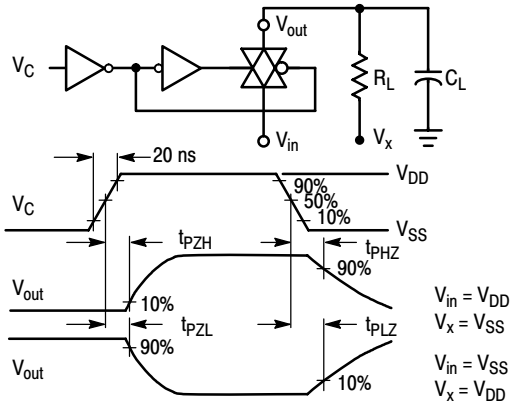


Figure 2. Turn−On Delay Time Test Circuit and Waveforms

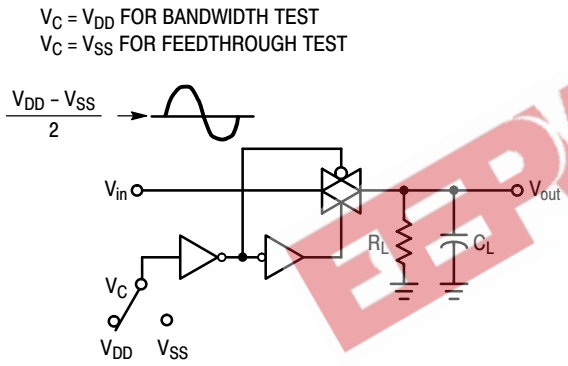


Figure 3. Bandwidth and Feedthrough Attenuation

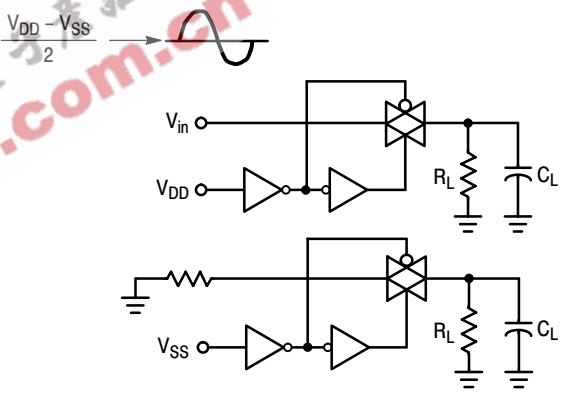


Figure 4. Channel Separation

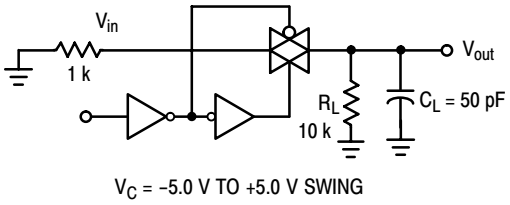


Figure 5. Crosstalk, Control to Output

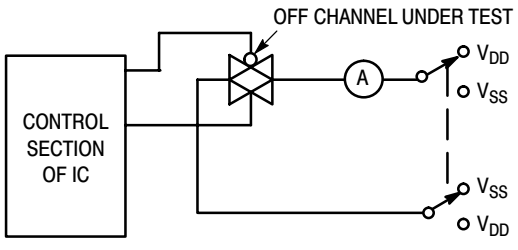


Figure 6. Off Channel Leakage

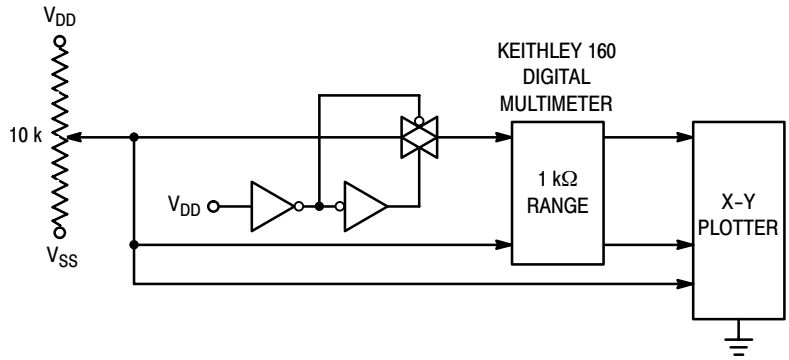


Figure 7. Channel Resistance (R_{ON}) Test Circuit

TYPICAL RESISTANCE CHARACTERISTICS

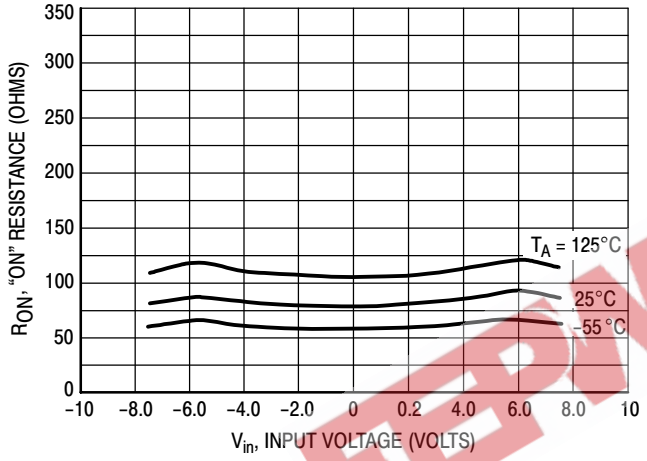


Figure 8. V_{DD} = 7.5 V, V_{SS} = – 7.5 V

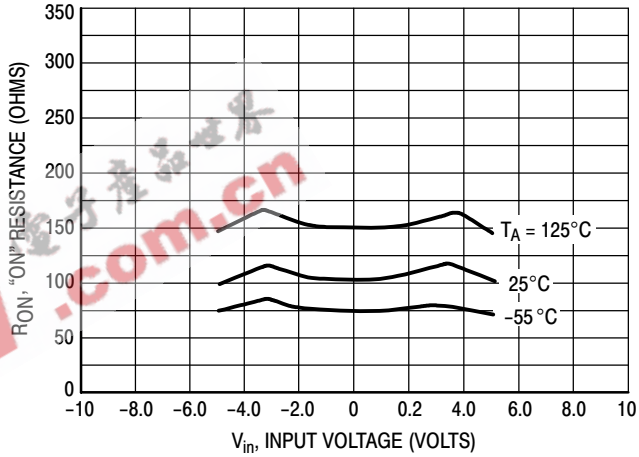


Figure 9. V_{DD} = 5.0 V, V_{SS} = – 5.0 V

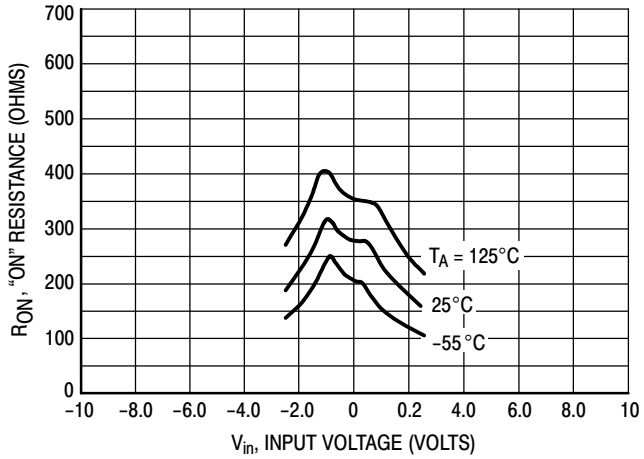


Figure 10. V_{DD} = 2.5 V, V_{SS} = – 2.5 V

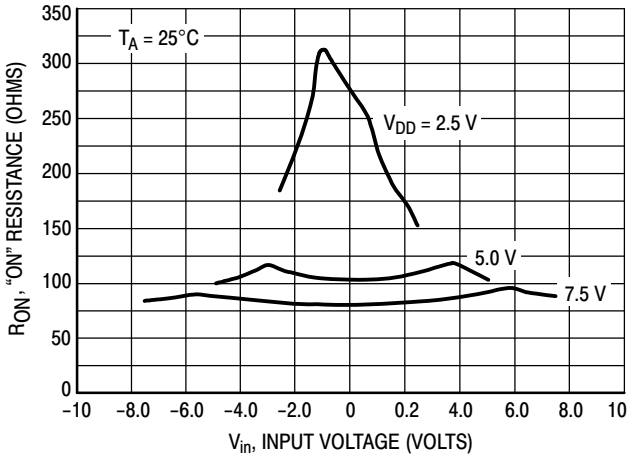


Figure 11. Comparison at 25°C, V_{DD} = –V_{SS}

APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Switch. The 0−to−5 V digital control signal is used to directly control a 5 V peak−to−peak analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage, the V_{SS} voltage is logic low. For the example, V_{DD} = + 5 V = logic high at the control inputs; V_{SS} = GND = 0 V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{SS}. The analog voltage must not swing higher than V_{DD} or lower than V_{SS}.

The example shows a 5 V peak−to−peak signal which allows no margin at either peak. If voltage transients above V_{DD} and/or below V_{SS} are anticipated on the analog channels, external diodes (D_x) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{SS} is 18 V. Most parameters are specified up to 15 V which is the *recommended* maximum difference between V_{DD} and V_{SS}.

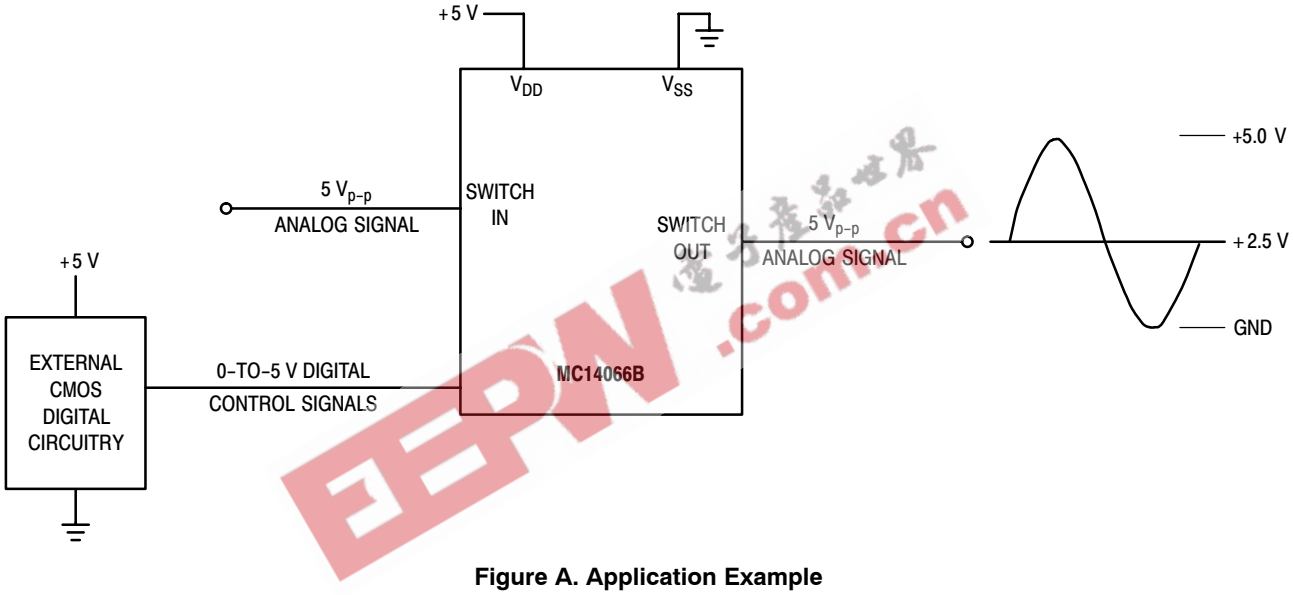


Figure A. Application Example

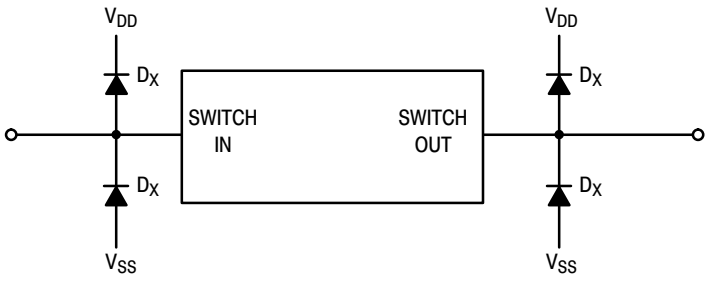
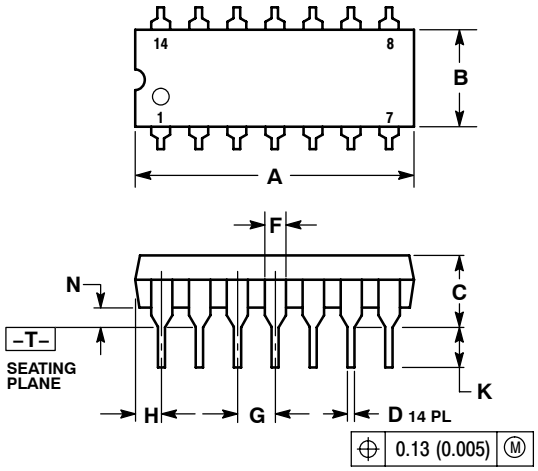


Figure B. External Germanium or Schottky Clipping Diodes

PACKAGE DIMENSIONS

PDIP−14
CASE 646−06
ISSUE P

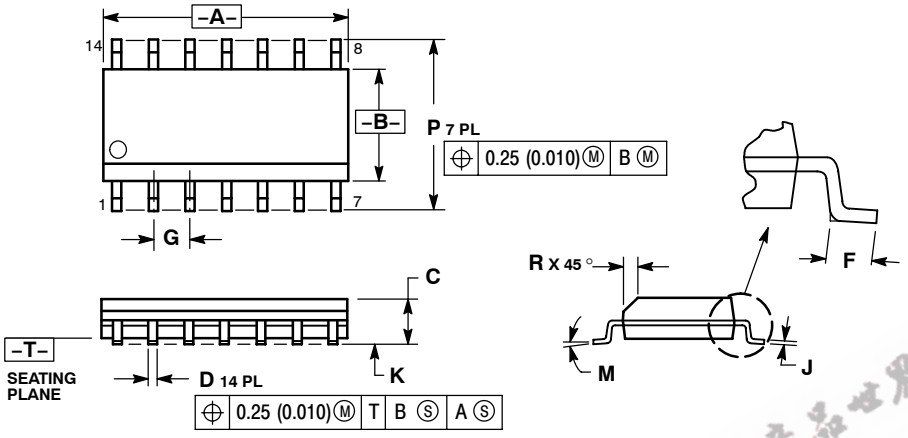


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10 °	---	10 °
N	0.015	0.039	0.38	1.01

PACKAGE DIMENSIONS

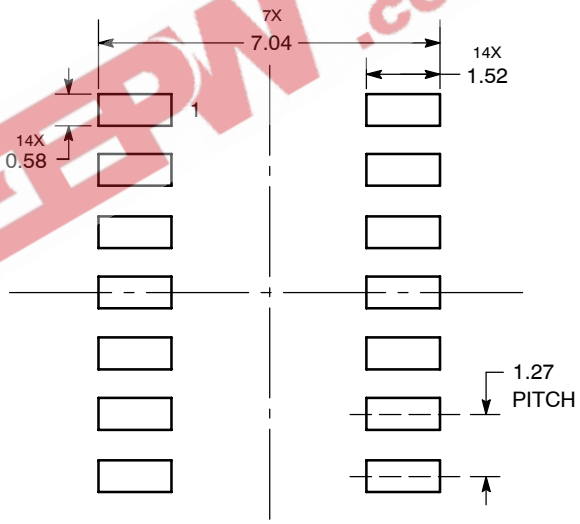
SOIC−14
CASE 751A−03
ISSUE H



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*

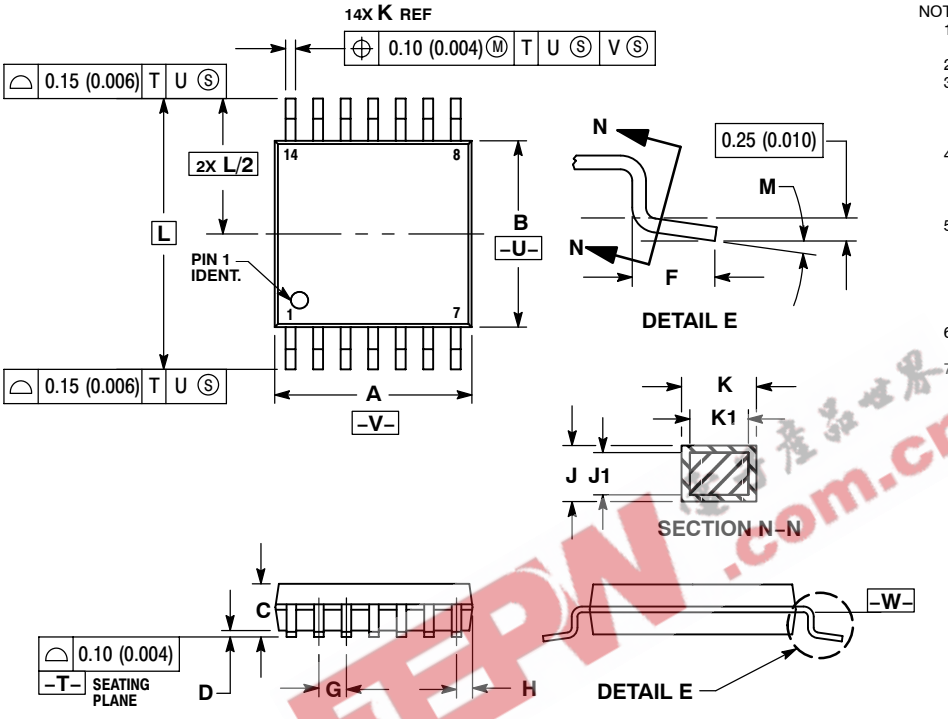


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

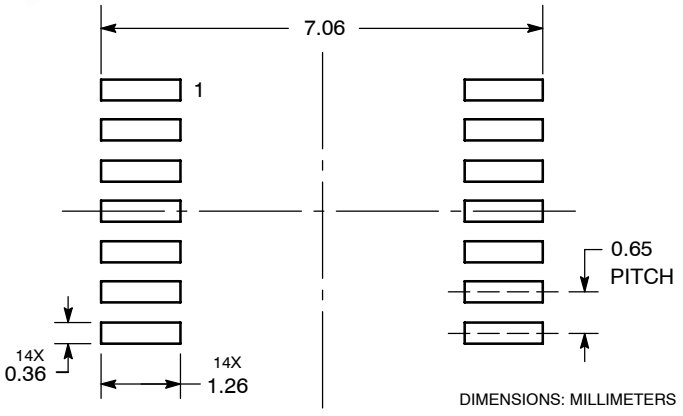
TSSOP−14
CASE 948G−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT*

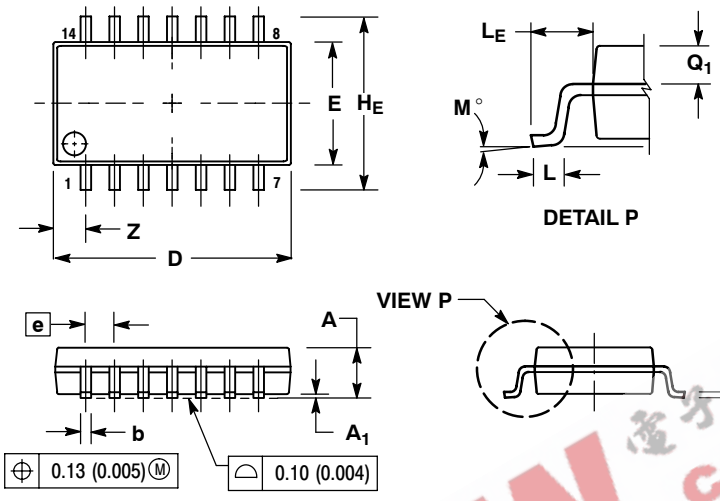


*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC14066B

PACKAGE DIMENSIONS

SOEIAJ−14
CASE 965−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.004	0.008
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

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