

**MC3447**

**BIDIRECTIONAL INSTRUMENTATION  
 BUS (GPIB) TRANSCEIVER**

This bidirectional bus transceiver is intended as the interface between TTL or MOS logic and the IEEE Standard Instrumentation Bus (488-1978, often referred to as GPIB). The required bus termination is internally provided.

Low power consumption has been achieved by trading a minimum of speed for low current drain on non-critical channels. A fast channel is provided for critical ATN and EOI paths.

Each driver/receiver pair forms the complete interface between the bus and an instrument. Either the driver or the receiver of each channel is enabled by a Send/Receive input with the disabled output of the pair forced to a high impedance state. The receivers have input hysteresis to improve noise margin, and their input loading follows the bus standard specifications.

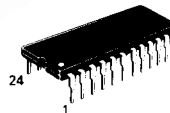
- **Low Power —**  
 Average Power Supply Current = 30 mA Listening  
 75 mA Talking
- **Eight Driver/Receiver Pairs**
- **Three-State Outputs**
- **High Impedance Inputs**
- **Receiver Hysteresis — 600 mV (Typ)**
- **Fast Propagation Times — 15–20 ns (Typ)**
- **TTL Compatible Receiver Outputs**
- **Single +5 Volt Supply**
- **Open Collector Driver Output with Terminations**
- **Power Up/Power Down Protection**  
 (No Invalid Information Transmitted to Bus)
- **No Bus Loading When Power is Removed From Device**
- **Terminations Provided: Termination Removed When Device is Unpowered**

**OCTAL BIDIRECTIONAL  
 BUS TRANSCEIVER  
 WITH  
 TERMINATION NETWORKS**

**SILICON MONOLITHIC  
 INTEGRATED CIRCUIT**

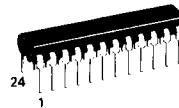


**L SUFFIX  
 CERAMIC PACKAGE  
 CASE 623**

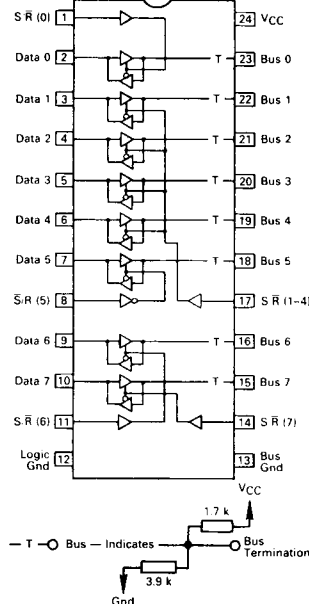


**P SUFFIX  
 PLASTIC PACKAGE  
 CASE 649**

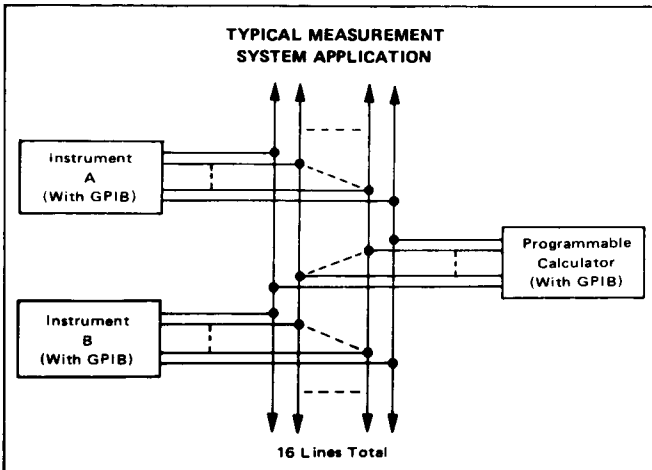
**P3 SUFFIX  
 PLASTIC PACKAGE  
 CASE 724**



**PIN CONNECTIONS**



**TYPICAL MEASUREMENT  
 SYSTEM APPLICATION**



## MC3447

### MAXIMUM RATINGS (T<sub>A</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V <sub>CC</sub>	7.0	Vdc
Input Voltage	V <sub>I</sub>	5.5	Vdc
Driver Output Current	I <sub>O(D)</sub>	150	mA
Junction Temperature	T <sub>J</sub>	150	°C
Operating Ambient Temperature Range	T <sub>A</sub>	0 to +70	°C
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C

### ELECTRICAL CHARACTERISTICS

(Unless otherwise noted 4.50 V ≤ V<sub>CC</sub> ≤ 5.50 V and 0 ≤ T<sub>A</sub> ≤ 70°C; typical values are at T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Characteristic — Note 1	Symbol	Min	Typ	Max	Unit
Bus Voltage (Bus Pin Open) (V <sub>I(S/R)</sub> = 0.8 V) (I <sub>(Bus)</sub> = -12 mA)	V <sub>(Bus)</sub> V <sub>IC(Bus)</sub>	2.5 —	— —	3.7 -1.5	V
Bus Current (5.0 V ≤ V <sub>(Bus)</sub> ≤ 5.5 V) (V <sub>(Bus)</sub> = 0.5 V) (V <sub>CC</sub> = 0 V, 0 V ≤ V <sub>(Bus)</sub> ≤ 2.75 V)	I <sub>(Bus)</sub>	0.7 -1.3 —	— — —	2.5 -3.2 +0.04	mA
Receiver Input Hysteresis (V <sub>I(S/R)</sub> = 0.8 V)	—	400	600	—	mV
Receiver Input Threshold (V <sub>I(S/R)</sub> = 0.8 V)	—	—	—	—	V
Receiver Output Voltage — High Logic State (V <sub>I(S/R)</sub> = 0.8 V, I <sub>OH(R)</sub> = -200 μA, V <sub>(Bus)</sub> = 2.0 V)	V <sub>OH(R)</sub>	—	1.6	2.0	V
Receiver Output Voltage — Low Logic State (V <sub>I(S/R)</sub> = 0.8 V, I <sub>OL(R)</sub> = 4.0 mA, V <sub>(Bus)</sub> = 0.8 V)	V <sub>OL(R)</sub>	—	1.0	—	V
Receiver Output Short Circuit Current (V <sub>I(S/R)</sub> = 0.8 V, V <sub>(Bus)</sub> = 2.0 V)	I <sub>OS(R)</sub>	2.4	—	—	mA
Driver Input Voltage — High Logic State (V <sub>I(S/R)</sub> = 2.0 V)	V <sub>IH(D)</sub>	—	—	0.5	V
Driver Input Voltage — Low Logic State (V <sub>I(S/R)</sub> = 2.0 V)	V <sub>IL(D)</sub>	—	—	-20	mA
Driver Input Current — Data Pins (V <sub>I(S/R)</sub> = 2.0 V) (0.5 ≤ V <sub>I(D)</sub> ≤ 2.7 V) (V <sub>I(D)</sub> = 5.5 V)	I <sub>I(D)</sub> I <sub>IB(D)</sub>	-100 —	— —	40 200	μA
Input Current — Send/Receive (0.5 ≤ V <sub>I(S/R)</sub> ≤ 2.7 V) (V <sub>I(S/R)</sub> = 5.5 V)	I <sub>IS/R</sub> I <sub>IB(S/R)</sub>	-250 —	— —	20 100	μA
Driver Input Clamp Voltage (V <sub>I(S/R)</sub> = 2.0 V, I <sub>IC(D)</sub> = -18 mA)	V <sub>IC(D)</sub>	—	—	-1.5	V
Driver Output Voltage — High Logic State (V <sub>I(S/R)</sub> = 2.0 V, V <sub>IH(D)</sub> = 2.0 V)	V <sub>OH(D)</sub>	2.5	—	—	V
Driver Output Voltage — Low Logic State (Note 2) (V <sub>I(S/R)</sub> = 2.0 V, V <sub>IL(D)</sub> = 0.8 V, I <sub>OL(D)</sub> = 48 mA)	V <sub>OL(D)</sub>	—	—	0.5	V
Power Supply Current (Listening Mode — All Receivers On) (Talking Mode — All Drivers On)	I <sub>CCL</sub> I <sub>CCH</sub>	— —	30 75	45 95	mA

### SWITCHING CHARACTERISTICS (V<sub>CC</sub> = 5.0 V, T<sub>A</sub> = 25°C unless otherwise noted)

Propagation Delay of Driver (Output Low to High) (Output High to Low)	t <sub>PLH(D)</sub> t <sub>PHL(D)</sub>	— —	7.0 16	15 30	ns
Propagation Delay of Receiver (Channels 0 to 5, 7) (Output Low to High) (Output High to Low)	t <sub>PLH(R)</sub> t <sub>PHL(R)</sub>	— —	28 15	50 30	ns
Propagation Delay of Receiver (Channel 6, Note 3) (Output Low to High) (Output High to Low)	t <sub>PLH(R)</sub> t <sub>PHL(R)</sub>	— —	17 12	30 22	ns

- NOTES: 1. Specified test conditions for V<sub>I(S/R)</sub> are 0.8 V (Low) and 2.0 V (High). Where V<sub>I(S/R)</sub> is specified as a test condition, V<sub>I(S/R)</sub> uses the opposite logic levels.  
 2. The IEEE 488-1979 Bus Standard changes V<sub>OL(D)</sub> from 0.4 to 0.5 V maximum to permit the use of Schottky technology.  
 3. In order to meet the IEEE 488-1978 Standard for total system delay on the ATN and EOI channels, a fast receiver has been provided on Channel 6 (Pins 9 and 16).

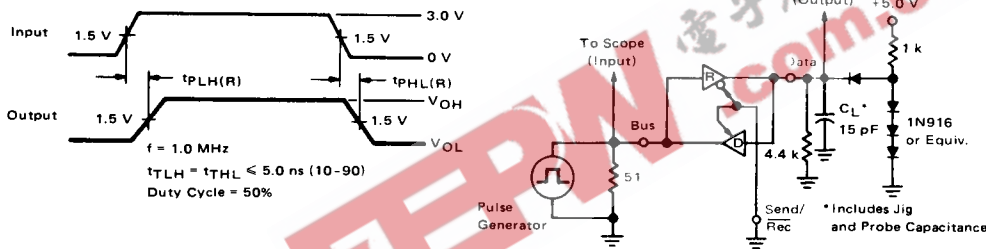
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**SWITCHING CHARACTERISTICS (continued)** ( $V_{CC} = 5.0\text{ V}$ ,  $T_A = 25^\circ\text{C}$  unless otherwise noted)

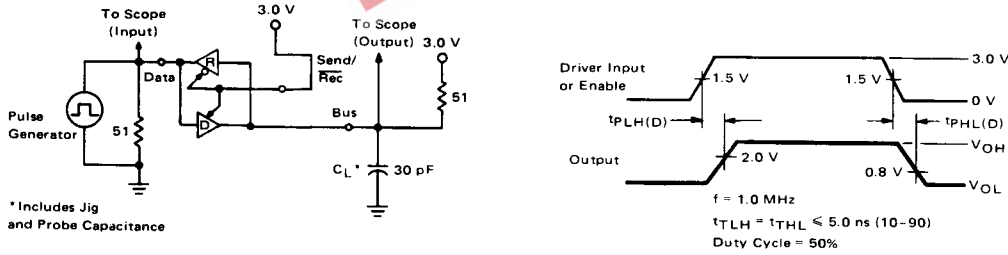
Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time – Send/Receiver to Data					ns
Logic High to Third State	$t_{PHZ}(R)$	–	15	30	
Third State to Logic High	$t_{PZH}(R)$	–	15	30	
Logic Low to Third State	$t_{PLZ}(R)$	–	15	25	
Third State to Logic Low	$t_{PZL}(R)$	–	10	25	
Propagation Delay Time – Send/Receiver to Bus					ns
Logic Low to Third State	$t_{PLZ}(D)$	–	13	25	
Third State to Logic Low	$t_{PZL}(D)$	–	30	50	

## PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS

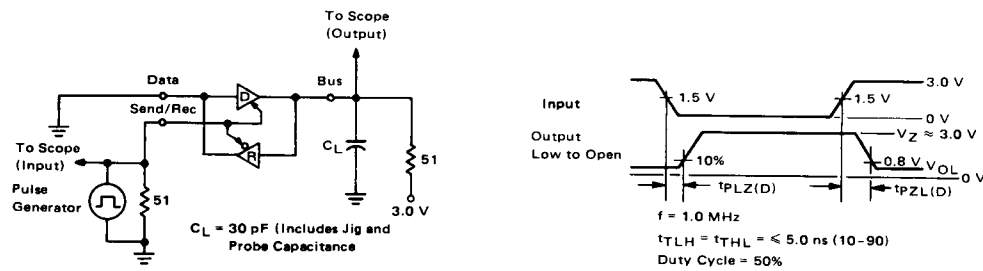
**FIGURE 1 – BUS INPUT TO DATA OUTPUT (RECEIVER)**



**FIGURE 2 – DATA INPUT TO BUS OUTPUT (DRIVER)**



**FIGURE 3 – SEND/RECEIVE INPUT TO BUS OUTPUT (DRIVER)**



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FIGURE 4 - SEND/RECEIVE INPUT TO DATA OUTPUT (RECEIVER)

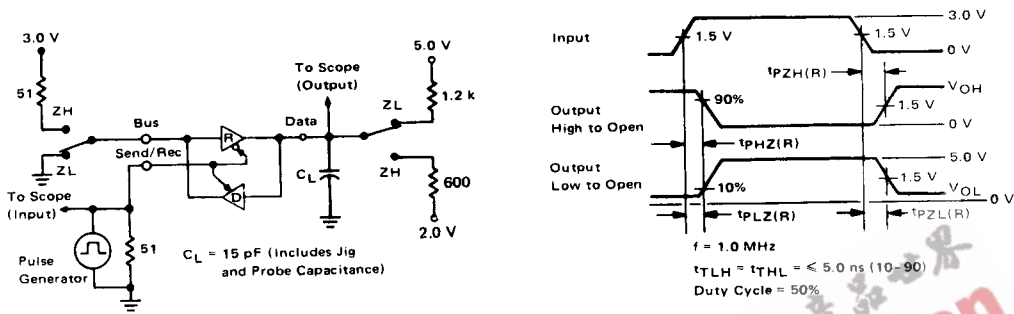


FIGURE 5 - TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

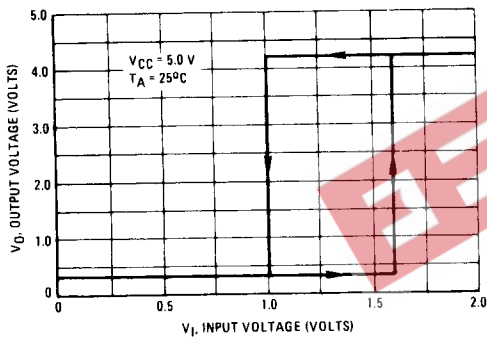


FIGURE 6 - TYPICAL BUS LOAD LINE

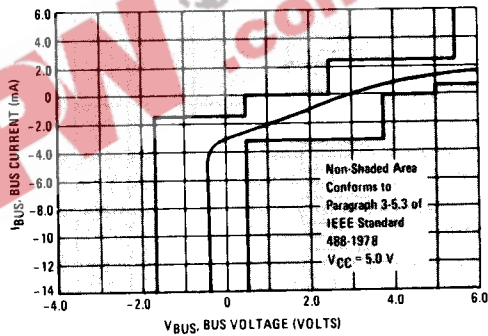
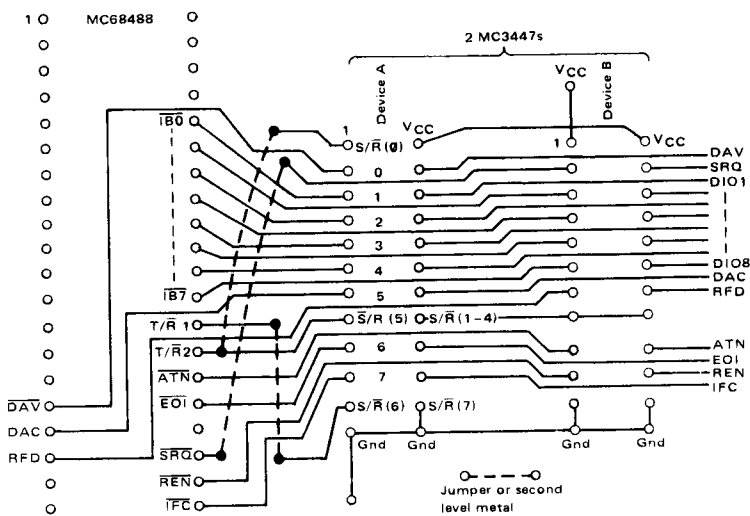
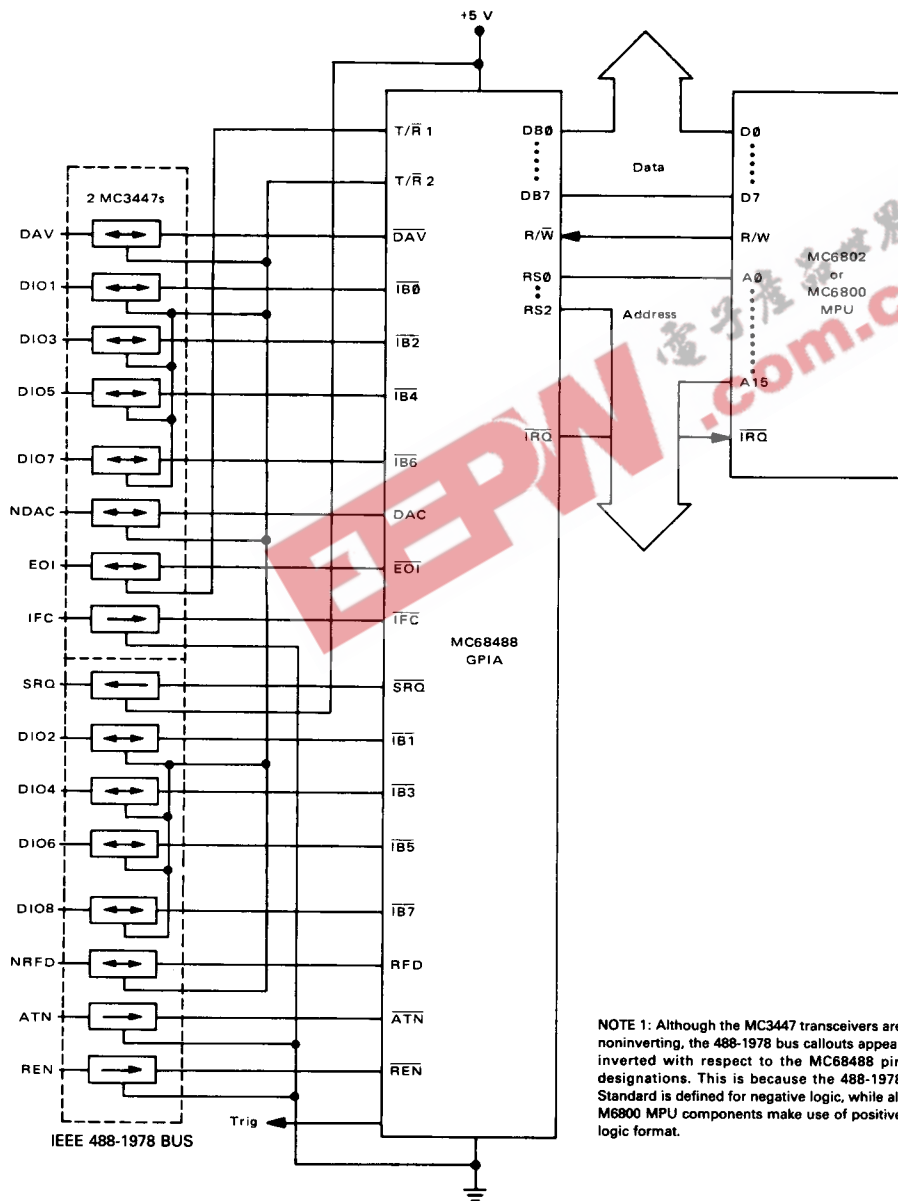


FIGURE 7 - SUGGESTED PRINTED CIRCUIT BOARD LAYOUT USING MC3447s AND MC68488



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FIGURE 8 - SIMPLE SYSTEM CONFIGURATION



NOTE 1: Although the MC3447 transceivers are noninverting, the 488-1978 bus callouts appear inverted with respect to the MC68488 pin designations. This is because the 488-1978 Standard is defined for negative logic, while all M6800 MPU components make use of positive logic format.

## MC3447

**FIGURE 9 – SUGGESTED PIN DESIGNATIONS FOR USE WITH MC68488**

MC68488 Connections		MC3447 Pin Designations						MC68488 Connections	
A	B							A	B
T/R 2	V <sub>CC</sub>	S/R (0)	1	24	V <sub>CC</sub>		V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>
DAV	SRQ	Data 0 0	2	23	Bus 0		DAV	DAV	SRQ
IB0	IB1	Data 1	3	22	Bus 1		DIO 1	DIO 2	
IB2	IB3	Data 2	4	21	Bus 2		DIO 3	DIO 4	
IB4	IB5	Data 3	5	20	Bus 3		DIO 5	DIO 6	
IB6	IB7	Data 4	6	19	Bus 4	Octal GPB	DIO 7	DIO 8	
DAC	RFD	Data 5	7	18	Bus 5	Transceiver	NDAC	NRFD	
T/R 2	T/R 2	S/R (5)	8	17	S/R (1-4)		T/R 2	T/R 2	
EOI	ATN	Data 6	9	16	Bus 6		EOI	ATN	
IFC	REN	Data 7	10	15	Bus 7		IFC	REN	
T/R 1	Gnd	S/R (6)	11	14	S/R (7)		Gnd	Gnd	
Gnd	Gnd	Logic Gnd	12	13	Bus Gnd		Gnd	Gnd	

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