

# MC34071,2,4,A MC33071,2,4,A

## High Slew Rate, Wide Bandwidth, Single Supply Operational Amplifiers

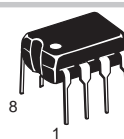
Quality bipolar fabrication with innovative design concepts are employed for the MC33071/72/74, MC34071/72/74 series of monolithic operational amplifiers. This series of operational amplifiers offer 4.5 MHz of gain bandwidth product, 13 V/ $\mu$ s slew rate and fast settling time without the use of JFET device technology. Although this series can be operated from split supplies, it is particularly suited for single supply operation, since the common mode input voltage range includes ground potential ( $V_{EE}$ ). With A Darlington input stage, this series exhibits high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source/sink AC frequency response.

The MC33071/72/74, MC34071/72/74 series of devices are available in standard or prime performance (A Suffix) grades and are specified over the commercial, industrial/vehicular or military temperature ranges. The complete series of single, dual and quad operational amplifiers are available in plastic DIP, SOIC and TSSOP surface mount packages.

- Wide Bandwidth: 4.5 MHz
- High Slew Rate: 13 V/ $\mu$ s
- Fast Settling Time: 1.1  $\mu$ s to 0.1%
- Wide Single Supply Operation: 3.0 V to 44 V
- Wide Input Common Mode Voltage Range: Includes Ground ( $V_{EE}$ )
- Low Input Offset Voltage: 3.0 mV Maximum (A Suffix)
- Large Output Voltage Swing: -14.7 V to +14 V (with  $\pm 15$  V Supplies)
- Large Capacitance Drive Capability: 0 pF to 10,000 pF
- Low Total Harmonic Distortion: 0.02%
- Excellent Phase Margin: 60°
- Excellent Gain Margin: 12 dB
- Output Short Circuit Protection
- ESD Diodes/Clamps Provide Input Protection for Dual and Quad



**ON Semiconductor**  
Formerly a Division of Motorola  
<http://onsemi.com>

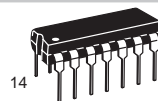
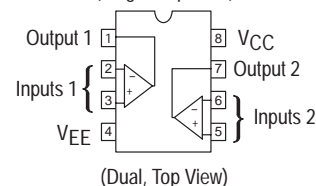
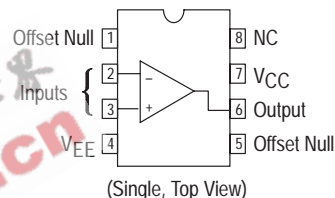


**P SUFFIX  
CASE 626**



**SO-8  
D SUFFIX  
CASE 751**

### PIN CONNECTIONS



**P SUFFIX  
CASE 646**

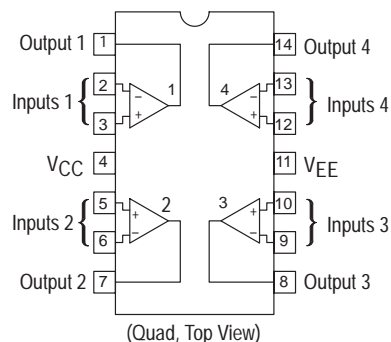


**SO-14  
D SUFFIX  
CASE 751A**



**TSSOP-14  
DTB SUFFIX  
CASE 948G**

### PIN CONNECTIONS

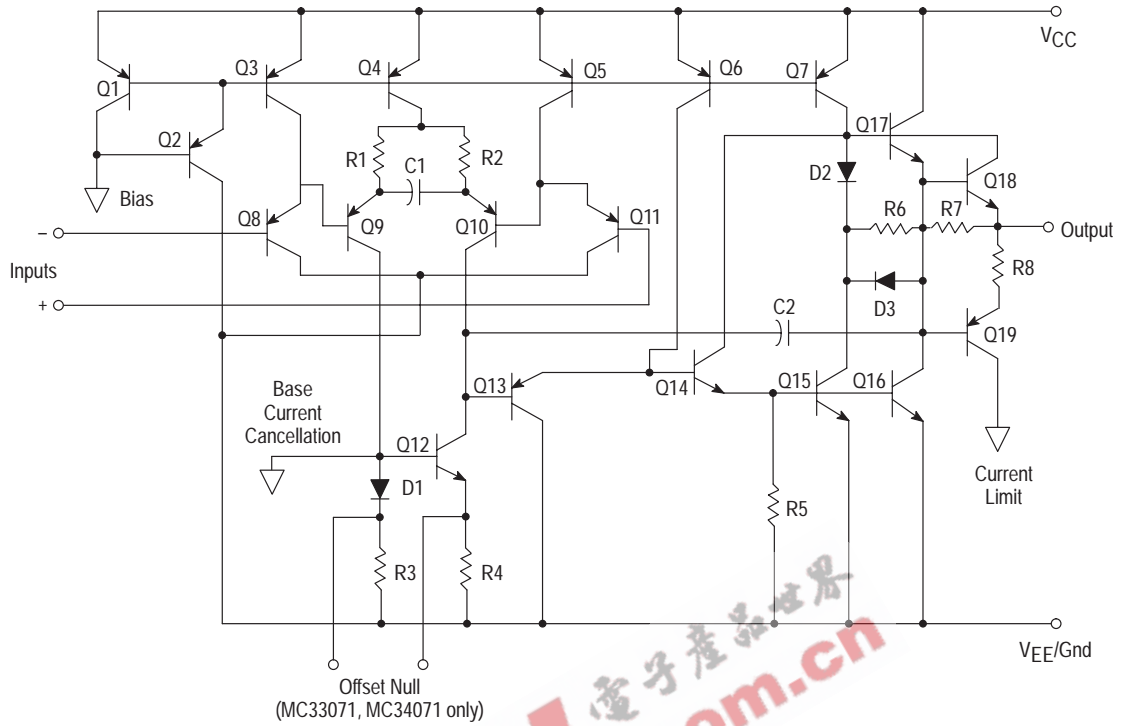


### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 17 of this data sheet.

# MC34071,2,4,A MC33071,2,4,A

Representative Schematic Diagram  
(Each Amplifier)



## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from $V_{EE}$ to $V_{CC}$ )	$V_S$	+44	V
Input Differential Voltage Range	$V_{IDR}$	Note 1	V
Input Voltage Range	$V_{IR}$	Note 1	V
Output Short Circuit Duration (Note 2)	$t_{SC}$	Indefinite	sec
Operating Junction Temperature	$T_J$	+150	$^{\circ}\text{C}$
Storage Temperature Range	$T_{stg}$	-60 to +150	$^{\circ}\text{C}$

**NOTES:** 1. Either or both input voltages should not exceed the magnitude of  $V_{CC}$  or  $V_{EE}$ .  
2. Power dissipation must be considered to ensure maximum junction temperature ( $T_J$ ) is not exceeded (see Figure 1).

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**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = +15\text{ V}$ ,  $V_{EE} = -15\text{ V}$ ,  $R_L$  = connected to ground, unless otherwise noted. See Note 3 for  $T_A = T_{low}$  to  $T_{high}$ )

Characteristics	Symbol	A Suffix			Non-Suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ( $R_S = 100\ \Omega$ , $V_{CM} = 0\text{ V}$ , $V_O = 0\text{ V}$ ) $V_{CC} = +15\text{ V}$ , $V_{EE} = -15\text{ V}$ , $T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ , $V_{EE} = 0\text{ V}$ , $T_A = +25^\circ\text{C}$ $V_{CC} = +15\text{ V}$ , $V_{EE} = -15\text{ V}$ , $T_A = T_{low}$ to $T_{high}$	$V_{IO}$	— — —	0.5 0.5 —	3.0 3.0 5.0	— — —	1.0 1.5 —	5.0 5.0 7.0	mV
Average Temperature Coefficient of Input Offset Voltage $R_S = 10\ \Omega$ , $V_{CM} = 0\text{ V}$ , $V_O = 0\text{ V}$ , $T_A = T_{low}$ to $T_{high}$	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	$\mu\text{V}/^\circ\text{C}$
Input Bias Current ( $V_{CM} = 0\text{ V}$ , $V_O = 0\text{ V}$ ) $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to $T_{high}$	$I_{IB}$	— —	100 —	500 700	— —	100 —	500 700	nA
Input Offset Current ( $V_{CM} = 0\text{ V}$ , $V_O = 0\text{ V}$ ) $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to $T_{high}$	$I_{IO}$	— —	6.0 —	50 300	— —	6.0 —	75 300	nA
Input Common Mode Voltage Range $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to $T_{high}$	$V_{ICR}$	$V_{EE}$ to $(V_{CC} - 1.8)$ $V_{EE}$ to $(V_{CC} - 2.2)$			$V_{EE}$ to $(V_{CC} - 1.8)$ $V_{EE}$ to $(V_{CC} - 2.2)$			V
Large Signal Voltage Gain ( $V_O = \pm 10\text{ V}$ , $R_L = 2.0\text{ k}\Omega$ ) $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to $T_{high}$	$A_{VOL}$	50 25	100 —	— —	25 20	100 —	— —	V/mV
Output Voltage Swing ( $V_{ID} = \pm 1.0\text{ V}$ ) $V_{CC} = +5.0\text{ V}$ , $V_{EE} = 0\text{ V}$ , $R_L = 2.0\text{ k}\Omega$ , $T_A = +25^\circ\text{C}$ $V_{CC} = +15\text{ V}$ , $V_{EE} = -15\text{ V}$ , $R_L = 10\text{ k}\Omega$ , $T_A = +25^\circ\text{C}$ $V_{CC} = +15\text{ V}$ , $V_{EE} = -15\text{ V}$ , $R_L = 2.0\text{ k}\Omega$ , $T_A = T_{low}$ to $T_{high}$	$V_{OH}$	3.7 13.6 13.4	4.0 14 —	— — —	3.7 13.6 13.4	4.0 14 —	— — —	V
$V_{CC} = +5.0\text{ V}$ , $V_{EE} = 0\text{ V}$ , $R_L = 2.0\text{ k}\Omega$ , $T_A = +25^\circ\text{C}$ $V_{CC} = +15\text{ V}$ , $V_{EE} = -15\text{ V}$ , $R_L = 10\text{ k}\Omega$ , $T_A = +25^\circ\text{C}$ $V_{CC} = +15\text{ V}$ , $V_{EE} = -15\text{ V}$ , $R_L = 2.0\text{ k}\Omega$ , $T_A = T_{low}$ to $T_{high}$	$V_{OL}$	— — —	0.1 -14.7 —	0.3 -14.3 -13.5	— — —	0.1 -14.7 —	0.3 -14.3 -13.5	V
Output Short Circuit Current ( $V_{ID} = 1.0\text{ V}$ , $V_O = 0\text{ V}$ , $T_A = 25^\circ\text{C}$ ) Source Sink	$I_{SC}$	10 20	30 30	— —	10 20	30 30	— —	mA
Common Mode Rejection $R_S \leq 10\text{ k}\Omega$ , $V_{CM} = V_{ICR}$ , $T_A = 25^\circ\text{C}$	CMR	80	97	—	70	97	—	dB
Power Supply Rejection ( $R_S = 100\ \Omega$ ) $V_{CC}/V_{EE} = +16.5\text{ V}/-16.5\text{ V}$ to $+13.5\text{ V}/-13.5\text{ V}$ , $T_A = 25^\circ\text{C}$	PSR	80	97	—	70	97	—	dB
Power Supply Current (Per Amplifier, No Load) $V_{CC} = +5.0\text{ V}$ , $V_{EE} = 0\text{ V}$ , $V_O = +2.5\text{ V}$ , $T_A = +25^\circ\text{C}$ $V_{CC} = +15\text{ V}$ , $V_{EE} = -15\text{ V}$ , $V_O = 0\text{ V}$ , $T_A = +25^\circ\text{C}$ $V_{CC} = +15\text{ V}$ , $V_{EE} = -15\text{ V}$ , $V_O = 0\text{ V}$ , $T_A = T_{low}$ to $T_{high}$	$I_D$	— — —	1.6 1.9 —	2.0 2.5 2.8	— — —	1.6 1.9 —	2.0 2.5 2.8	mA

NOTES: 3.  $T_{low} = -40^\circ\text{C}$  for MC33071, 2, 4, /A  
=  $0^\circ\text{C}$  for MC34071, 2, 4, /A

$T_{high} = +85^\circ\text{C}$  for MC33071, 2, 4, /A  
=  $+70^\circ\text{C}$  for MC34071, 2, 4, /A

# MC34071,2,4,A MC33071,2,4,A

**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = +15\text{ V}$ ,  $V_{EE} = -15\text{ V}$ ,  $R_L = \text{connected to ground}$ .  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

Characteristics	Symbol	A Suffix			Non-Suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Slew Rate ( $V_{in} = -10\text{ V to } +10\text{ V}$ , $R_L = 2.0\text{ k}\Omega$ , $C_L = 500\text{ pF}$ ) $A_V = +1.0$ $A_V = -1.0$	SR	8.0 —	10 13	— —	8.0 —	10 13	— —	$\text{V}/\mu\text{s}$
Setting Time (10 V Step, $A_V = -1.0$ ) To 0.1% (+1/2 LSB of 9-Bits) To 0.01% (+1/2 LSB of 12-Bits)	$t_s$	— —	1.1 2.2	— —	— —	1.1 2.2	— —	$\mu\text{s}$
Gain Bandwidth Product ( $f = 100\text{ kHz}$ )	GBW	3.5	4.5	—	3.5	4.5	—	MHz
Power Bandwidth $A_V = +1.0$ , $R_L = 2.0\text{ k}\Omega$ , $V_O = 20\text{ V}_{pp}$ , THD = 5.0%	BW	—	160	—	—	160	—	kHz
Phase margin $R_L = 2.0\text{ k}\Omega$ $R_L = 2.0\text{ k}\Omega$ , $C_L = 300\text{ pF}$	$f_m$	— —	60 40	— —	— —	60 40	— —	Deg
Gain Margin $R_L = 2.0\text{ k}\Omega$ $R_L = 2.0\text{ k}\Omega$ , $C_L = 300\text{ pF}$	$A_m$	— —	12 4.0	— —	— —	12 4.0	— —	dB
Equivalent Input Noise Voltage $R_S = 100\ \Omega$ , $f = 1.0\text{ kHz}$	$e_n$	—	32	—	—	32	—	$\text{nV}/\sqrt{\text{Hz}}$
Equivalent Input Noise Current $f = 1.0\text{ kHz}$	$i_n$	—	0.22	—	—	0.22	—	$\text{pA}/\sqrt{\text{Hz}}$
Differential Input Resistance $V_{CM} = 0\text{ V}$	$R_{in}$	—	150	—	—	150	—	$\text{M}\Omega$
Differential Input Capacitance $V_{CM} = 0\text{ V}$	$C_{in}$	—	2.5	—	—	2.5	—	pF
Total Harmonic Distortion $A_V = +10$ , $R_L = 2.0\text{ k}\Omega$ , $2.0\text{ V}_{pp} \leq V_O \leq 20\text{ V}_{pp}$ , $f = 10\text{ kHz}$	THD	—	0.02	—	—	0.02	—	%
Channel Separation ( $f = 10\text{ kHz}$ )	—	—	120	—	—	120	—	dB
Open Loop Output Impedance ( $f = 1.0\text{ MHz}$ )	$ Z_O $	—	30	—	—	30	—	$\Omega$

Figure 1. Power Supply Configurations

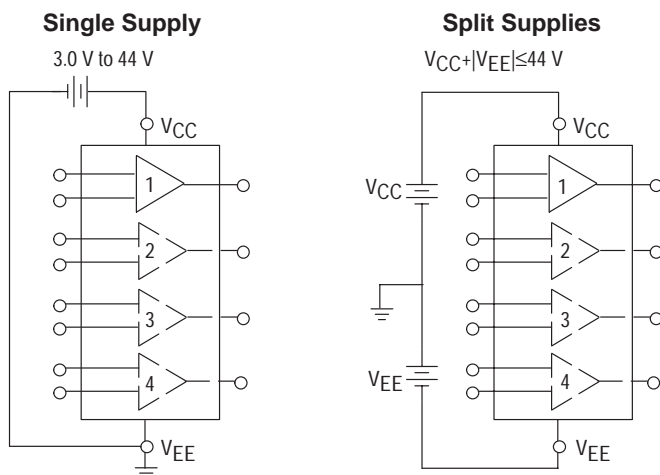
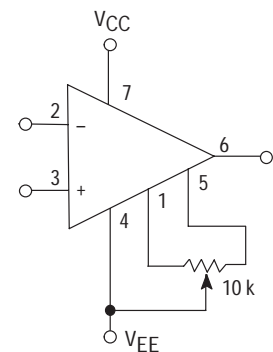


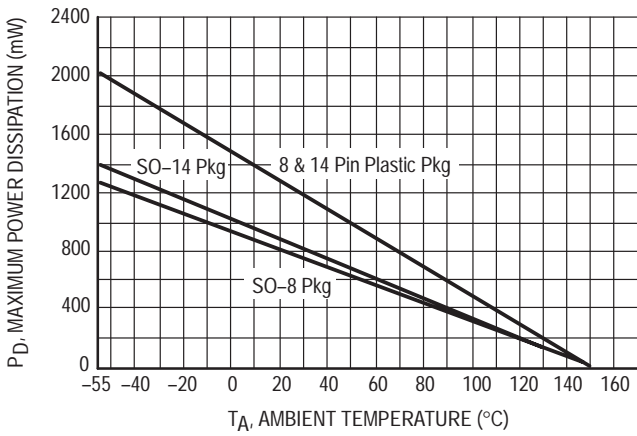
Figure 2. Offset Null Circuit



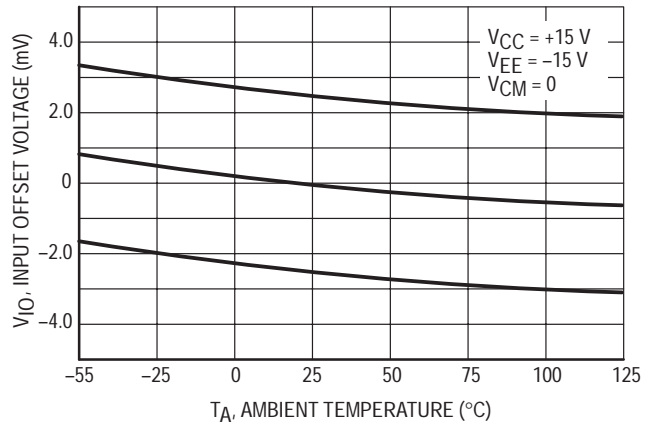
Offset nulling range is approximately  $\pm 80\text{ mV}$  with a 10 k potentiometer (MC33071, MC34071 only).

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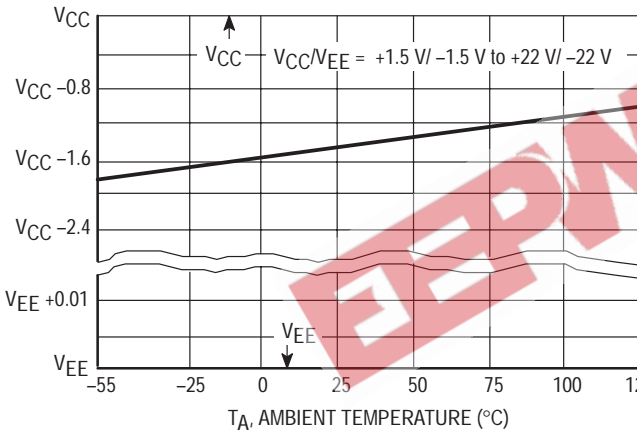
**Figure 3. Maximum Power Dissipation versus Temperature for Package Types**



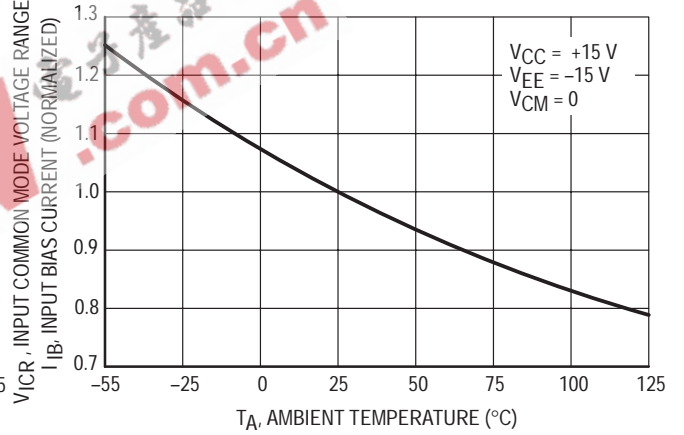
**Figure 4. Input Offset Voltage versus Temperature for Representative Units**



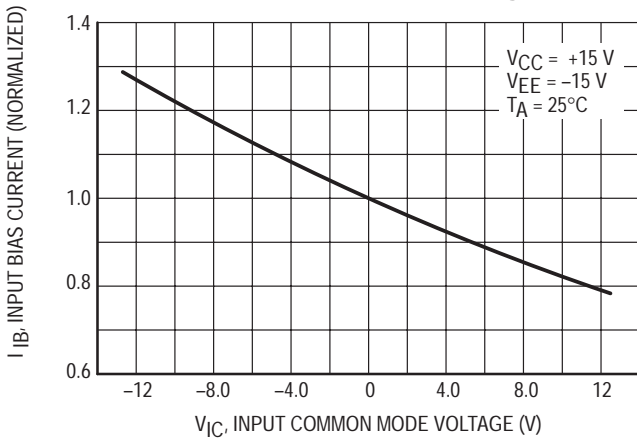
**Figure 5. Input Common Mode Voltage Range versus Temperature**



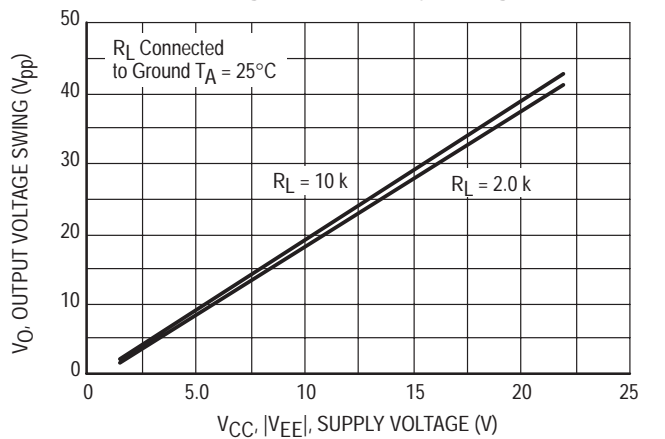
**Figure 6. Normalized Input Bias Current versus Temperature**



**Figure 7. Normalized Input Bias Current versus Input Common Mode Voltage**

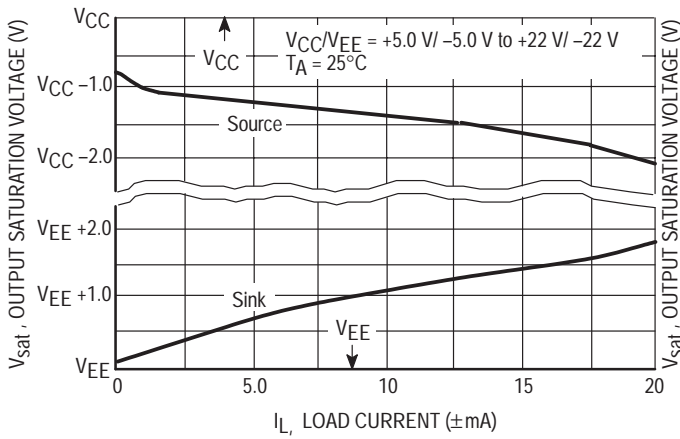


**Figure 8. Split Supply Output Voltage Swing versus Supply Voltage**

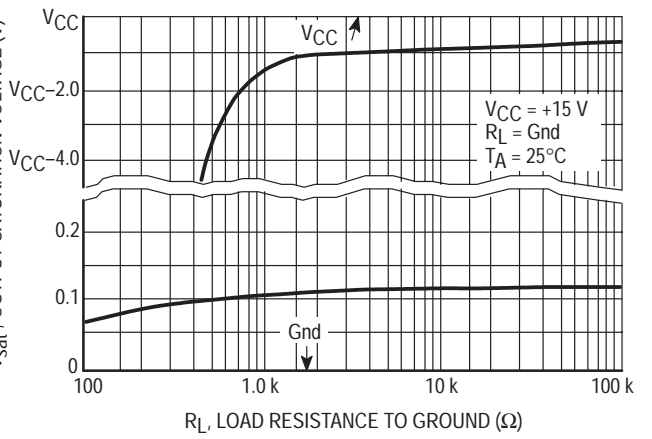


# MC34071,2,4,A MC33071,2,4,A

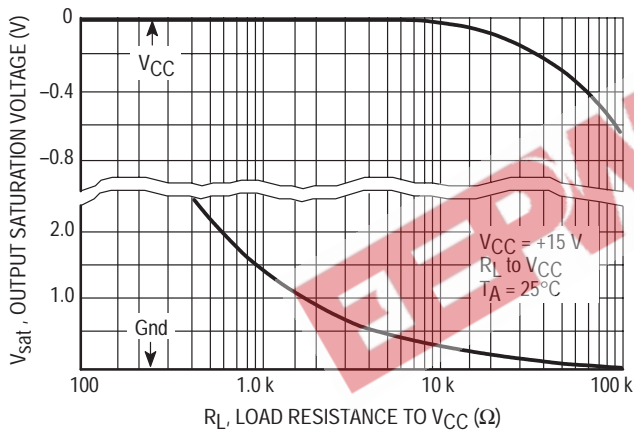
**Figure 9. Single Supply Output Saturation versus Load Resistance to V<sub>CC</sub>**



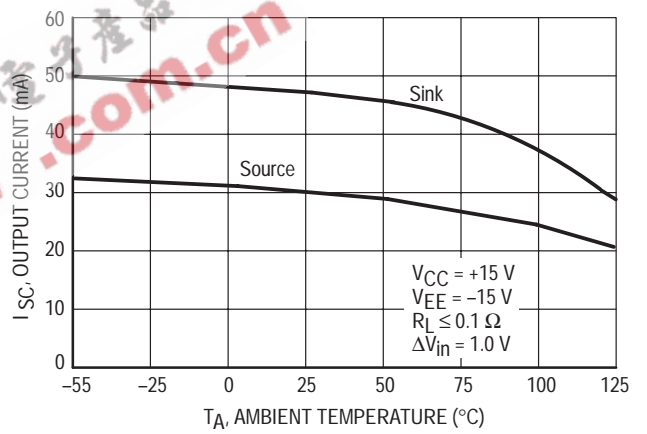
**Figure 10. Split Supply Output Saturation versus Load Current**



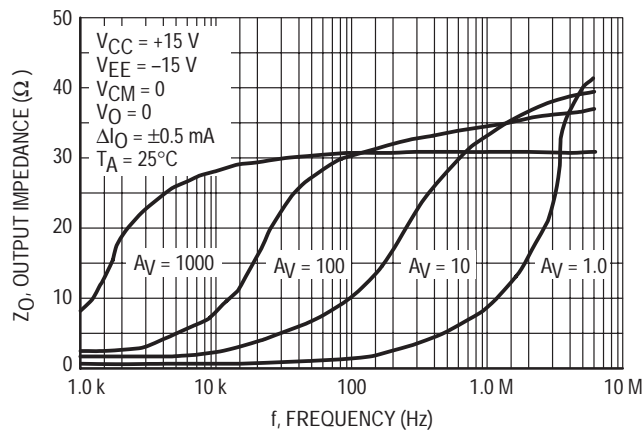
**Figure 11. Single Supply Output Saturation versus Load Resistance to Ground**



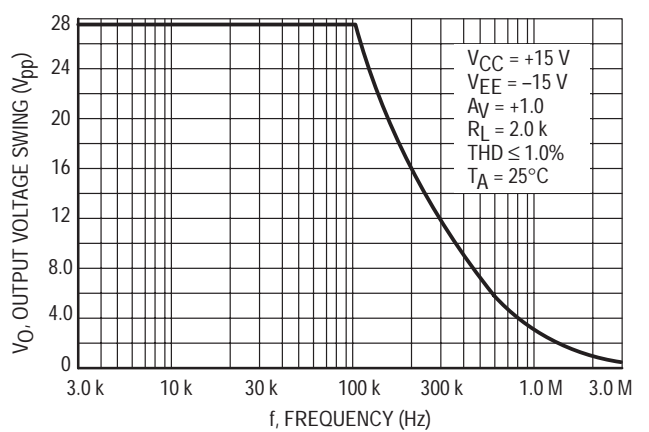
**Figure 12. Output Short Circuit Current versus Temperature**



**Figure 13. Output Impedance versus Frequency**

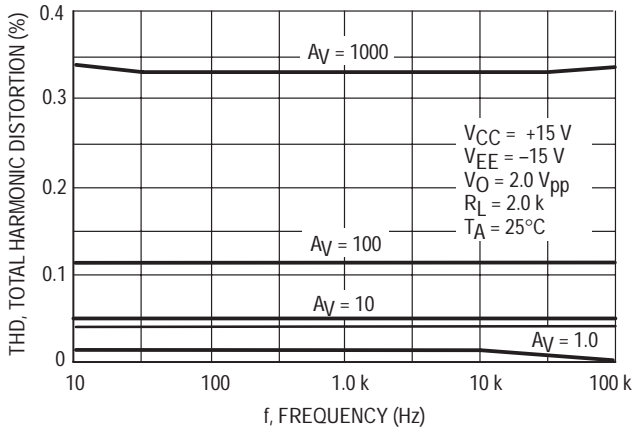


**Figure 14. Output Voltage Swing versus Frequency**

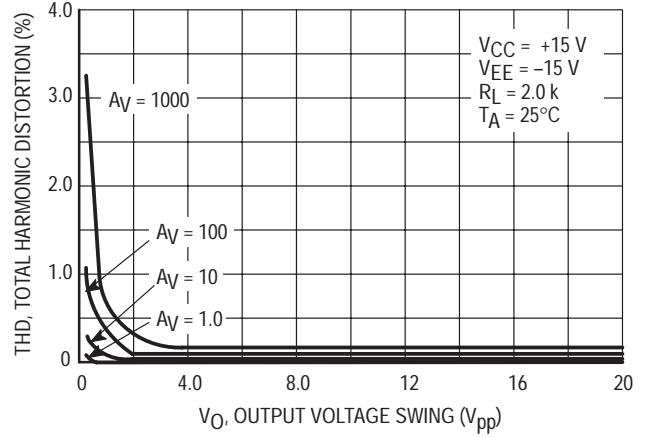


# MC34071,2,4,A MC33071,2,4,A

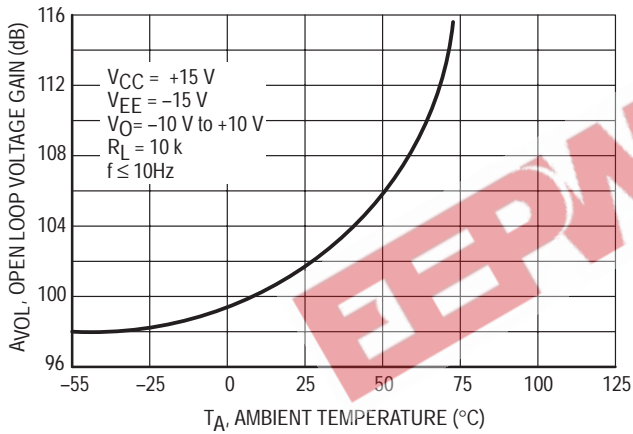
**Figure 15. Total Harmonic Distortion versus Frequency**



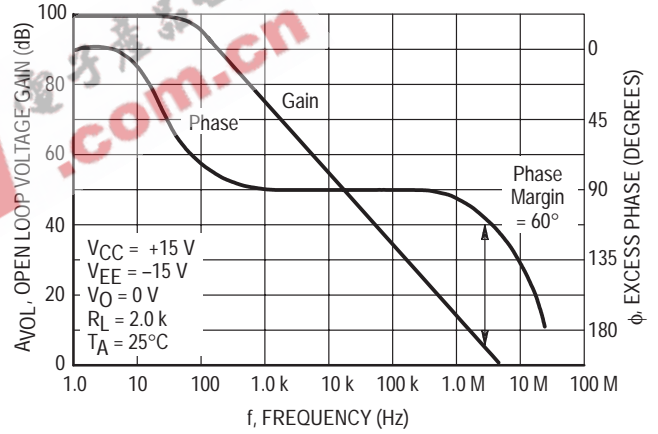
**Figure 16. Total Harmonic Distortion versus Output Voltage Swing**



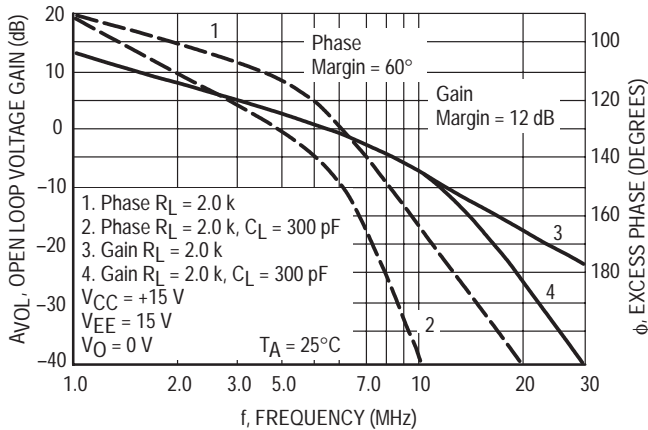
**Figure 17. Open Loop Voltage Gain versus Temperature**



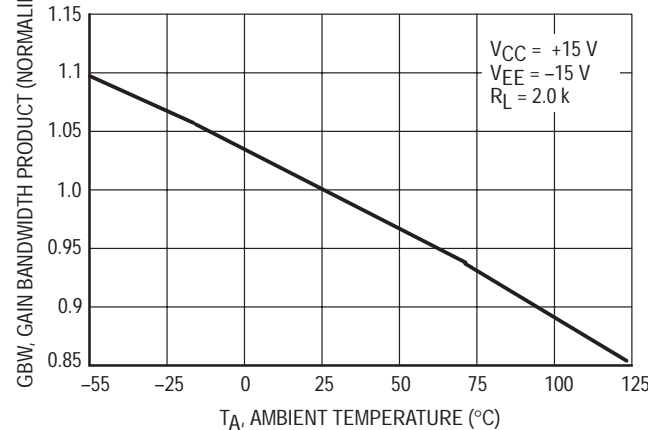
**Figure 18. Open Loop Voltage Gain and Phase versus Frequency**



**Figure 19. Open Loop Voltage Gain and Phase versus Frequency**

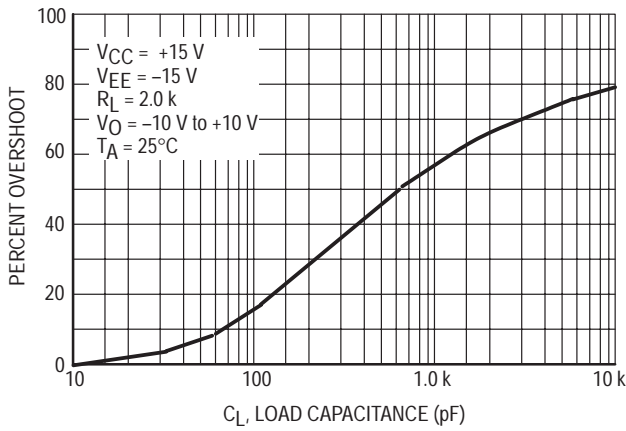


**Figure 20. Normalized Gain Bandwidth Product versus Temperature**

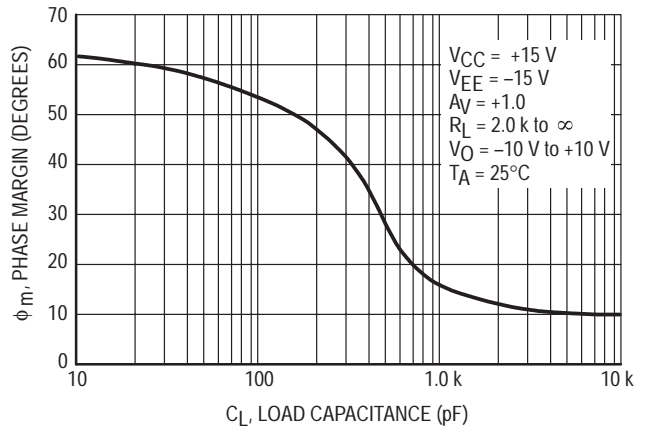


# MC34071,2,4,A MC33071,2,4,A

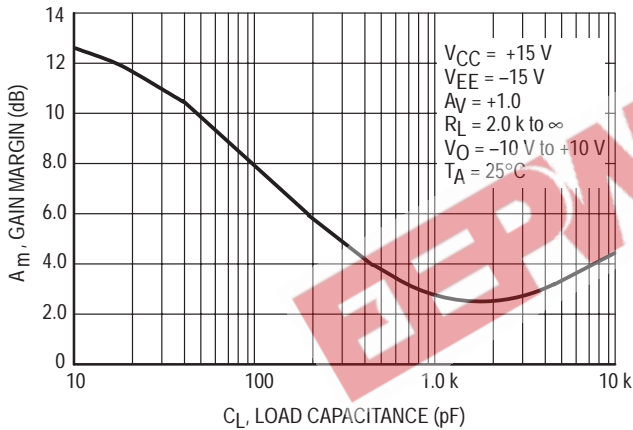
**Figure 21. Percent Overshoot versus Load Capacitance**



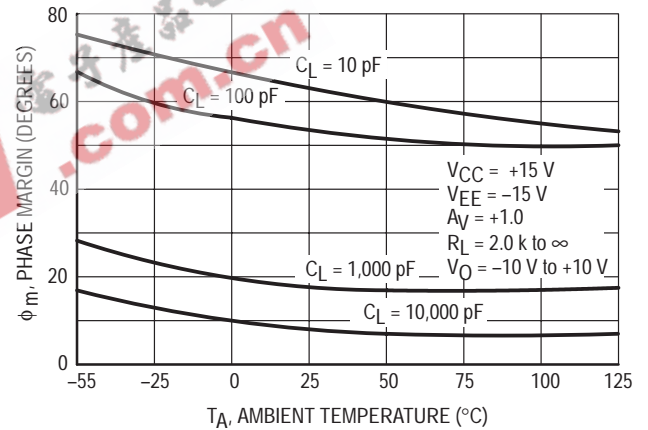
**Figure 22. Phase Margin versus Load Capacitance**



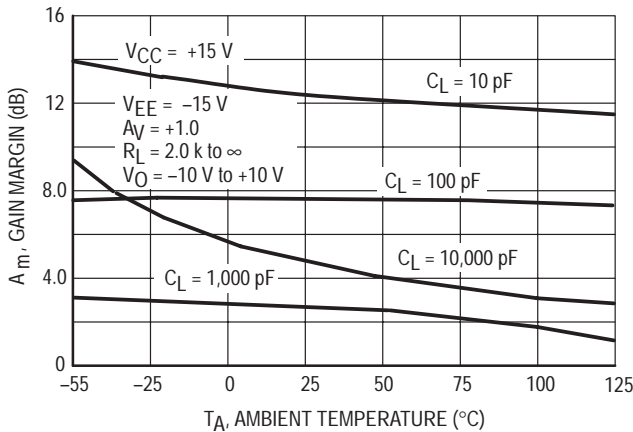
**Figure 23. Gain Margin versus Load Capacitance**



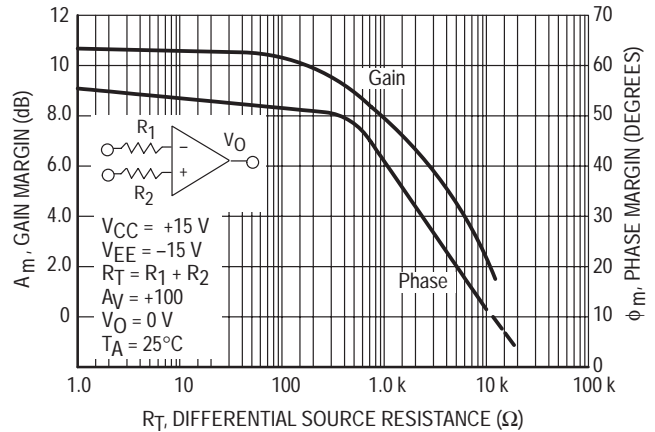
**Figure 24. Phase Margin versus Temperature**



**Figure 25. Gain Margin versus Temperature**



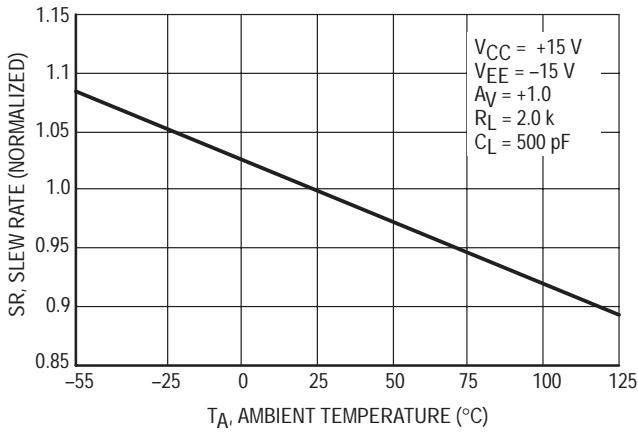
**Figure 26. Phase Margin and Gain Margin versus Differential Source Resistance**



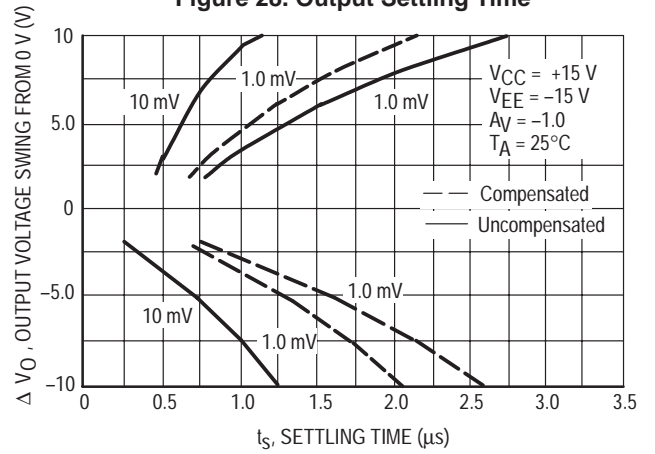


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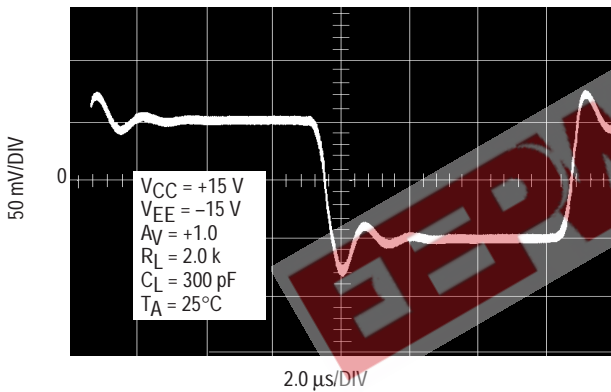
**Figure 27. Normalized Slew Rate versus Temperature**



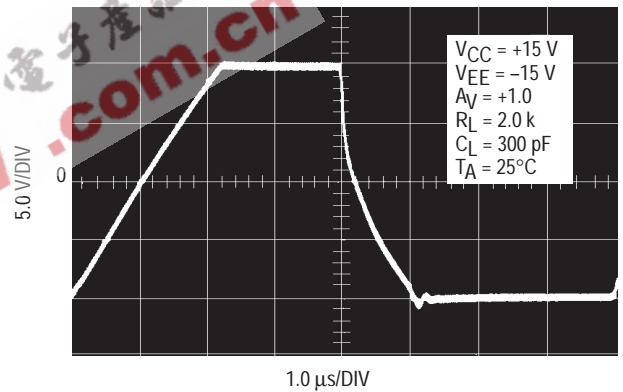
**Figure 28. Output Settling Time**



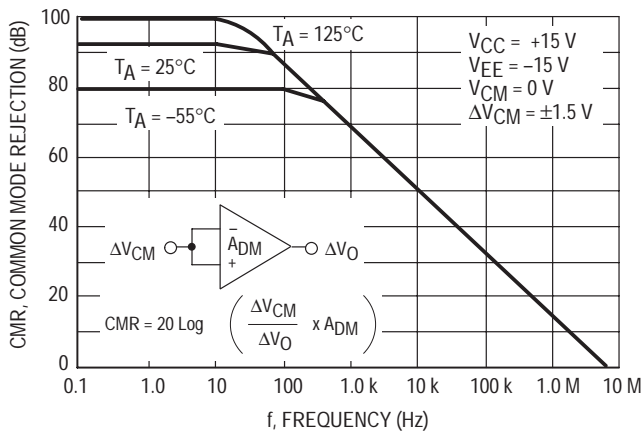
**Figure 29. Small Signal Transient Response**



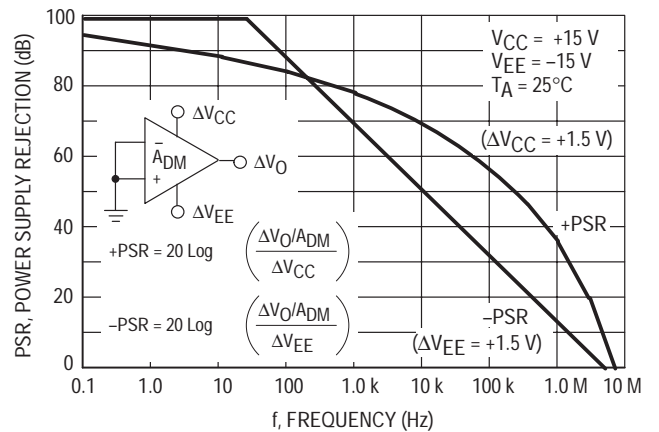
**Figure 30. Large Signal Transient Response**



**Figure 31. Common Mode Rejection versus Frequency**

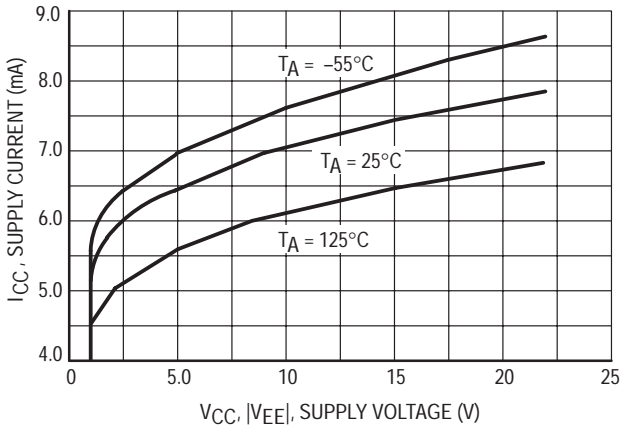


**Figure 32. Power Supply Rejection versus Frequency**

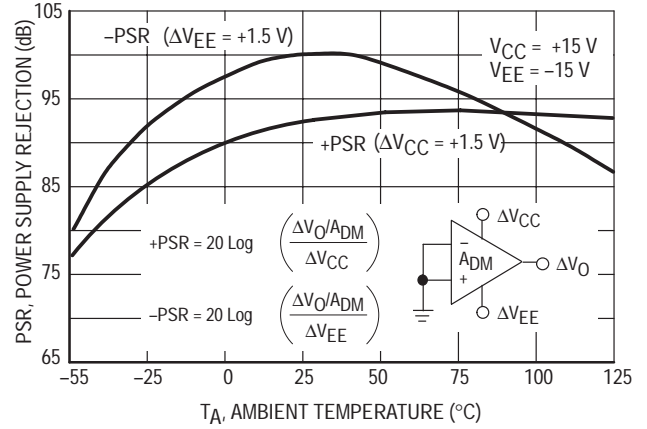


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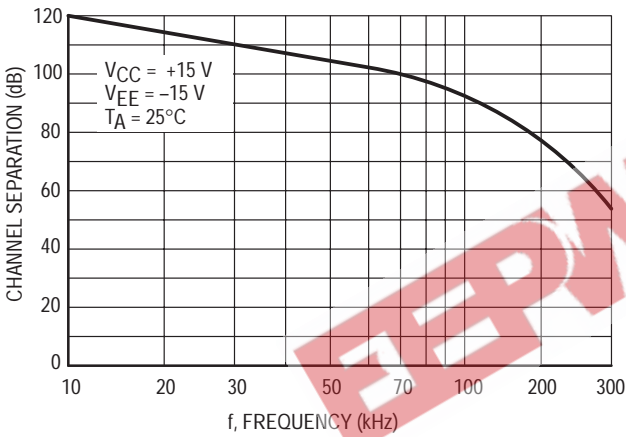
**Figure 33. Supply Current versus Supply Voltage**



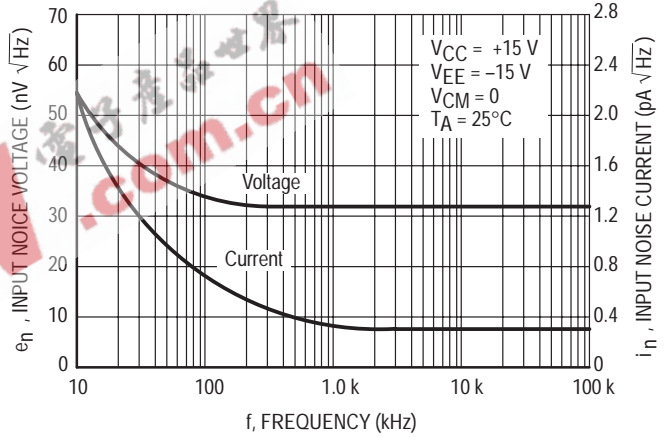
**Figure 34. Power Supply Rejection versus Temperature**



**Figure 35. Channel Separation versus Frequency**



**Figure 36. Input Noise versus Frequency**



## APPLICATIONS INFORMATION CIRCUIT DESCRIPTION/PERFORMANCE FEATURES

Although the bandwidth, slew rate, and settling time of the MC34071 amplifier series are similar to op amp products utilizing JFET input devices, these amplifiers offer other additional distinct advantages as a result of the PNP transistor differential input stage and an all NPN transistor output stage.

Since the input common mode voltage range of this input stage includes the V<sub>EE</sub> potential, single supply operation is feasible to as low as 3.0 V with the common mode input voltage at ground potential.

The input stage also allows differential input voltages up to ±44 V, provided the maximum input voltage range is not exceeded. Specifically, the input voltages must range between V<sub>EE</sub> and V<sub>CC</sub> supply voltages as shown by the maximum rating table. In practice, although not recommended, the input voltages can exceed the V<sub>CC</sub> voltage by approximately 3.0 V and decrease below the V<sub>EE</sub> voltage by 0.3 V without causing product damage, although output phase reversal may occur. It is also possible to source

up to approximately 5.0 mA of current from V<sub>EE</sub> through either inputs clamping diode without damage or latching, although phase reversal may again occur.

If one or both inputs exceed the upper common mode voltage limit, the amplifier output is readily predictable and may be in a low or high state depending on the existing input bias conditions.

Since the input capacitance associated with the small geometry input device is substantially lower (2.5 pF) than the typical JFET input gate capacitance (5.0 pF), better frequency response for a given input source resistance can be achieved using the MC34071 series of amplifiers. This performance feature becomes evident, for example, in fast settling D-to-A current to voltage conversion applications where the feedback resistance can form an input pole with the input capacitance of the op amp. This input pole creates a 2nd order system with the single pole op amp and is therefore detrimental to its settling time. In this context, lower input capacitance is desirable especially for higher

## MC34071,2,4,A MC33071,2,4,A

values of feedback resistances (lower current DACs). This input pole can be compensated for by creating a feedback zero with a capacitance across the feedback resistance, if necessary, to reduce overshoot. For 2.0 k $\Omega$  of feedback resistance, the MC34071 series can settle to within 1/2 LSB of 8 bits in 1.0  $\mu$ s, and within 1/2 LSB of 12-bits in 2.2  $\mu$ s for a 10 V step. In an inverting unity gain fast settling configuration, the symmetrical slew rate is  $\pm 13$  V/ $\mu$ s. In the classic noninverting unity gain configuration, the output positive slew rate is +10 V/ $\mu$ s, and the corresponding negative slew rate will exceed the positive slew rate as a function of the fall time of the input waveform.

Since the bipolar input device matching characteristics are superior to that of JFETs, a low untrimmed maximum offset voltage of 3.0 mV prime and 5.0 mV downgrade can be economically offered with high frequency performance characteristics. This combination is ideal for low cost precision, high speed quad op amp applications.

The all NPN output stage, shown in its basic form on the equivalent circuit schematic, offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. A 10 k $\Omega$  load resistance can swing within 1.0 V of the positive rail ( $V_{CC}$ ), and within 0.3 V of the negative rail ( $V_{EE}$ ), providing a 28.7  $V_{pp}$  swing from  $\pm 15$  V supplies. This large output swing becomes most noticeable at lower supply voltages.

The positive swing is limited by the saturation voltage of the current source transistor Q7, and  $V_{BE}$  of the NPN pull up transistor Q17, and the voltage drop associated with the short circuit resistance, R7. The negative swing is limited by the saturation voltage of the pull-down transistor Q16, the voltage drop  $I_L R_6$ , and the voltage drop associated with resistance R7, where  $I_L$  is the sink load current. For small valued sink currents, the above voltage drops are negligible, allowing the negative swing voltage to approach within millivolts of  $V_{EE}$ . For large valued sink currents (>5.0 mA), diode D3 clamps the voltage across R6, thus limiting the negative swing to the saturation voltage of Q16, plus the forward diode drop of D3 ( $\approx V_{EE} + 1.0$  V). Thus for a given supply voltage, unprecedented peak-to-peak output voltage swing is possible as indicated by the output swing specifications.

If the load resistance is referenced to  $V_{CC}$  instead of ground for single supply applications, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to  $V_{CC}$  during the positive swing and the output will pull the load resistance near ground during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull up capability.

Because the PNP output emitter-follower transistor has been eliminated, the MC34071 series offers a 20 mA

minimum current sink capability, typically to an output voltage of ( $V_{EE} + 1.8$  V). In single supply applications the output can directly source or sink base current from a common emitter NPN transistor for fast high current switching applications.

In addition, the all NPN transistor output stage is inherently fast, contributing to the bipolar amplifier's high gain bandwidth product and fast settling capability. The associated high frequency low output impedance (30  $\Omega$  typ @ 1.0 MHz) allows capacitive drive capability from 0 pF to 10,000 pF without oscillation in the unity closed loop gain configuration. The 60° phase margin and 12 dB gain margin as well as the general gain and phase characteristics are virtually independent of the source/sink output swing conditions. This allows easier system phase compensation, since output swing will not be a phase consideration. The high frequency characteristics of the MC34071 series also allow excellent high frequency active filter capability, especially for low voltage single supply applications.

Although the single supply specifications is defined at 5.0 V, these amplifiers are functional to 3.0 V @ 25°C although slight changes in parametrics such as bandwidth, slew rate, and DC gain may occur.

If power to this integrated circuit is applied in reverse polarity or if the IC is installed backwards in a socket, large unlimited current surges will occur through the device that may result in device destruction.

Special static precautions are not necessary for these bipolar amplifiers since there are no MOS transistors on the die.

As with most high frequency amplifiers, proper lead dress, component placement, and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input-output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous "pick up" at this node. Supply decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

The output of any one amplifier is current limited and thus protected from a direct short to ground. However, under such conditions, it is important not to allow the device to exceed the maximum junction temperature rating. Typically for  $\pm 15$  V supplies, any one output can be shorted continuously to ground without exceeding the maximum temperature rating.

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(Typical Single Supply Applications  $V_{CC} = 5.0\text{ V}$ )

Figure 37. AC Coupled Noninverting Amplifier

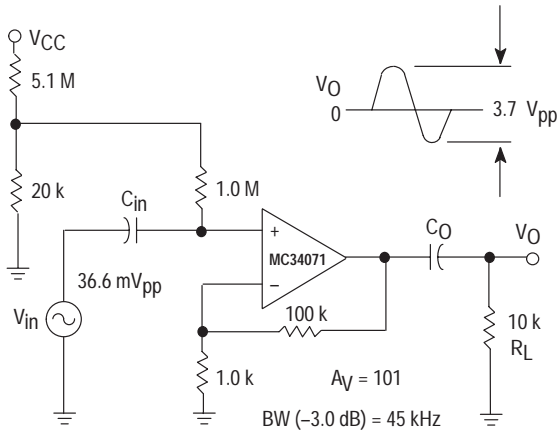


Figure 38. AC Coupled Inverting Amplifier

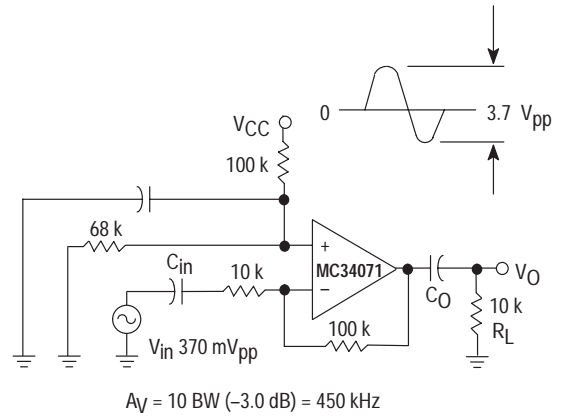


Figure 39. DC Coupled Inverting Amplifier  
Maximum Output Swing

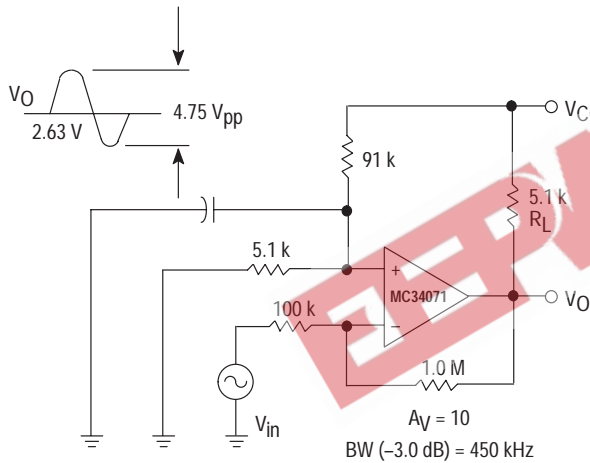


Figure 40. Unity Gain Buffer TTL Driver

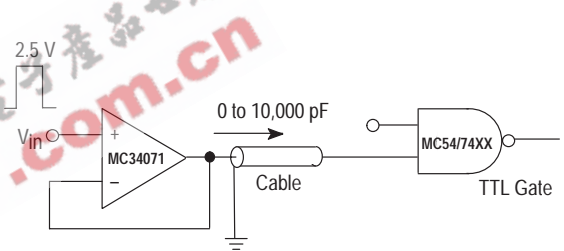


Figure 41. Active High-Q Notch Filter

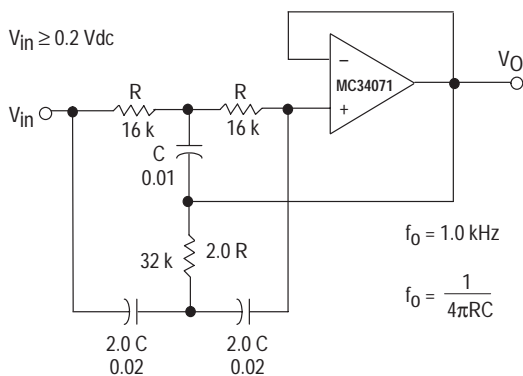
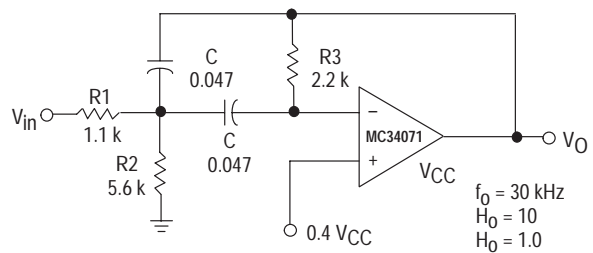


Figure 42. Active Bandpass Filter



Given  $f_0$  = Center Frequency  
 $A_0$  = Gain at Center Frequency  
 Choose Value  $f_0$ ,  $Q$ ,  $A_0$ ,  $C$

Then:

$$R_3 = \frac{Q}{\pi f_0 C} \quad R_1 = \frac{R_3}{2H_0} \quad R_2 = \frac{R_1 R_3}{4Q^2 R_1 - R_3}$$

For less than 10% error from operational amplifier  $\frac{Q_0 f_0}{GBW} < 0.1$

where  $f_0$  and  $GBW$  are expressed in Hz.  
 $GBW = 4.5\text{ MHz Typ.}$

# MC34071,2,4,A MC33071,2,4,A

Figure 43. Low Voltage Fast D/A Converter

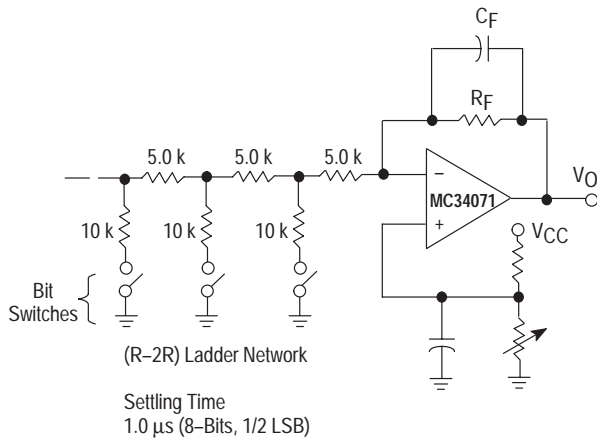


Figure 44. High Speed Low Voltage Comparator

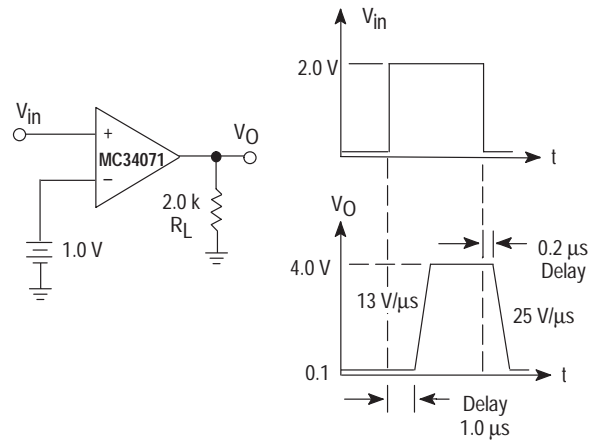


Figure 45. LED Driver

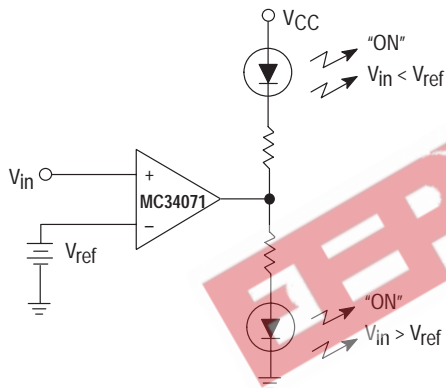


Figure 46. Transistor Driver

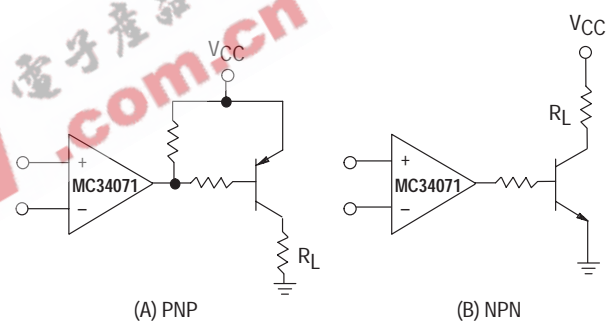


Figure 47. AC/DC Ground Current Monitor

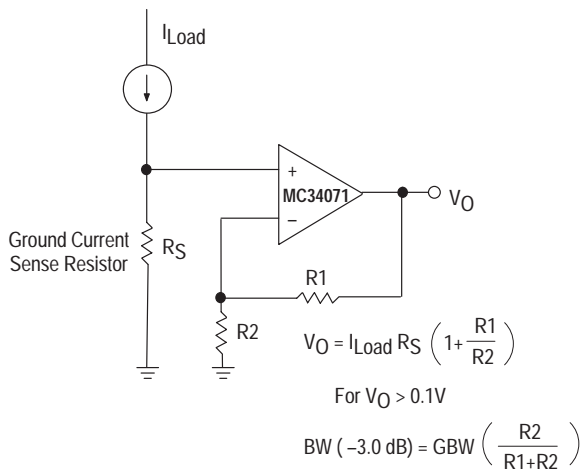
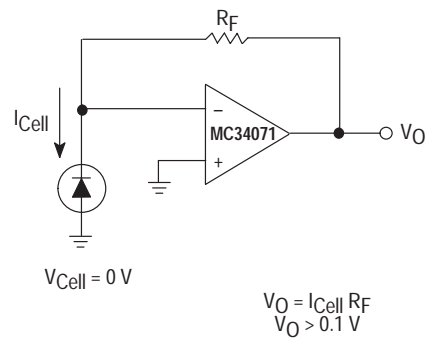
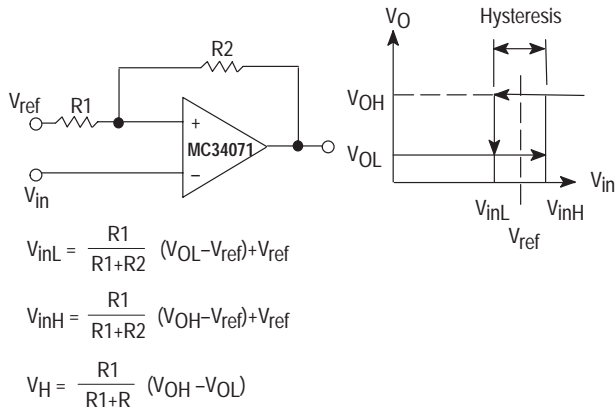


Figure 48. Photovoltaic Cell Amplifier

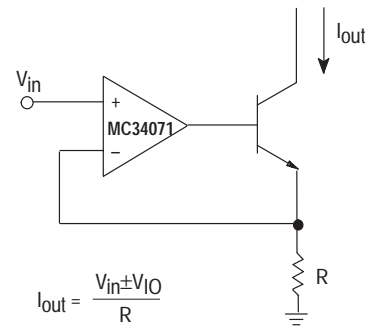


## MC34071,2,4,A MC33071,2,4,A

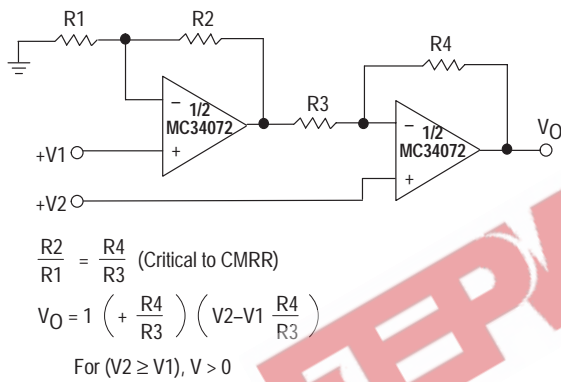
**Figure 49. Low Input Voltage Comparator with Hysteresis**



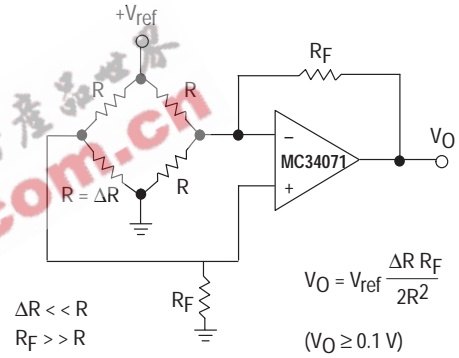
**Figure 50. High Compliance Voltage to Sink Current Converter**



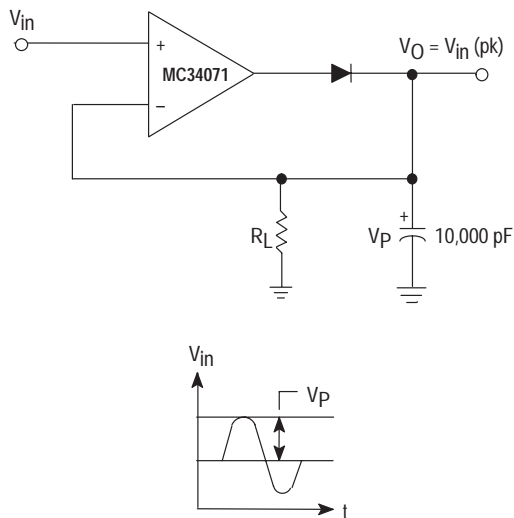
**Figure 51. High Input Impedance Differential Amplifier**



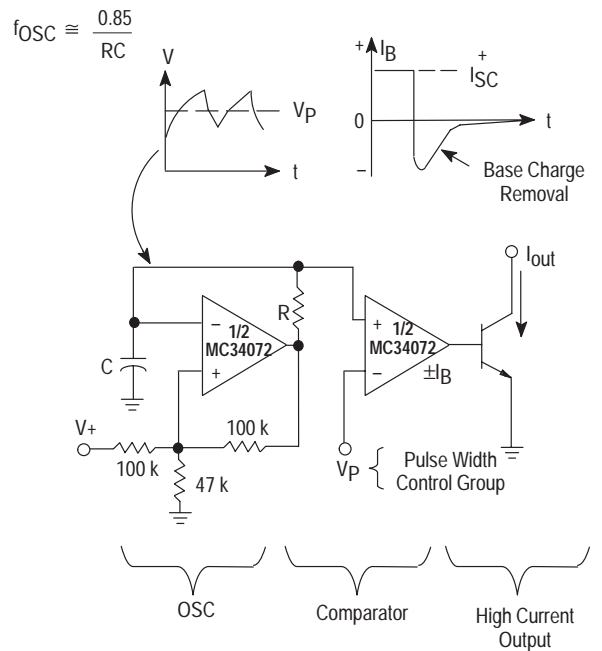
**Figure 52. Bridge Current Amplifier**



**Figure 53. Low Voltage Peak Detector**



**Figure 54. High Frequency Pulse Width Modulation**



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GENERAL ADDITIONAL APPLICATIONS INFORMATION  $V_S = \pm 15.0\text{ V}$

Figure 55. Second Order Low-Pass Active Filter

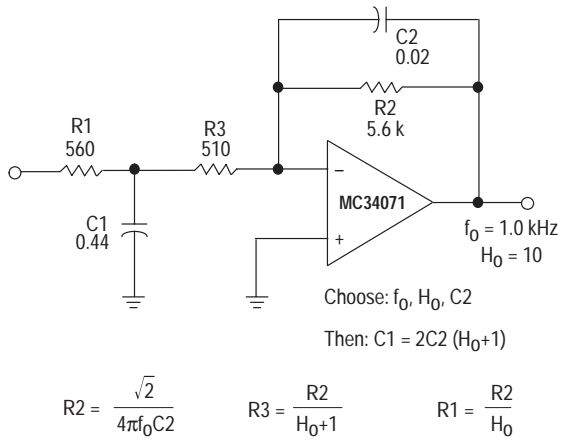


Figure 56. Second Order High-Pass Active Filter

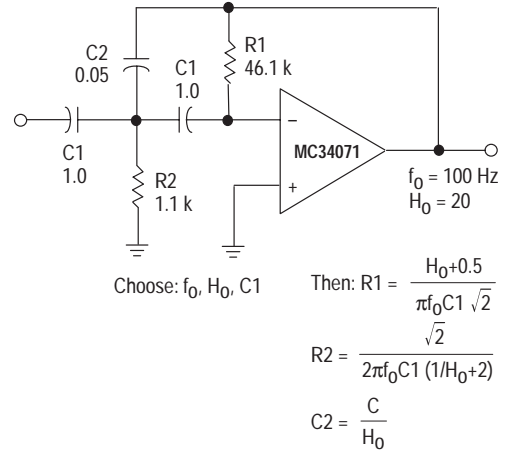


Figure 57. Fast Settling Inverter

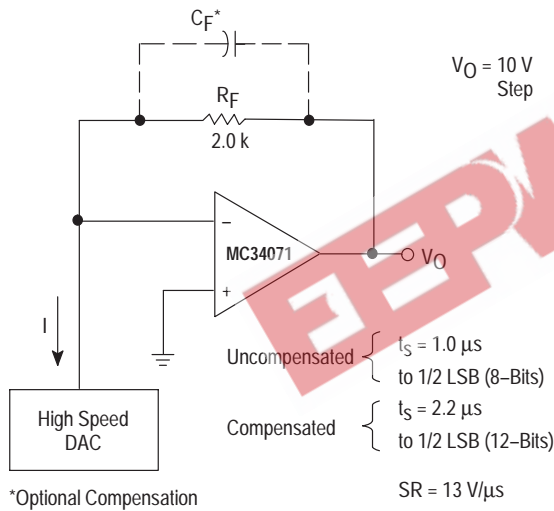


Figure 58. Basic Inverting Amplifier

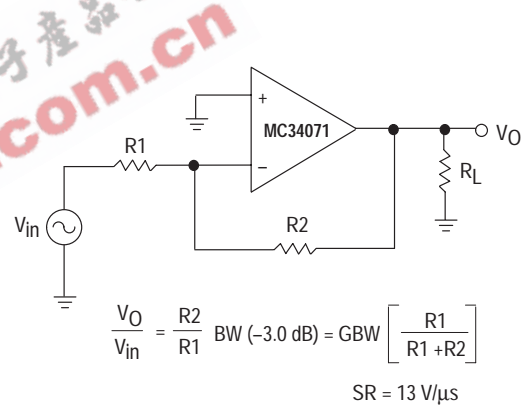


Figure 59. Basic Noninverting Amplifier

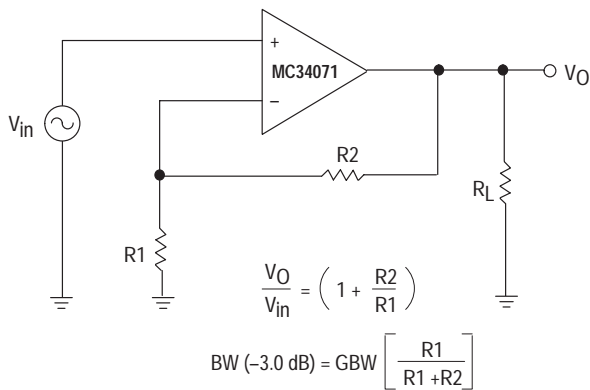
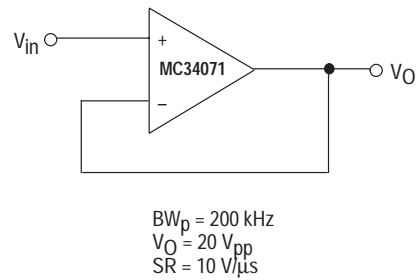


Figure 60. Unity Gain Buffer ( $A_V = +1.0$ )



## MC34071,2,4,A MC33071,2,4,A

Figure 61. High Impedance Differential Amplifier

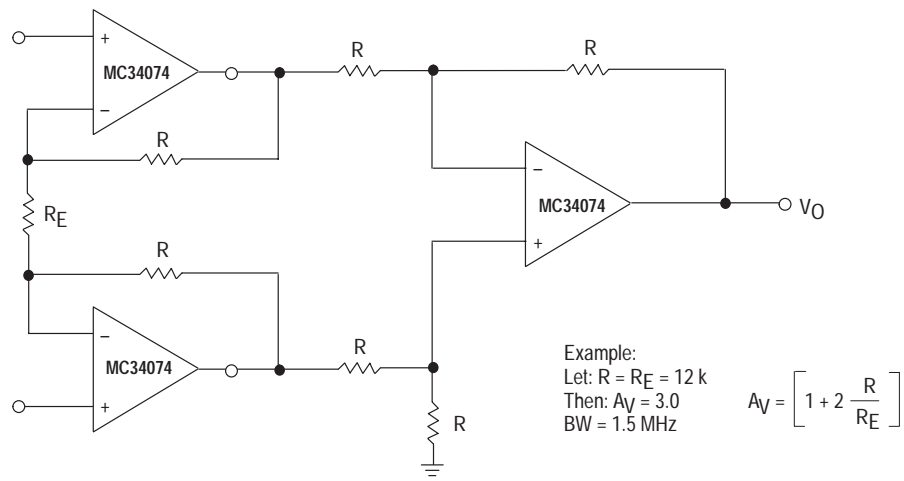
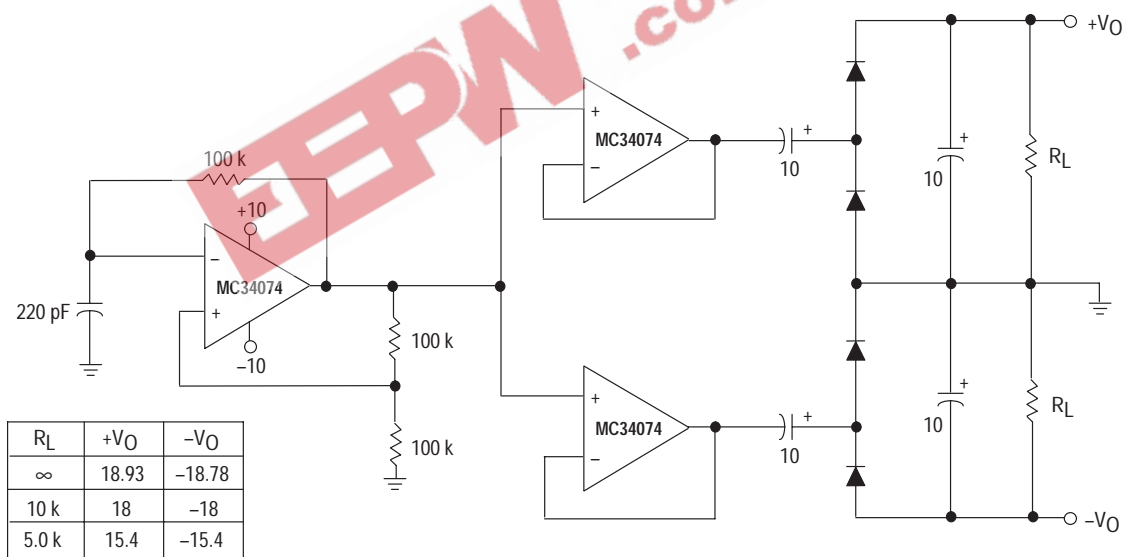


Figure 62. Dual Voltage Doubler





## MC34071,2,4,A MC33071,2,4,A

### ORDERING INFORMATION

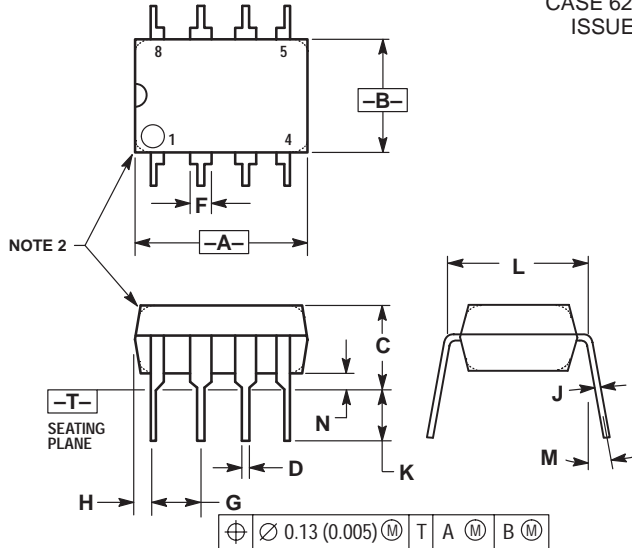
Op Amp Function	Device	Operating Temperature Range	Package	Shipping
Single	MC34071P, MC34071AP MC34071D, MC34071AD MC34071DR2, MC34071ADR2	$T_A = 0^\circ$ to $+70^\circ\text{C}$	DIP-8 SO-8 SO-8 / Tape & Reel	50 Units / Rail 98 Units / Rail 2500 Units / Tape & Reel
	MC33071P, MC33071AP MC33071D, MC33071AD MC33071DR2, MC33071ADR2	$T_A = -40^\circ$ to $+85^\circ\text{C}$	DIP-8 SO-8 SO-8 / Tape & Reel	50 Units / Rail 98 Units / Rail 2500 Units / Tape & Reel
Dual	MC34072P, MC34072AP MC34072D, MC34072AD MC34072DR2, MC34072ADR2	$T_A = 0^\circ$ to $+70^\circ\text{C}$	DIP-8 SO-8 SO-8 / Tape & Reel	50 Units / Rail 98 Units / Rail 2500 Units / Tape & Reel
	MC33072P, MC33072AP MC33072D, MC33072AD MC33072DR2, MC33072ADR2	$T_A = -40^\circ$ to $+85^\circ\text{C}$	DIP-8 SO-8 SO-8 / Tape & Reel	50 Units / Rail 98 Units / Rail 2500 Units / Tape & Reel
	MC34072VD MC34072VDR2	$T_A = -40^\circ$ to $+125^\circ\text{C}$	SO-8 SO-8 / Tape & Reel	98 Units / Rail 2500 Units / Tape & Reel
Quad	MC34074P, MC34074AP MC34074D, MC34074AD MC34074DR2, MC34074ADR2	$T_A = 0^\circ$ to $+70^\circ\text{C}$	DIP-8 SO-8 SO-8 / Tape & Reel	50 Units / Rail 98 Units / Rail 2500 Units / Tape & Reel
	MC33074P, MC33074AP MC33074D, MC33074AD MC33074DR2, MC33074ADR2 MC33074DTB, MC33074ADTB MC33074DTBR2, MC33074ADTBR2	$T_A = -40^\circ$ to $+85^\circ\text{C}$	DIP-8 SO-8 SO-8 / Tape & Reel TSSOP-14 TSSOP-14 / Tape & Reel	50 Units / Rail 98 Units / Rail 2500 Units / Tape & Reel 96 Units / Rail 2500 Units / Tape & Reel
	MC34074VD MC34074VDR2	$T_A = -40^\circ$ to $+125^\circ\text{C}$	SO-8 SO-8 / Tape & Reel	98 Units / Rail 2500 Units / Tape & Reel

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# MC34071,2,4,A MC33071,2,4,A

## PACKAGE DIMENSIONS

### P SUFFIX PLASTIC PACKAGE CASE 626-05 ISSUE K

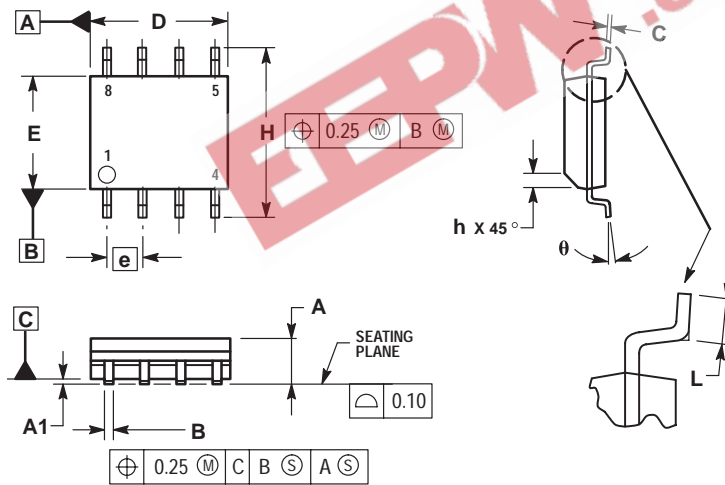


NOTES:

1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

### D SUFFIX (SO-8) PLASTIC PACKAGE CASE 751-05 ISSUE R



NOTES:

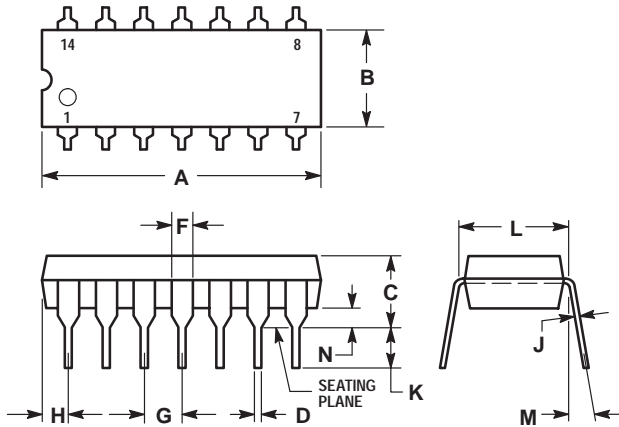
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

# MC34071,2,4,A MC33071,2,4,A

## PACKAGE DIMENSIONS

**P SUFFIX**  
 PLASTIC PACKAGE  
 CASE 646-06  
 ISSUE L

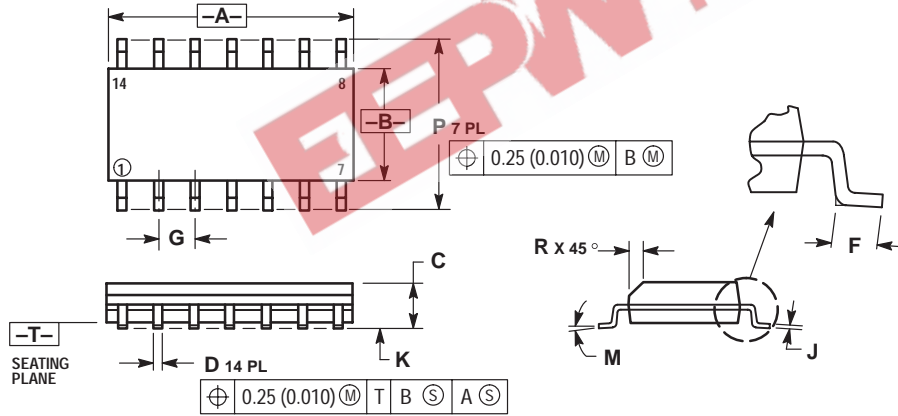


**NOTES:**

- LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

**D SUFFIX**  
 (SO-14)  
 PLASTIC PACKAGE  
 CASE 751A-03  
 ISSUE F



**NOTES:**

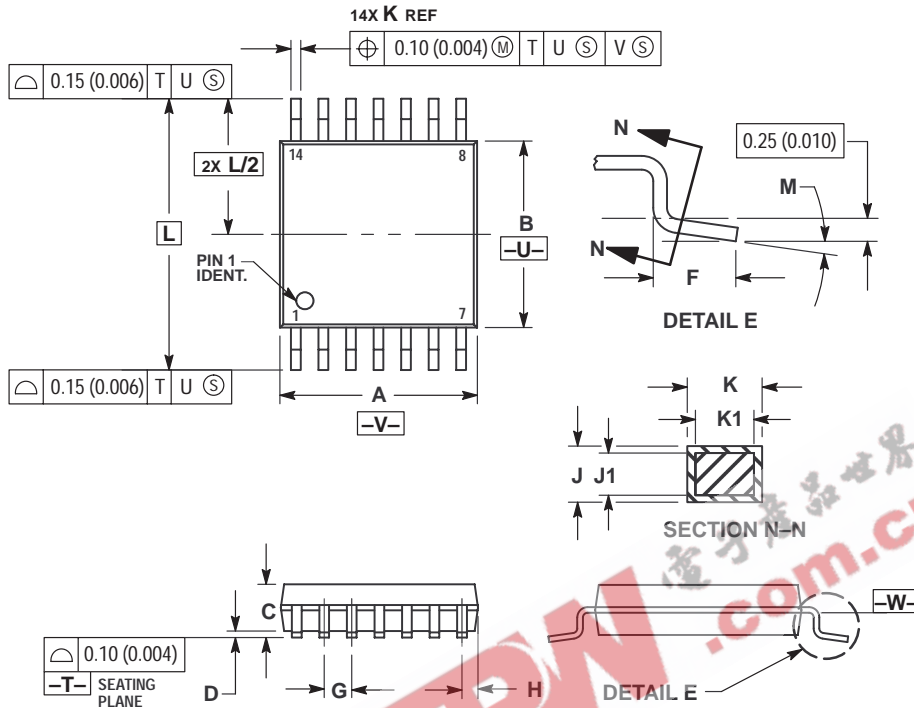
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

# MC34071,2,4,A MC33071,2,4,A

## PACKAGE DIMENSIONS

DTB SUFFIX  
(TSSOP-14)  
PLASTIC PACKAGE  
CASE 948G-01  
ISSUE O



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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