

# **MI-Bus Interface Stepper Motor Controller**

The MC33192 Stepper Motor Controller is intended to control loads in harsh automotive environments using a serial communication bus. The MI–Bus can provide satisfactory real time control of up to eight stepper motors. MI–Bus technology offers a noise immune system solution for difficult control applications involving relay drivers, motor controllers, etc.

The MC33192 stepper motor controller provides four phase signals to drive two phase motors in either half or full step modes. When used with an appropriate Motorola HCMOS microprocessor it provides an economical solution for applications requiring a minimum amount of wiring and optimized system versatility.

The MC33192 is packaged in an economical 16 pin surface mount package and specified at an operating voltage 12 V for –  $40^{\circ}$ C  $\leq$  T<sub>A</sub>  $\leq$  100 $^{\circ}$ C.

- Single Wire Open Bus Capability Up to 10 Meters in Length
- Programmable Address Bus System
- Fault Detection of Half–Bridge Drivers and Motor Windings
- Ceramic Resonator For Accurate and Reliable Transmission of Data
- Sub–Multiple of Oscillator End–of–Frame Signal
- MI–Bus Signal Slew Rate Limited to 1.0 V/µs for Minimum RFI
- MI–Bus Error Diagnostics
- Non–Functioning Device Diagnotics
- Over Temperature Detection
- **Address Programming Sequence Status**
- Load and Double Battery (Jump Start) Protection



# **MI–BUS INTERFACE STEPPER MOTOR CONTROLLER**

**SEMICONDUCTOR TECHNICAL DATA**









#### **ORDERING INFORMATION**







**DC ELECTRICAL CHARACTERISTICS** (Characteristics noted under conditions 9.0 V ≤ V<sub>CC</sub> ≤ 15.5 V, – 40°C ≤ T<sub>A</sub> ≤ 100°C, unless otherwise noted.)



CONTROL LOGIC ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions 9.0 V ≤ V<sub>CC</sub> ≤ 15.5 V, – 40°C ≤ T<sub>A</sub> ≤ 100°C, unless otherwise noted.)



**NOTES:** 1. Transient capability is defined as the positive overvoltage transient with 250 ms decay time constant. The detection on an overvoltage condition causes all H–Bridges to be latched "off".

2. Ambient temperature is given as a convience; Maximum junction temperature is the limiting factor.

3. Load Dump is the inductive transient voltage imposed on an automotive battery line as a result of opening the battery connection while the alternator system is producing charge current. The detection on an overvoltage condition causes all H–Bridges to be latched "off".

4. Standby Current is with both H–Bridges "off" (Inh1 = Inh2 = 0).

5. H–Bridge Saturation Voltage is referenced to the positive supply or ground respective of the H–Bridge output being High or Low.

Saturation voltage is the voltage drop from the output to the positive supply (with output High) and the voltage drop to ground (with output Low). 6. Address Programming Current is the current encountered when the bus is at 12 V during address programming.

7. A typical application uses an external ceramic resonator crystal having a frequency of 644 kHz. An internal capacitor in parallel with ceramic resonator is used to shift the frequency to the working frequency of 640 kHz. The frequency accuracy of the oscillator is dependant on the capacitor and ceramic resonator tolerance (usually ±1.0%).

8. The Message Time Slot is the time required for one complete device message transfer. The message time is equivalent to a total of 16 periods of the oscillator frequency used.

9. If the MI–Bus becomes shorted to ground, all MC33192 outputs will be disabled after a period of nine time slots (9t<sub>S</sub>).

10. MI–Bus voltage required for address programming.

#### **GENERAL DESCRIPTION**

The MC33192 is a serial stepper motor controller for use in harsh automotive applications using multiplex wiring. The MC33192 provides all the necessary four phase drive signals to control two phase bipolar stepper motors operated in either half or full step modes. Multiple stepper motor controllers can be operated on a real time basis at step frequencies up to 200 Hz using a single microcontroller (MCU). A primary attribute of operation is the utilization of the MI–Bus message media to provide high noise immunity communication ensuring very high operating reliability of motor stepping.

The MC33192 is designed to drive bipolar stepper motors having a winding resistance of 80  $\Omega$  at 20°C with a supply voltage of 12 V. It is supplied in a SO–16L plastic package having eight pins, on one side, connected directly to the lead frame thus enhancing the thermal performance to allow a power dissipation of 0.5 W at 120°C ambient temperature.

#### **Multiple Simultaneous Motor Operation**

Several motors can be controlled in a serial fashion, one after the other, using the same software time base. The time base determines the step frequency of the motors. A single motor can be operated at a maximum speed of 200 Hz pull–in with a duration of 5.0 ms per step. Three motors can be operated simultaneously using a 68HC05B6 MCU at the same time base (200 Hz) with about 1.7 ms per step. A 68HC11 MCU can control 4 stepper motors with adequate program step time. The step frequency must be decreased to control additional motors. To control eight motors simultaneously would require the motor speed to be

decreased to 100 Hz producing about 2.0 ms time duration per step with adequate program time.

#### **MI–Bus General Description**

The Motorola Interconnect Bus (MI–Bus) is a serial push–pull communications protocol which efficiently supports distributed real time control while exhibiting a high level of noise immunity.

Under the SAE Vehicle Network categories, the MI–Bus is a Class A bus with a data stream transfer bit rate in excess of 20 kHz and thus inaudible to the human ear. It requires a single wire to carry the control data between the master MCU and its slave devices. The bus can be operated at lengths up to 15 meters.

At 20 kHz the time slot used to construct the message  $(25 \,\mu s)$  can be handled by software using many MCUs available on the market.

The MI–Bus is suitable for medium speed networks requiring very low cost multiplex wiring. Aside from ground, the MI–Bus requires only one signal wire connecting the MCU to multiple slave MC33192 devices with individual control.

A single MI–Bus can accomplish simultaneous automotive system control of Air Conditioning, Head Lamp Levellers, Window Lifts, Sensors, Intelligent Coil Drivers, etc. The MI–Bus has been found to be cost effective in vehicle body electronics by replacing the conventional wiring harness.

Figure 1 shows the internal block diagram of the MC33192 Stepper Motor Controller.



#### **Figure 1. MC33192 Stepper Motor Conroller Block Diagram**

**NOTE:** (\*) Pins 2, 9, 10, 11, 12, 13, 14, 15 and 16 are common electrical and heatsink ground pins for the device.

#### **MI–Bus Access Method**

The information on the MI–Bus is sent in a fixed message frame format (See Figure 4). The system MCU can take control of the MI–Bus at any time with a start bit which violates the law of Manchester Bi–Phase code by having three consecutive Time Slots  $(3t<sub>s</sub>)$  held constantly at a Logic "0" state.

#### **Push–Pull Communication Sequence**

Communication between the system MCU and slave MC33192 devices always use the same message frame organization. The MCU first sends eight serial data bits over the MI–Bus comprised of five control bits followed by three address bits. This communication sequence is called a "Push Field" since it represents command information sent from the MCU. The sequence of the five control data bits follow the order D0, D1, D2, D3 and D4. The three address bits are sent in sequential order A0, A1 and A2 defining a binary address code. The condition of MI–Bus during any of the control bit time windows defines a specific control function as shown in Figure 2. A "Pull Sync" bit is sent at the end of the Push Field, the positive edge of which causes all data sent to the selected device to be latched into the output circuit.

**Figure 2. Push Field Data Bits**

<b>Bit</b>	Name	<b>Control Function</b>	synchronization with the MCU's machine cycle. The strobe pulse occurs only after the Push Field sequence is validated
D4	lnh2	Inhibits H-Bridge 2	by the address selected device.
D <sub>3</sub>	Dir <sub>2</sub>	Establishes Direction of H-Bridge 2 Current	<b>Message Validation</b>
D <sub>2</sub>	E	Energizes Bridge Coils 1 and 2	The communication between the MCU and the selected MC33192 device is valid only when the MCU reads
D <sub>1</sub>	Dir1	Establishes Direction of H-Bridge 1 Current	(receives) the Pull Field Data having the correct codes
D <sub>0</sub>	Inh1	Inhibits H-Bridge 1	(excluding the code "1-1-1" and "0-0-0") followed by an
			End-of-Frame signal The frequency of the End-of-Frame

After the Pull Sync bit is sent, following the Push Field, the MCU listens on the MI–Bus for serial data bits sent back from the previously addressed MC33192 device. This portion of the communication sequence starts the "Pull Field Data" since it represents information pulled from the addressed MC33192 and received by the MCU.

The address selected MC33192 device sends data, in the form of status bits, back to the MCU reporting the devices condition. At the end of the Push Field the MCU

outputs a Pull Sync bit which signals the start of the Pull Field. In the Pull Field are three bits (S2, S1 and S0) which report the status of the previously addressed MC33192 according to Figure 3.





**EXECUTE:** The synchronization with the MCU's machine cycle. The strobe **Name**<br> **Rame**<br> **Example 2018 Control Function**<br> **Example 2018 Dulse occurs only after the Push Field sequence is validated**  The positive edge of the Pull Sync pulse (set by the MCU) causes all Push Field Data sent to the selected MC33192 to be stored in the output latch circuit in time with the strobe pulse. This means the data bits are emitted in real time

#### **Message Validation**

Energizes Bridge Coils 1 and 2<br>MC33192 device is valid only when the MCU reads (excluding the code "1–1–1" and "0–0–0") followed by an Establishes Direction of H–Bridge 1 Current (receives) the Pull Field Data having the correct codes Inhibits H–Bridge 1 (excluding the code  $1-1-1$  and  $0-0-0$  ) followed by an End–of–Frame signal. The frequency of the End–of–Frame signal may be a sub–multiple of the selected devices local oscillator or related to an internal or external analog parameter using a Voltage to Frequency Converter.

#### **Error Detection**

An error is detected when the Pull Field contains the code "1–1–1" followed by the End–of–Frame permanently tied to a logic "1" state (internally from 5.0 V through a pull–up resistor). This means the communication between the MCU and the selected device was not obtained.



#### **Figure 4. MI–Bus Timing Diagram**

There are four types of system error detections which are not mutually exclusive; These are:

#### 1) Noise Detection

The system MC33192 slave devices receive the Push Field message from the MCU twice for each Time Slot  $(t<sub>s</sub>)$ of the Bi–Phase Code. A receive error occurs when the two message samples fail to "logic wise" match. Noise and Bi–Phase detection are discussed further under Message Coding.

#### 2) Bi–Phase Detection

The system slave devices receiving the Push Field message from the MCU detect the Bi–Phase Code. A detector error occurs when the two time slots of the Bi–Phase Code do not contain an Exclusive–OR logic function.

#### 3) Field Check

A field error is detected when a fixed–form bit field contains an improper number of bits. A bit error can also be detected by the MCU during the Push Field. The MCU can simultaneously monitor the MI–Bus at the time it is sending data. A bit error is detected if the sent bit value does not match the value which was monitored.

#### 4) Urgent Output Disable

If the MI–Bus becomes shorted to ground, the slave device outputs will be disabled after a period of 9ts. The MCU itself can take advantage of this feature to "globally" disable the outputs of all system slave devices by keeping the MI–Bus at a logic "0" level for a duration of 9ts or more. Normal operation is resumed when the MCU sends a "standard" instruction over the MI–Bus.

#### **Basic Stepper Motor Construction and Operation**

Stepper motors are constructed with a permanent magnet rotor magnetized with the same number of pole pairs as contained in one stator coil section. Operationally, stepper motors rotate at constant incremental angles by stepping one step every time the current switches discretely in one stator field coil causing the North–South stator field to rotate either clockwise or counter–clockwise causing the permanent magnet rotor to follow (see Figure 5). For simplicity, assume the starting condition of the A1 to A2 stator field to be top to bottom polarized N to S and the B1 to B2 stator field to be left to right polarized N to S. The resulting stator field will produce a vector which points in the direction of position 3. The rotor will, in this case, be in the position shown in Figure 5 (pointing to position 1). This initial condition corresponds to that of step 1 in Figure 6. As the direction of current flow in the B1 to B2 stator field is reversed, the field polarity of the B1 to B2 also reverses and is left to right polarized S to N. This causes the resulting stator field vector to point in the direction of position 4. This in turn causes the N–S rotor to follow and rotate 90° in a clockwise direction and point in the direction of position 2. This condition corresponds to step 2 of Figure 6. Continued clockwise rotor steps will be experienced as the stator field continues to be incrementally rotated as shown in steps 3, 4, 5, etc. of Figure 6. The 90° steps in this simplistic example constitute "full steps". It is to be noticed that both coils, in the foregoing full step example, were simultaneously energized in one of two directions. It is possible to increment the rotor in 45° "intermediate steps" or "half steps" by alternately energizing only one stator coil at a time in the appropriate direction while turning the other stator coil off. The drive signals for Half Step operation are shown in

Figure 7. The Power output stages of the MC33192 consist of two H–Bridges capable of driving two–phase bi–polar permanent magnet motors in either half or full step increment.

**Figure 5. Permanent Magnet Stepper Motor**



**Figure 6. 4–Step "Full Step" Operation**



#### **Figure 7. 8–Step "Half Step" Operation**



Permanent magnetic stepping motors exhibit the characteristic ability to hold a shaft rotor position with or without a stator coil being energized. Normally the shaft holding ability of the motor with a stator coil energized is referred to as "Holding Torque" while "Residual Torque" or "Detent Torque" refers to the shaft holding ability when a stator coil is not energized. The Holding Torque value is dependent on the interactive magnetic force created by the resulting energized stator fields with that of the permanent magnet rotor. The Residual Torque is a function of the physical size and composition of the permanent magnet rotor material coupled with its intrinsic magnetic attraction for the un–energized stator core material and as a result, the weaker of the two torques.

It is to be noted when using half step operation, only one coil is energized during alternate step periods which produces a somewhat weaker Holding Torque. Holding Torque is maximized when both coils are simultaneously energized. In addition, since each winding and resulting flux conditions are not perfectly matched for each half step, incremental accuracy is not as good as when full stepping.

#### **Two Phase Drive Signals**

The DIR1 and DIR2 bits in the Data Frame of the Push Field determine the direction of H–Bridge current flow, and thus the magnetic field polarization of the stator coils, for H–Bridge outputs "A" and "B" respectively. The directional signals DIR1 and DIR2, generated by the MCU, communicate over the MI–Bus to control the two H–Bridge power output stages of the MC33192 to drive two phase bipolar permanent magnet motors. Figure 8 shows the MC33192 truth table to accomplish incremental stepping of the motor in a clockwise or counter–clockwise direction in either half or full step modes. The stator field polarization and rotor position are also shown for reference relative to the basic stepper motor of Figure 5.

		Push Field Bits									٨		
Step		D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>		H-Bridge Outputs			Ð Stator Field	Rotor Position	Direction of Shaft
Full	Half	Inh1	DIR1	$\mathsf E$	DIR <sub>2</sub>	Inh <sub>2</sub>	A <sub>1</sub>	A2	B1	<b>B2</b>	(Note 2)	(Note 2)	Rotation
$\mathbf{1}$	$\mathbf{1}$	$\mathbf{1}$	$\pmb{0}$	$\overline{1}$	$\pmb{0}$	$\mathbf{1}$	$\overline{1}$	$\overline{\phantom{0}}^0$	$\mathbf{1}$	$\mathbf 0$	↖		CCW
$\qquad \qquad -$	$\overline{2}$	$\mathbf{1}$	$\pmb{0}$	$\mathbf{1}$	X	$\overline{0}$	$\mathbf{1}$	0	Z	$\mathsf Z$			
$\sqrt{2}$	$\mathbf{3}$	$\mathbf{1}$	$\mathsf{O}\xspace$	$\overline{1}$	$\overline{1}$	$\overline{\mathbf{1}}$	$\overline{1}$	$\pmb{0}$	$\pmb{0}$	$\mathbf{1}$	$\overline{\mathscr{M}}$	↙	
-	$\overline{4}$	$\overline{0}$	X	$\mathbf{I}$	$\overline{1}$	$\mathbf{1}$	Z	$\mathsf Z$	$\pmb{0}$	$\mathbf{1}$	,		
$\sqrt{3}$	$\sqrt{5}$	$\mathbf{1}$	$\uparrow$	$\overline{1}$	$\mathbf{1}$	$\mathbf{1}$	$\pmb{0}$	$\mathbf{1}$	$\pmb{0}$	$\mathbf{1}$			
$\overline{\phantom{0}}$	6	$\mathbf{1}$	$\mathbf{1}$	$\mathbf{1}$	Χ	$\mathbf 0$	$\pmb{0}$	$\mathbf{1}$	$\pmb{0}$	$\pmb{0}$			
$\overline{\mathbf{4}}$	$\overline{7}$	$\mathbf{1}$	$\mathbf{1}$	$\mathbf{1}$	$\pmb{0}$	$\mathbf{1}$	$\pmb{0}$	$\mathbf{1}$	$\mathbf{1}$	$\pmb{0}$	¥		CW
-	$\bf 8$	$\pmb{0}$	$\mathsf X$	$\overline{1}$	$\pmb{0}$	$\mathbf{1}$	$\mathsf Z$	$\mathsf Z$	$\mathbf{1}$	$\pmb{0}$			
		$\pmb{0}$	$\mathsf X$	$\mathsf X$	Χ	$\pmb{0}$	Z	$\mathsf Z$	$\mathsf Z$	Z			
		$\mathbf{1}$	$\mathbf{1}$	$\pmb{0}$	$\mathbf{1}$	$\mathbf{1}$	Z	$\mathbf{1}$	$\mathsf Z$	$\mathbf{1}$			
		$\mathbf{1}$	$\pmb{0}$	$\pmb{0}$	$\pmb{0}$	$\mathbf{1}$	$\mathbf{1}$	$\mathsf Z$	$\mathbf{1}$	$\mathsf Z$			
		$\mathbf{1}$	$\mathbf{1}$	$\pmb{0}$	$\pmb{0}$	$\pmb{0}$	Z	$\mathbf{1}$	$\mathsf Z$	Z			
		$\pmb{0}$	$\pmb{0}$	$\pmb{0}$	$\mathbf{1}$	$\mathbf{1}$	Z	Z	Ζ	$\mathbf{1}$			

**Figure 8. Truth Table and Serial Push Field Data Bits For Sequential Stepping**

**NOTES:**  $1 \times$  = Don't care;  $Z =$  High impedance;  $1 =$  High (active "on") state;  $0 =$  Low (inactive "off") state.

2. The stator field direction and position of the rotor are shown for explanation purposes and relative to the basic stepper motor shown in Figure 3.

3. DIR1 establishes the direction of current flow in H–Bridge "A".

4. DIR2 establishes the direction of current flow in H–Bridge "B".

#### **MI–Bus Interface Description**

The MI–Bus Interface shown in Figure 9 is made up of a single NPN transistor (Q1). The two main functions of this NPN transistor are:

1) To drive the MI–Bus during the Push Field with approximately 20 mA of current while also exhibiting low saturation characteristics (V<sub>CE(sat)</sub>).

2) To protect the Input/Output (I/O) pin of the MCU against any Electro–Magnetic Interference (EMI) captured on the bus wire.

Without the NPN transistor, the MCU could be destroyed as a result of receiving excessive EMI energy present on the bus. In addition, the transistor blocks the MCU from receiving EMI signals which could erroneously change the data direction register of the MCU I/O.

The MCU input pin (P<sub>in</sub>), used to read the Pull Field of the MI–Bus, is protected by two diodes (D2 and D3) and two resistors (R5 and R6). Any transient EMI generated voltage present on the bus is clamped by the two diodes to a windowed voltage value not to be greater than the V<sub>DD</sub> or less than the V<sub>SS</sub> supply voltages of the MCU.

#### **MI–Bus Levels**

The MI–Bus can have one of two valid logic states, recessive or dominant. The recessive state corresponds to a Logic "1" and is obtained through use of a 10 kΩ pull–up resistor (R9) to 5.0 V. The dominant state corresponds to a Logic "0" which represents a voltage less than 0.3 V and created by the VCE(sat) of Q1.

#### **MI–Bus Overvoltage Protection**

An external zener diode (Z1) is incorporated in the interface circuit so as to protect the MCU output pin  $(P_{\text{out}})$ from overvoltages commonly encountered in automotive applications as a result of "Load Dump" and "Jump Start" conditions. Load Dump is defined as the inductive transient generated on the battery line as a result of opening the battery connection while the alternator system is producing charge current. Jump Start overvoltages are the result of paralleling the installed automotive battery, through the use of "jumper cables", to an external voltage source in excess of the vehicles nominal system voltage. For 12 V automotive systems, it is common for 24 V "jump start" voltages to be used.

When an overvoltage situation (>18 V) exists, due to a load dump or jump start condition, the zener diode (Z1) is activated and supplies base current to turn on the NPN transistor Q1 causing the bus to be pulled to less than 0.3 V producing a Logic "0" on the MI–Bus. After a duration corresponding to  $8t<sub>S</sub>$  (200  $\mu$ s) of continuous Logic "0" on the bus all MC33192 devices will disable their outputs. Normal operation is resumed, following the overvoltage, by the MCU sending out a "standard" message instruction.

#### **MI–Bus Termination Network**

The MI-Bus is resistively loaded according to the number of MC33192 devices installed on the bus. Each MC33192 has an internal 10 kΩ pull–up resistor to 5.0 V. An external pull–up resistor (R7) is recommended to be used to optimally adjust termination of the bus for a load resistance of 600  $Ω$ .



#### **Figure 9. MI–Bus MCU Interface**

### **MESSAGE CODING**

#### **Bi–Phase Coding and Detection**

The Manchester Bi–Phase code shown in Figure 10 requires two time slots  $(2t<sub>s</sub>)$  to encode a single data bit. This allows detection of a single error at the time slot level. The logic levels "1" or "0" are determined by the organization of the two time slots. These always have complementary logic levels of either zero volts or plus five volts, which are detected using an Exclusive OR detection circuit during the Push Field sequence. A "1" bit is detected when the first time slot is set to a zero logic state (0 V) followed by the second time slot set to a logic state one (5.0 V). Conversely, a "0" bit is detected when the first time slot is set to the logic state "one" (5.0 V) followed by a second time slot set to a "zero" logic state (0 V). For these two bits are Exclusive–ORs of each other.

The addressed devices receiving the Push Field detect the Bi–Phase code. Bi–Phase detection involves the sampling of the Push Field Bi–Phase code twice (a and b) for each time slot. A code error occurs when the two time slots of the Bi–Phase do not follow a logical Exclusive–OR function (see Figure 10).

Noise monitoring is accomplished by sampling the Push Field Bi–Phase code twice (a and a') and (b and b') during each time slot. A noise error is detected if the two sample values do not have the same logical level.

**Figure 10. Noise/Bi–Phase Detection**



Each message frame consists of two fields: The Push Field, in which data and addresses are transferred by the MCU to the slave device; and the Pull Field, in which serial data is transferred back to the MCU from the address selected slave device. The message frame is broken down into seven individual field segments as indicated in Figure 4 (Start, Push Field Sync, Push Field Data, Push Field Address, Pull Field Sync, Pull Field Data, and End–of–Frame). The following lists the bit size and function of each of these segments:

1) **Start** is the start of message and consists of three time slots (3ts) having the dominant Logic "0" state of less than 0.3 V. Holding the MI-Bus at ground for three time slots  $(3t<sub>S</sub>)$ marks the beginning of the message frame by violating the law of the Manchester Code.

2) **Push Field Sync** is a single bit which establishes initial timing for the Push Field Data to follow.

3) **Push Field Data** is comprised of five serial data bit fields (D0, D1, D2, D3 and D4) which comprise the instruction set defining the configuration and condition of the two H–Bridge output stages.

4) **Push Field Address** is comprised of three serial data bit fields (A0, A1 and A2) which define the address or name of a MC33192 on the MI–Bus.

5) **Pull Field Sync** is a single bit which establishes the end of the Push Field and the initial start timing for the Pull Field Data to follow.

6) **Pull Field Data** is made up of three serial data bit fields (S2, S1 and S0) which contain the existing status information of an addressed MC33192.

7) **End–of–Frame** field is a signal which communicates to the MCU that the status information sent by the MC33192 is complete.

The Push Field Sync bit, Push Field Data bits, Push Field Address bits, Pull Field Sync bit are all coded by the Manchester Bi–Phase L Code. The Pull Field Data bits are Non–Return to Zero (NRZ) coded. The End–of Frame field is a square wave signal with a frequency of 20 kHz or higher so as to avoid a condition which causes a bus violation.

The Manchester Bi-Phase L code requires two time slots  $(2t<sub>s</sub>)$  to encode a single bit. This allows a single error to be detected during the time slot.

**Address Programming** involves the use of three instructions. Refer to Figure10.

**First Instruction** Set the MI–Bus continuously at 12 V. This places the MC33192 in the programming mode. Programming is possible only when the MI–Bus is at 12 V.

Next, the MCU serially enters "Logic Zeros" in all five Push Field Data bit positions (D0, D1, D2, D3 and D4) followed by the designated address value in the Push Field Address positions (A0, A1, & A2).

The MCU now waits 275 us before starting the second instruction. The total of the Pull time, Delay time, and Bus Violation time (V) of the second instruction (150  $\mu$ s, 275  $\mu$ s and 75 µs respectively) will cause the memory cell to be energized for 500 µs. During the first 150 µs of this time, the MCU is checking the Pull Field Data Bits S2, S1 and S0 looking for the **programming code "110"** to indicate complete activation of the memory cell.

**Second Instruction** (MI–Bus voltage remaining at 12 V) The MCU repeats the same Push Field instruction as previously sent in the First Instruction; entering all "Logic Zeros" in the Push Field Data positions followed by the designated Push Field Address value in the address positions.

Again, the MCU waits for the Pull, Delay, and Bus violation time while checking the Pull Field Data bits looking for the **programming code "110"** code. The MCU must repeat the initial Push Field Address instruction until a "110" code is received before advancing to the Third Instruction.

**Third Instruction** The MI–Bus voltage is lowered to 5.0 V. The MCU serially loads "Logic Zeros" in all five Push Field Data bit positions followed by the programmed address in the Push Field Address positions. The MCU then checks the Pull Field Address status bits looking this time for the

**programming OK code "100"** indicating the address programming to be executed.

The First and Second Instructions must be repeated until the MCU successfully receives the programming code "100". Address programming is not complete until a "100" OK status is received by the MCU with the MI–Bus voltage at 5.0 V.

**Overwrite–Bit Programming** involves the use of two instructions. See Figure 11.

**First Instruction** Have the MI–Bus continuously set at 12 V so as to have the MC33192 in the programming mode. Programming can only be accomplished with the MI–Bus at 12 V.

The MCU serially enters "Logic Zeros" for the Push Field Data bits D0, D1, D2 and D3 and a Logic "1" for D4 bit followed by the programmed address bits A0, A1 and A2.

The MCU now waits 275 us before starting the second instruction. The total of the Pull time, Delay time, and Bus Violation time (V) of the second instruction (150 µs, 275 µs and 75 µs respectively) will cause the memory cell to be energized for 500 µs. During the first 150 µs of this time, the MCU is checking the Pull Field Data Bits for the status of bits S2, S1 and S0 looking for the **programming code "110"** to indicate complete activation of the memory cell.

**Second Instruction** (MI–Bus remaining at 12 V)

The MCU repeats the first instruction outlined above until the **programming OK code "100"** is sent back to the MCU from the selected MC33192 indicating the overwrite–bit protection to be programmed. If after eight repeat instructions, the programming code "110" or the OK code "100" is not generated four times in succession, programming of the MC33192 has failed. If this occurs, the Overwrite–Bit Programming sequence should be reviewed and re–started from the beginning.

#### **H–Bridge Output**

The H–Bridge output drive circuit and associated diagnostic encoder are shown in Figure 12. The H–Bridge output uses internal diode clamps (D1, D2, D3, D4) to provide transient protection of the output transistors necessary when switching inductive loads associated with stepper motors.

#### **Back EMF Detection**

Three different Back EMF currents can occur depending on whether the motor is running or manner in which it is being stopped. Referring to Figure 12; When the Dir1 bit is set to logic 0, the direction of current flow will be from V<sub>CC</sub> through transistor Q2, Coil A (A1 to A2), and transistor Q4 to ground.

1) **Fast Decay** (when transistors Q1, Q2, Q3 and Q4 are switched off).

When the current flowing in the coil is stopped by setting the Inh1 bit to logic 0, the back EMF current will circulate through the voltage supply ( $V_{\text{CC}}$ ) and diodes D1 and D3. At that time, the voltage developed across the diode D1 is detected by transistor Q6. The generated voltage pulse of Q6 is then encoded and sent, in the Pull–Field, to the microprocessor.

2) **Slow Decay** (Q3 and Q4 are switched off)

When the current flowing in the coil is stopped by setting the E bit to logic 0, the back EMF current will circulate through the diode D1 and transistor Q2 which is already switched on. 3) **When Motor is Running**

The rotational direction of the motor changes whenever the Dir bit state is changed. When the Dir bit is changed from a logic 0 to a logic 1, transistors Q2 and Q4 are switched off and transistors Q1 and Q3 are switched on. At this time, the back EMF current will circulate from ground through diodes D1 and D3 to the voltage supply ( $V_{\text{CC}}$ ). In all cases, the back EMF currents will be detected by transistors Q5 and Q6.



**Figure 11. Address Programming Diagram**



## **Figure 12. H–Bridge Output Drive Circuit and Diagnostic Encoder**



### **Figure 13. Single Wire MI–Bus Control of 8 Stepper Motors**

#### **OUTLINE DIMENSIONS**



Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding<br>the suitability of its products for any particular purpose, nor d specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that<br>Motorola was negligent regarding the design or manufacture Opportunity/Affirmative Action Employer.

**How to reach us:<br>USA/EUROPE/Locations Not Listed: Motorola Literature Distribution:** P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447 or 602–303–5454 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center,

**MFAX**: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609 **ASIA/PACIFIC**: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298



