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MOTOROLA

MC34065
MC33065

High Performance Dual Channel Current Mode Controller

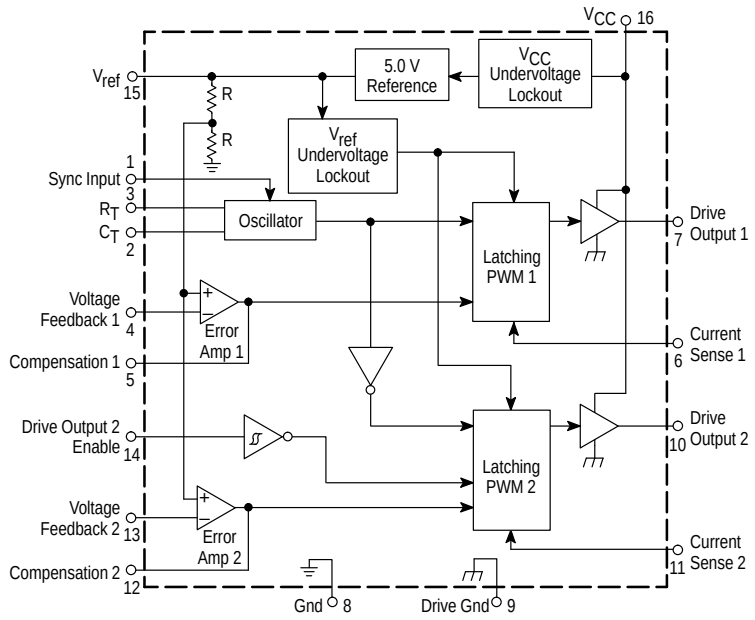
The MC34065 is a high performance, fixed frequency, dual current mode controllers. It is specifically designed for off–line and dc–to–dc converter applications offering the designer a cost effective solution with minimal external components. This integrated circuit feature a unique oscillator for precise duty cycle limit and frequency control, a temperature compensated reference, two high gain error amplifiers, two current sensing comparators, Drive Output 2 Enable pin, and two high current totem pole outputs ideally suited for driving power MOSFETs.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle–by–cycle current limiting, and a latch for single pulse metering of each output.

The MC34065 and MC33065 are available in dual–in–line and surface mount packages.

- Unique Oscillator for Precise Duty Cycle Limit and Frequency Control
- Current Mode Operation to 500 kHz
- Automatic Feed Forward Compensation
- Separate Latching PWMs for Cycle–By–Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- Drive Output 2 Enable Pin
- Two High Current Totem Pole Outputs
- Input Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current

Representative Block Diagram

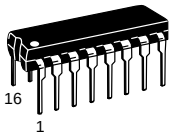


This device contains 208 active transistors.

HIGH PERFORMANCE DUAL CHANNEL CURRENT MODE CONTROLLER

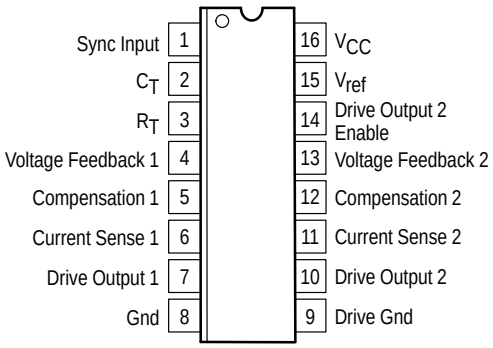
SEMICONDUCTOR TECHNICAL DATA

P SUFFIX
PLASTIC PACKAGE
CASE 648



DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO–16L)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34065DW	T_A = 0° to +70°C	SO–16L
MC34065P		Plastic DIP
MC33065DW	T_A = –40° to +85°C	SO–16L
MC33065P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	50	mA
Output Current, Source or Sink (Note 1)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense, Enable, and Voltage Feedback Inputs	V_{in}	–0.3 to +5.5	V
Sync Input High State (Voltage) Low State (Reverse Current)	 V_{IH} I_{IL}	 5.5 –5.0	 V mA
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics DW Suffix, Plastic Package Case 751G Maximum Power Dissipation @ T_A = 25°C Thermal Resistance, Junction–to–Air P Suffix, Plastic Package Case 648 Maximum Power Dissipation @ T_A = 25°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 862 145 1.25 100	 mW °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature MC34065 MC33065	T_A	 0 to +70 –40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 8.2 kΩ, C_T = 3.3 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3].)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.9	5.0	5.1	V
Line Regulation (V_{CC} = 11 V to 15 V)	Reg_{line}	–	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	–	3.0	25	mV
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.85	–	5.15	V
Output Short Circuit Current	I_{SC}	30	100	–	mA
OSCILLATOR AND PWM SECTIONS					
Total Frequency Variation over Line and Temperature V_{CC} = 11 V to 15 V, T_A = T_{low} to T_{high} MC34065 MC33065	f_{osc}	 46.5 45	 49 49	 51.5 53	kHz
Frequency Change with Voltage (V_{CC} = 11 V to 15 V)	$\Delta f_{osc}/\Delta V$	–	0.2	1.0	%
Duty Cycle at each Output Maximum Minimum	 DC_{max} DC_{min}	 46 –	 49.5 –	 52 0	%
Sync Input Current High State (V_{in} = 2.4 V) Low State (V_{in} = 0.8 V)	 I_{IH} I_{IL}	 – –	 170 80	 250 160	μA

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the startup threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible:
T_{low} = 0°C for the MC34065 T_{high} = +70°C for MC34065
T_{low} = –40°C for the MC33065 T_{high} = +85°C for MC33065
4. This parameter is measured at the latch trip point with V_{FB} = 0 V
5. Comparator gain is defined as $AV = \frac{\Delta V \text{ Compensation}}{\Delta V \text{ Current Sense}}$

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 15 V [Note 2], R_T = 8.2 kΩ, C_T = 3.3 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3].)

Characteristics	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIERS					
Voltage Feedback Input (V_O = 2.5 V)	V_{FB}	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 5.0 V)	I_{IB}	–	– 0.1	–1.0	µA
Open Loop Voltage Gain (V_O = 2.0 to 4.0 V)	A_{VOL}	65	100	–	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	–	MHz
Power Supply Rejection Ratio (V_{CC} = 11 V to 15 V)	PSRR	60	90	–	dB
Output Current Source (V_O = 3.0 V, V_{FB} = 2.3 V) Sink (V_O = 1.2 V, V_{FB} = 2.7 V)	 I_{source} I_{sink}	 –0.45 2.0	 –1.0 12	 – –	mA
Output Voltage Swing High State (R_L = 15 k to ground, V_{FB} = 2.3 V) Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)	 V_{OH} V_{OL}	 5.0 –	 6.2 0.8	 – 1.1	V
CURRENT SENSE SECTION					
Current Sense Input Voltage Gain (Notes 4 and 5)	A_V	2.75	3.0	3.25	V/V
Maximum Current Sense Input Threshold (Note 4)	V_{th}	430	480	530	mV
Input Bias Current	I_{IB}	–	–2.0	–10	µA
Propagation Delay (Current Sense Input to Output)	$t_{PLN(In/Out)}$	–	150	300	ns
DRIVE OUTPUT 2 ENABLE PIN					
Enable Pin Voltage High State (Output 2 Enabled) Low State (Output 2 Disabled)	 V_{IH} V_{IL}	 3.5 0	 – –	 V_{ref} 1.5	V
Low State Input Current (V_{IL} = 0 V)	I_{IB}	100	250	400	µA
DRIVE OUTPUTS					
Output Voltage Low State (I_{sink} = 20 mA) (I_{sink} = 200 mA) High State (I_{source} = 20 mA) (I_{source} = 200 mA)	 V_{OL} V_{OH} 	 – – 13 12	 0.1 1.6 13.5 13.4	 0.4 2.5 – –	V
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{sink} = 1.0 mA)	$V_{OL(UVLO)}$	–	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF)	t_r	–	28	150	ns
Output Voltage Fall Time (C_L = 1.0 nF)	t_f	–	25	150	ns
UNDERVOLTAGE LOCKOUT SECTION					
Startup Threshold	V_{th}	13	14	15	V
Minimum Operating Voltage After Turn–On	$V_{CC(min)}$	9.0	10	11	V
TOTAL DEVICE					
Power Supply Current Startup (V_{CC} = 12 V) Operating (Note 2)	I_{CC} 	 – –	 0.6 20	 1.0 25	mA
Power Supply Zener Voltage (I_{CC} = 30 mA)	V_Z	15.5	17	19	V

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the startup threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible:
T_{low} = 0°C for the MC34065 T_{high} = +70°C for MC34065
T_{low} = –40°C for the MC33065 T_{high} = +85°C for MC33065
4. This parameter is measured at the latch trip point with V_{FB} = 0 V
5. Comparator gain is defined as $AV = \frac{\Delta V \text{ Compensation}}{\Delta V \text{ Current Sense}}$

PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	Sync Input	A narrow rectangular waveform applied to this input will synchronize the oscillator. A dc voltage within the range of 2.4 V to 5.5 V will inhibit the oscillator.
2	C_T	Timing capacitor C_T connects from this pin to ground setting the free–running oscillator frequency range.
3	R_T	Resistor R_T connects from this pin to ground precisely setting the charge current for C_T. R_T must be between 4.0 k and 16 k.
4	Voltage Feedback 1	This pin is the inverting input of Error Amplifier 1. It is normally connected to the switching power supply output through a resistor divider.
5	Compensation 1	This pin is the output of Error Amplifier 1 and is made available for loop compensation.
6	Current Sense 1	A voltage proportional to the inductor current is connected to this input. PWM 1 uses this information to terminate conduction of output switch Q1.
7	Drive Output 1	This pin directly drives the gate of a power MOSFET Q1. Peak currents up to 1.0 A are sourced and sunk by this pin.
8	Gnd	This pin is the control circuitry ground return and is connected back to the source ground.
9	Drive Gnd	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
10	Drive Output 2	This pin directly drives the gate of a power MOSFET Q2. Peak currents up to 1.0 A are sourced and sunk by this pin.
11	Current Sense 2	A voltage proportional to inductor current is connected to this input. PWM 2 uses this information to terminate conduction of output switch Q2.
12	Compensation 2	This pin is the output of Error Amplifier 2 and is made available for loop compensation.
13	Voltage Feedback 2	This pin is the inverting input of Error Amplifier 2. It is normally connected to the switching power supply output through a resistor divider.
14	Drive Output 2 Enable	A logic low at this input disables Drive Output 2.
15	V_{ref}	This is the 5.0 V reference output. It can provide bias for any additional system circuitry.
16	V_{CC}	This pin is the positive supply of the control IC. The minimum operating voltage range after startup is 11 V to 15.5 V.

Figure 1. Timing Resistor versus Oscillator Frequency

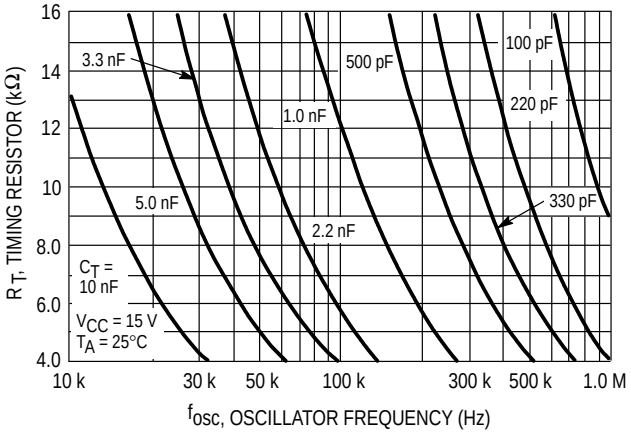


Figure 2. Maximum Output Duty Cycle versus Oscillator Frequency

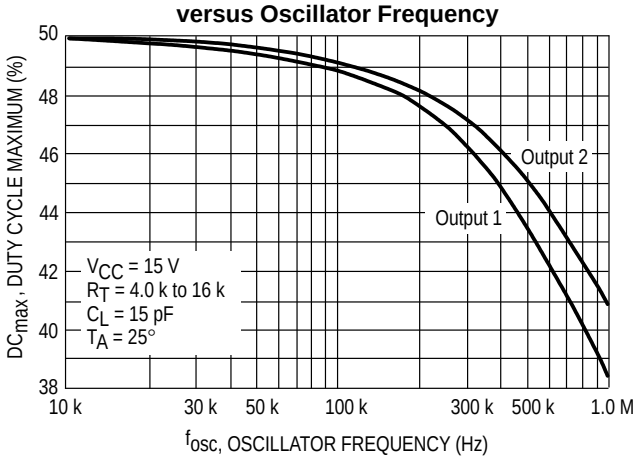


Figure 3. Error Amp Small–Signal Transient Response

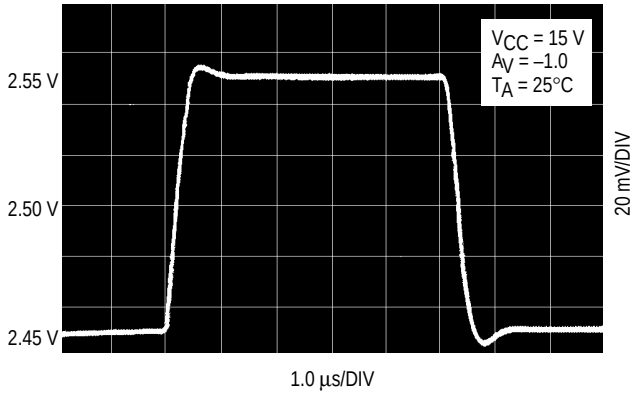


Figure 4. Error Amp Large–Signal Transient Response

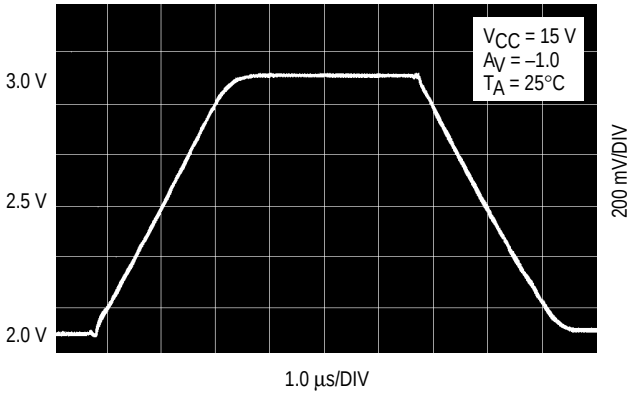


Figure 5. Error Amp Open Loop Gain and Phase versus Frequency

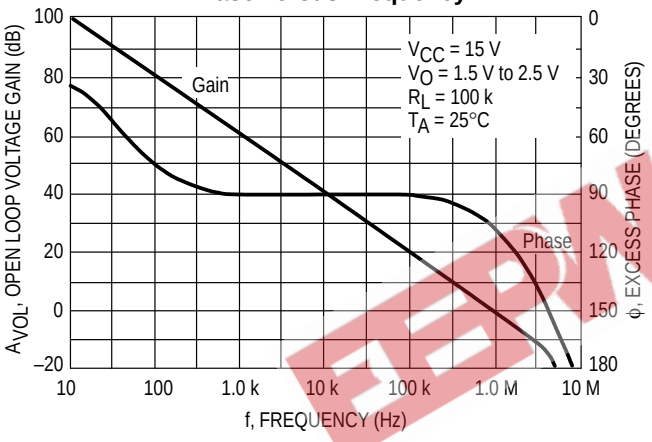


Figure 6. Current Sense Input Threshold versus Error Amp Output Voltage

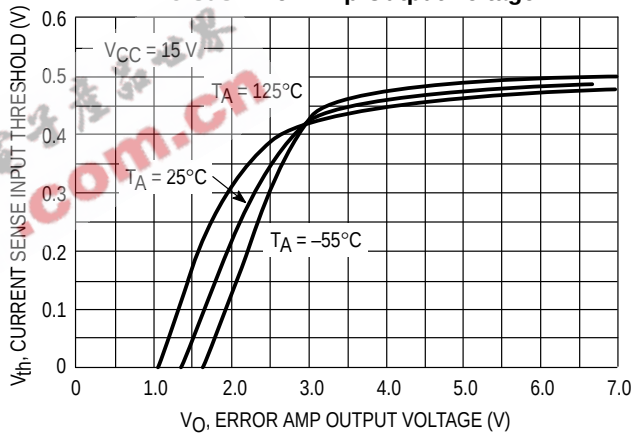


Figure 7. Reference Voltage Change versus Source Current

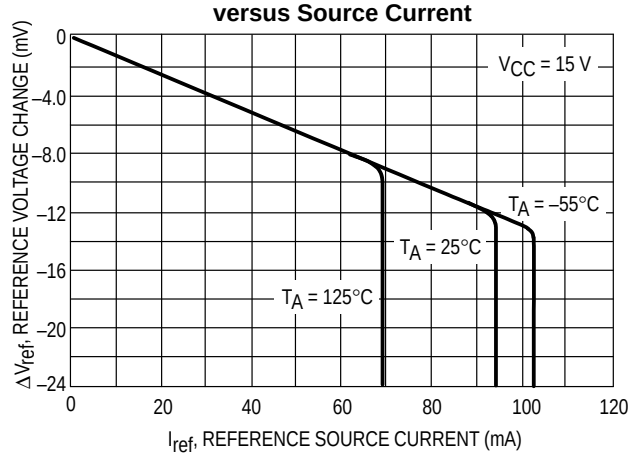


Figure 8. Reference Short Circuit Current versus Temperature

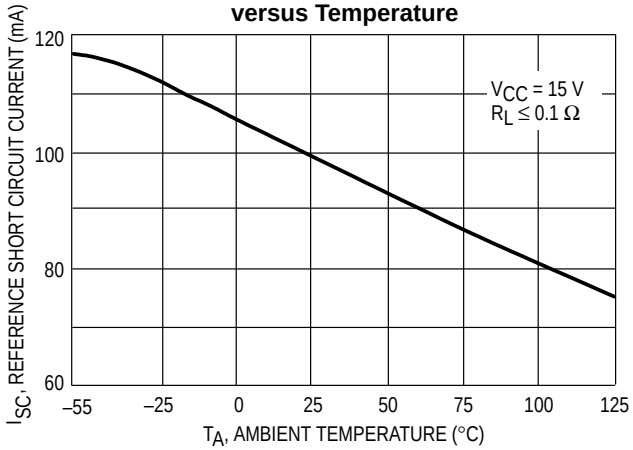


Figure 9. Reference Load Regulation

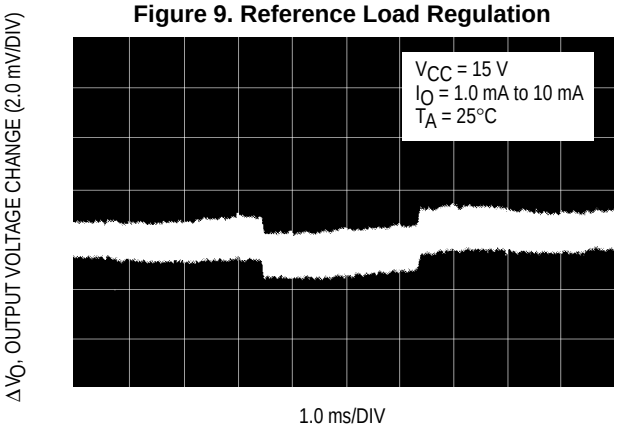


Figure 10. Reference Line Regulation

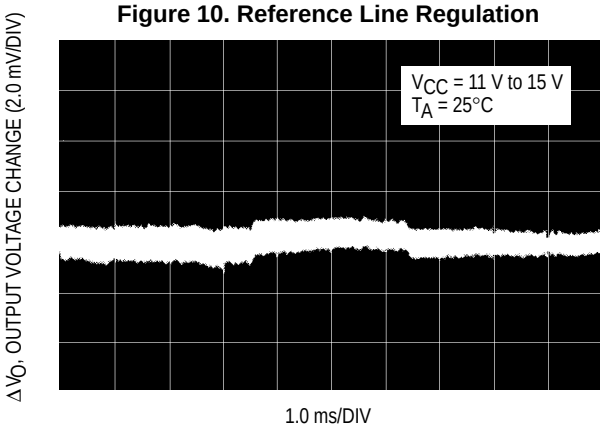


Figure 11. Output Saturation Voltage versus Load Current

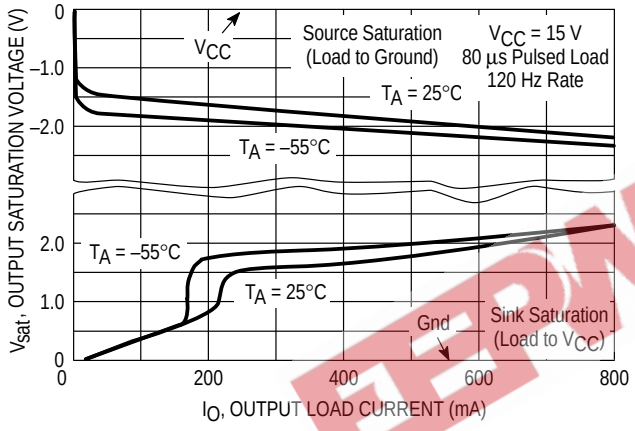


Figure 12. Output Waveform

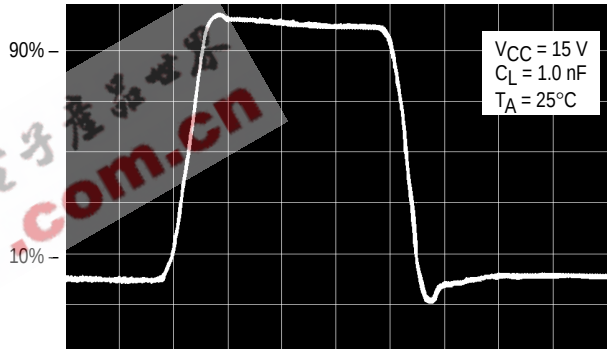


Figure 13. Output Cross Conduction Current

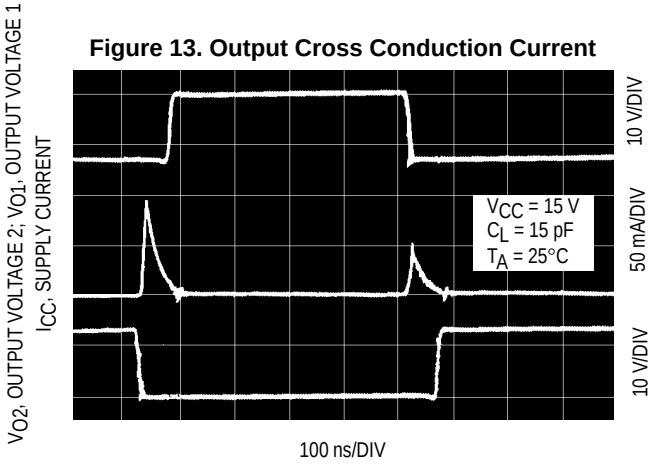
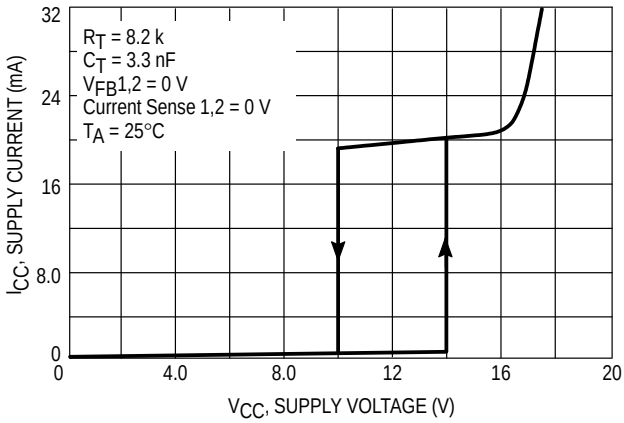


Figure 14. Supply Current versus Supply Voltage



OPERATING DESCRIPTION

The MC34065 series are high performance, fixed frequency, dual channel current mode controllers specifically designed for Off–Line and dc–to–dc converter applications. These devices offer the designer a cost effective solution with minimal external components where independent regulation of two power converters is required. The Representative Block Diagram is shown in Figure 15. Each channel contains a high gain error amplifier, current sensing comparator, pulse width modulator latch, and totem pole output driver. The oscillator, reference regulator, and undervoltage lock–out circuits are common to both channels.

Oscillator

The unique oscillator configuration employed features precise frequency and duty cycle control. The frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged and discharged by an equal magnitude internal current source and sink, generating a symmetrical 50 percent duty cycle waveform at Pin 2. The oscillator peak and valley thresholds are 3.5 V and 1.6 V respectively. The source/sink current magnitude is controlled by resistor R_T. For proper operation over temperature it must be in the range of 4.0 kΩ to 16 kΩ as shown in Figure 1.

As C_T charges and discharges, an internal blanking pulse is generated that alternately drives the center inputs of the upper and lower NOR gates high. This, in conjunction with a precise amount of delay time introduced into each channel, produces well defined non–overlapping output duty cycles. Output 2 is enabled while C_T is charging, and Output 1 is enabled during the discharge. Figure 2 shows the Maximum Output Duty Cycle versus Oscillator Frequency. Note that even at 500 kHz, each output is capable of approximately 44% on–time, making this controller suitable for high frequency power conversion applications.

In many noise sensitive applications it may be desirable to frequency–lock the converter to an external system clock. This can be accomplished by applying a clock signal as shown in Figure 17. For reliable locking, the free–running oscillator frequency should be set about 10% less than the clock frequency. Referring to the timing diagram shown in Figure 16, the rising edge of the clock signal applied to the Sync input, terminates charging of C_T and Drive Output 2 conduction. By tailoring the clock waveform symmetry, accurate duty cycle clamping of either output can be achieved. A circuit method for this, and multi–unit synchronization, is shown in Figure 18.

Error Amplifier

Each channel contains a fully–compensated Error Amplifier with access to the inverting input and output. The amplifier features a typical dc voltage gain of 100 dB, and a unity gain bandwidth of 1.0 MHz with 71° of phase margin (Figure 5). The noninverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input through a resistor divider. The maximum input bias current is –1.0 μA which will cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp output (Pin 5, 12) is provided for external loop compensation. The output voltage is offset by two diode drops (≈1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no pulses appear at the Drive Output (Pin 7, 10) when the error amplifier output is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft–start interval (Figures 20, 21).

The minimum allowable Error Amp feedback resistance is limited by the amplifier's source current (0.5 mA) and the output voltage (V_{OH}) required to reach the comparator's 0.5 V clamp level with the inverting input at ground. This condition happens during initial system startup or when the sensed output is shorted:

$$R_{f(min)} \approx \frac{3.0\ (0.5\ V)\ +\ 1.4\ V}{0.5\ mA} = 5800\ \Omega$$

Current Sense Comparator and PWM Latch

The MC34065 operates as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier output. Thus the error signal controls the peak inductor current on a cycle–by–cycle basis. The Current Sense Comparator–PWM Latch configuration used ensures that only a single pulse appears at the Drive Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting a ground–referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 6, 11) and compared to a level derived from the Error Amp output. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 5, 12 where:

$$I_{pk} = \frac{V_{(Pin\ 5,\ 12)} - 1.4\ V}{3\ R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 0.5 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{0.5\ V}{R_S}$$

When designing a high power switching regulator it may be desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 19. The two external diodes are used to compensate the internal diodes, yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense input with a time constant that approximates the spike duration will usually eliminate the instability, refer to Figure 24.

Figure 15. Representative Block Diagram

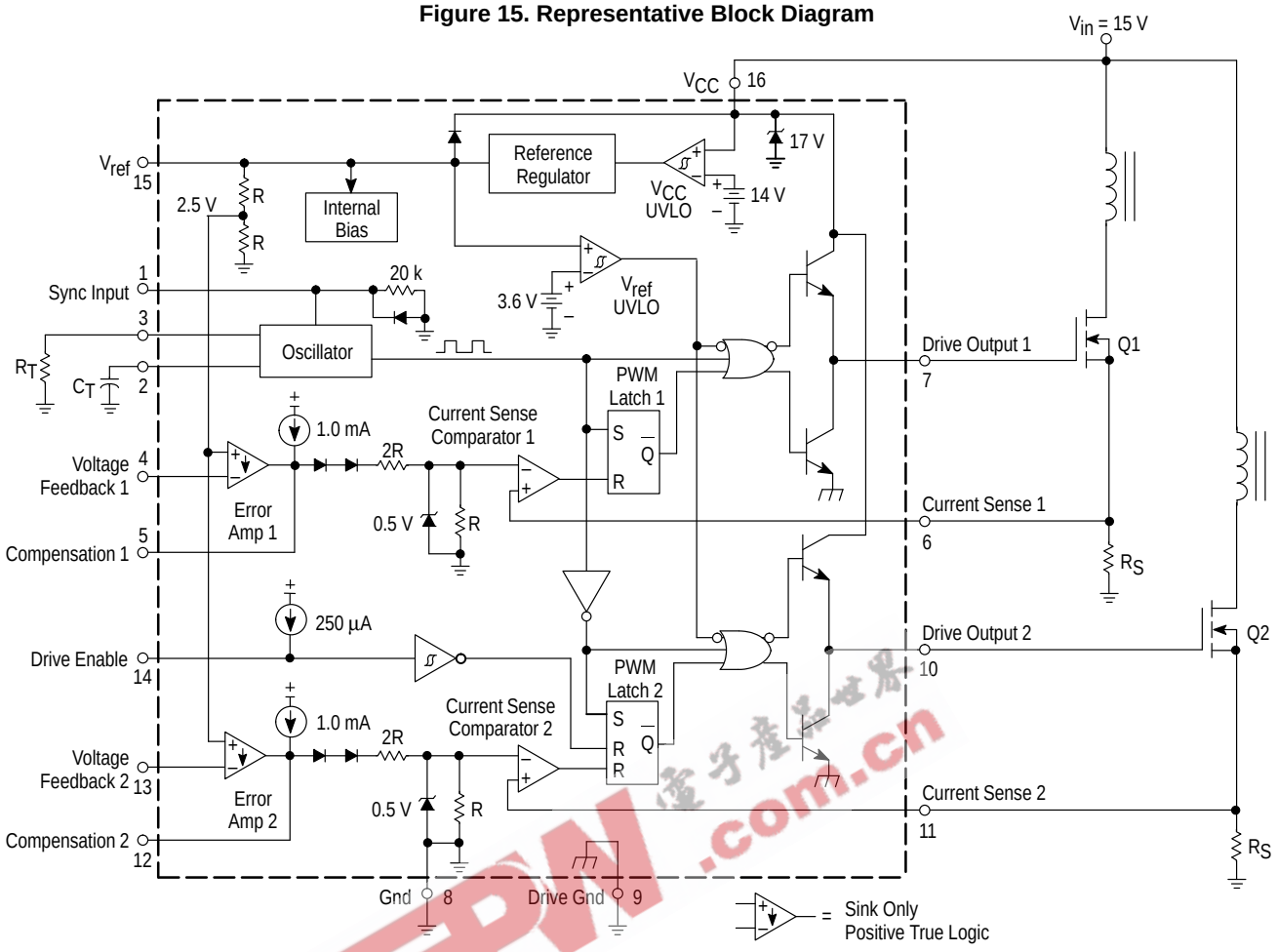
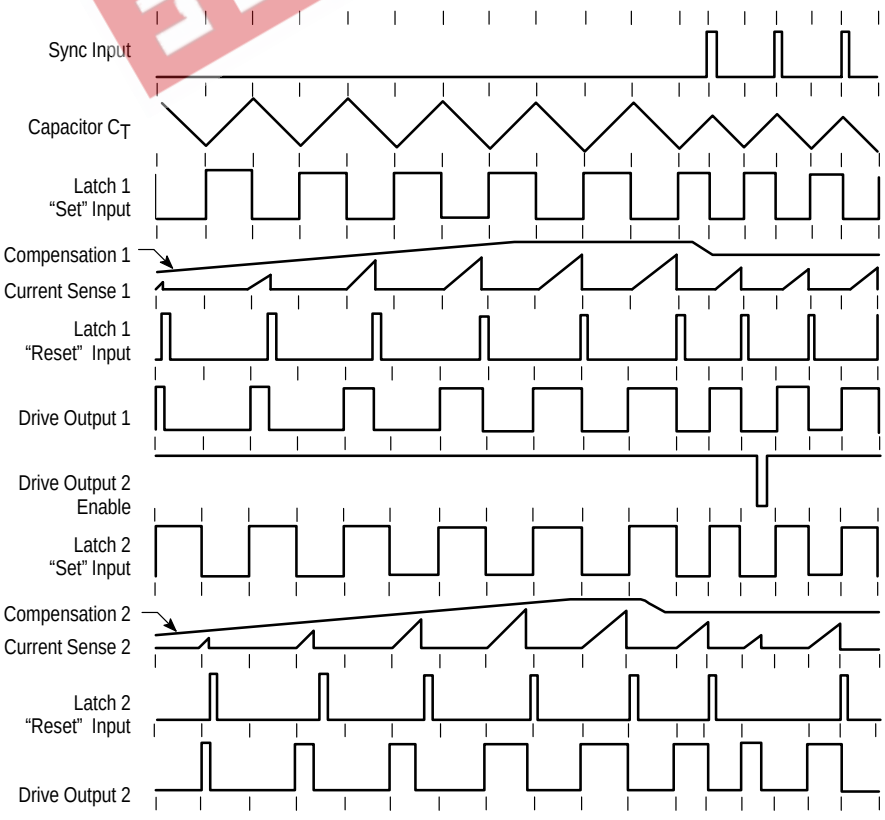


Figure 16. Timing Diagram



Undervoltage Lockout

Two Undervoltage Lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stages are enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built–in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 14 V and 10 V respectively. The hysteresis and low startup current makes these devices ideally suited to off–line converter applications where efficient bootstrap startup techniques are required (Figure 28). The V_{ref} comparator disables the Drive Outputs until the internal circuitry is functional. This comparator has upper and lower thresholds of 3.6 V and 3.4 V. A 17 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC and power MOSFET gate from excessive voltage that can occur during system startup. The guaranteed minimum operating voltage after turn–on is 11 V.

Drive Outputs and Drive Ground

Each channel contains a single totem–pole output stage that is specifically designed for direct drive of power MOSFETs. The Drive Outputs are capable of up to ±1.0 A peak current with a typical rise and fall time of 28 ns with a 1.0 nF load. Internal circuitry has been added to keep the outputs in a sinking mode whenever an Undervoltage Lockout is active. This characteristic eliminates the need for an external pull–down resistor. Cross–conduction current in the totem–pole output stage has been minimized for high speed operation, as shown in Figure 13. The average added power due to cross–conduction with V_{CC} = 15 V is only 60 mW at 500 kHz.

Although the Drive Outputs were optimized for MOSFETs, they can easily supply the negative base current required by bipolar NPN transistors for enhanced turn–off (Figure 25). The outputs do not contain internal current limiting, therefore an external series resistor may be required to prevent the peak output current from exceeding the 1.0 A maximum rating. The sink saturation (V_{OL}) is less than 0.4 V at 100 mA.

A separate Drive Ground pin is provided and, with proper implementation, will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. Figure 23 shows the proper ground connections required for current sensing power MOSFET applications.

Drive Output 2 Enable Pin

This input is used to enable Drive Output 2. Drive Output 1 can be used to control circuitry that must run continuously such as volatile memory and the system clock, or a remote controlled receiver, while Drive Output 2 controls the high power circuitry that is occasionally turned off.

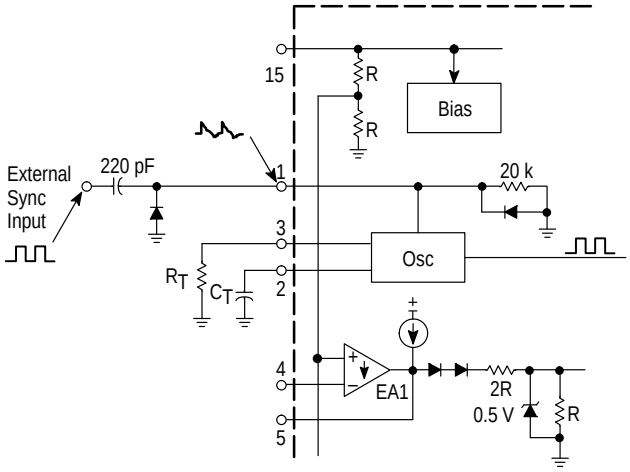
Reference

The 5.0 V bandgap reference is trimmed to ±2.0% tolerance at T_J = 25°C. The reference has short circuit protection and is capable of providing in excess of 30 mA for powering any additional control system circuitry.

Design Considerations

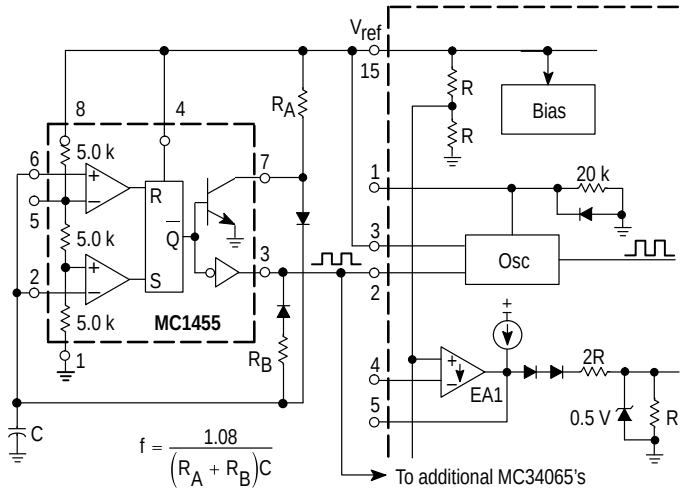
Do not attempt to construct the converter on wire–wrap or plug–in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse–width jitter. This is usually caused by excessive noise pick–up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low current signal and high current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 µF) connected directly to V_{CC} and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage–divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

Figure 17. External Clock Synchronization



The external diode clamp is required if the negative Sync current is greater than –5.0 mA.

Figure 18. External Duty Cycle Clamp and Multi–Unit Synchronization

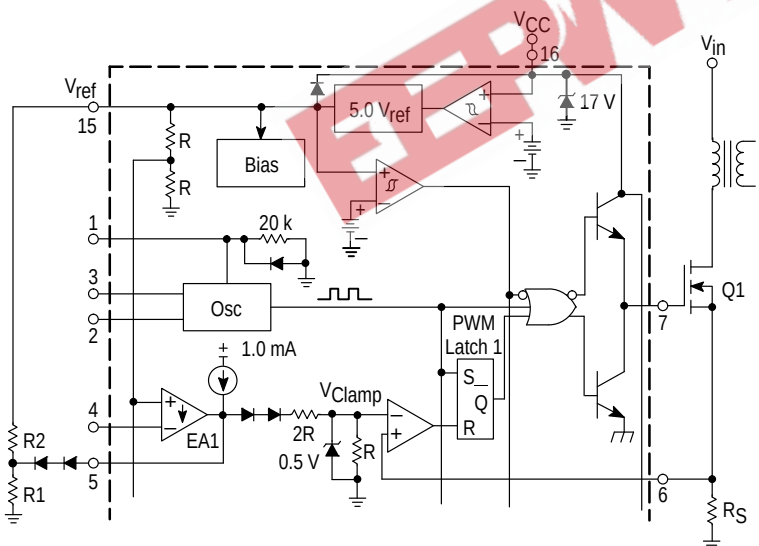


$$f = \frac{1.08}{(R_A + R_B)C}$$

$$D_{max}\ \text{Drive Output 1} = \frac{R_B}{R_A + R_B}$$

$$D_{max}\ \text{Drive Output 2} = \frac{R_A}{R_A + R_B}$$

Figure 19. Adjustable Reduction of Clamp Level

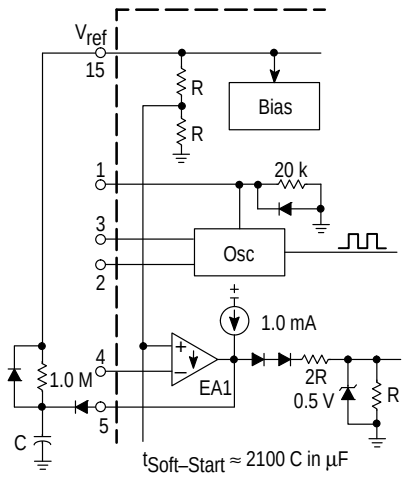


$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R2}{R1} + 1\right)} + 0.33 \times 10^{-3}\left(\frac{R1R2}{R1 + R2}\right)$$

$$I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

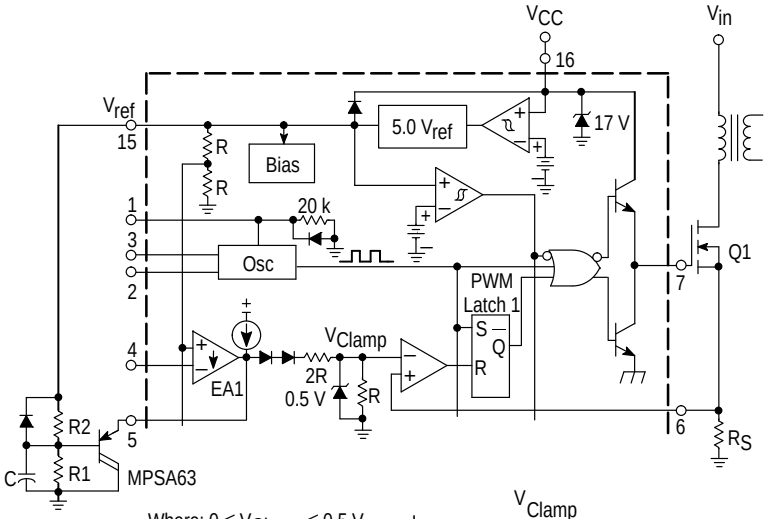
Where: $0 \le V_{Clamp} \le 0.5\ V$

Figure 20. Soft–Start Circuit



$$t_{Soft\text{–}Start} \approx 2100\ C\ \text{in}\ \mu F$$

Figure 21. Adjustable Reduction of Clamp Level with Soft–Start



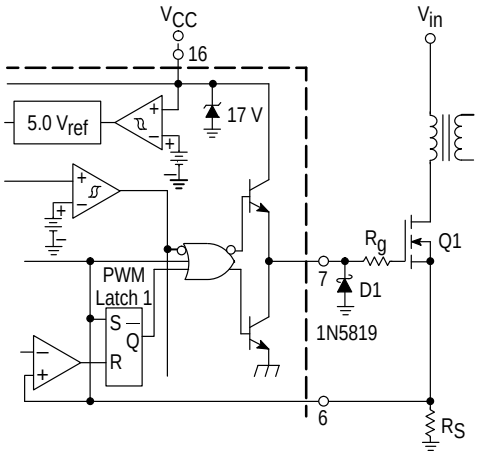
Where: $0 \le V_{Clamp} \le 0.5\ V$

$$I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R2}{R1} + 1\right)}$$

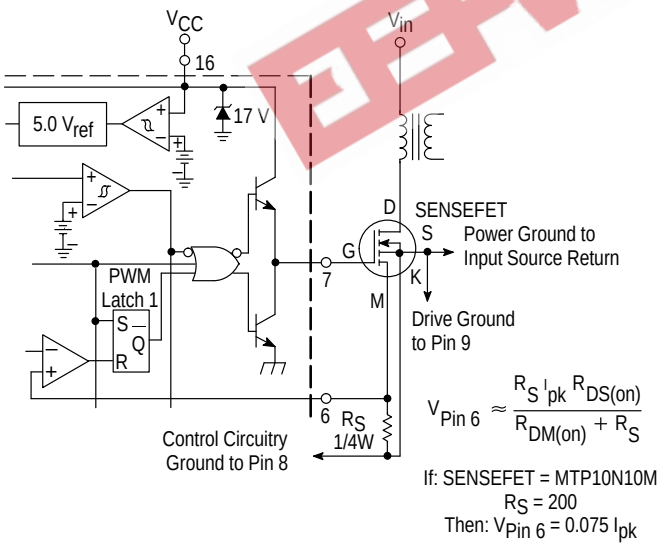
$$t_{Soft\text{–}Start} = \ln\left(\frac{1}{1 - \frac{V_C}{3\ V_{Clamp}}}\right) C\ \frac{R1R2}{R1 + R2}$$

Figure 22. MOSFET Parasitic Oscillations



Series gate resistor R_g may be needed to damp high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate–source circuit. R_g will decrease the MOSFET switching speed. Schottky diode D1 is required if circuit ringing drives the output pin below ground.

Figure 23. Current Sensing Power MOSFET

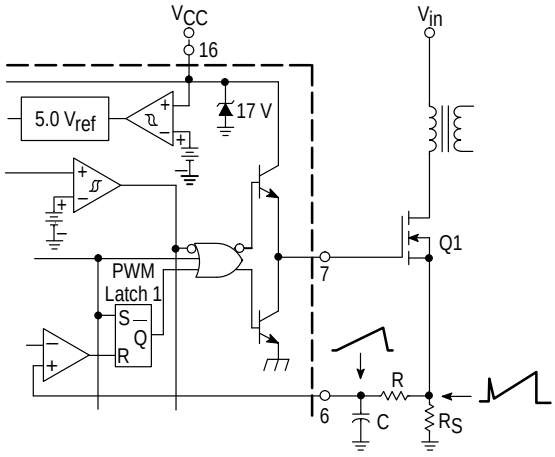


$$V_{Pin\ 6} \approx \frac{R_S\, I_{pk}\, R_{DS(on)}}{R_{DM(on)} + R_S}$$

If: SENSEFET = MTP10N10M
$R_S = 200$
Then: $V_{Pin\ 6} = 0.075\ I_{pk}$

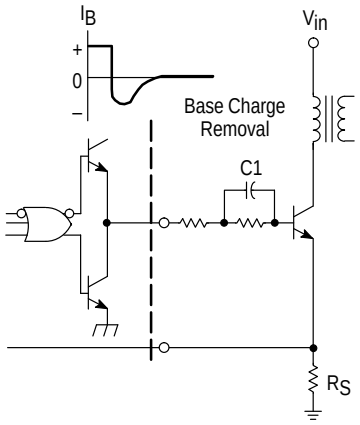
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation during over current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 19 and 21.

Figure 24. Current Waveform Spike Suppression



The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 25. Bipolar Transistor Drive



The totem–pole outputs can furnish negative base current for enhanced transistor turn–off, with the addition of capacitor C1.

Figure 26. Isolated MOSFET Drive

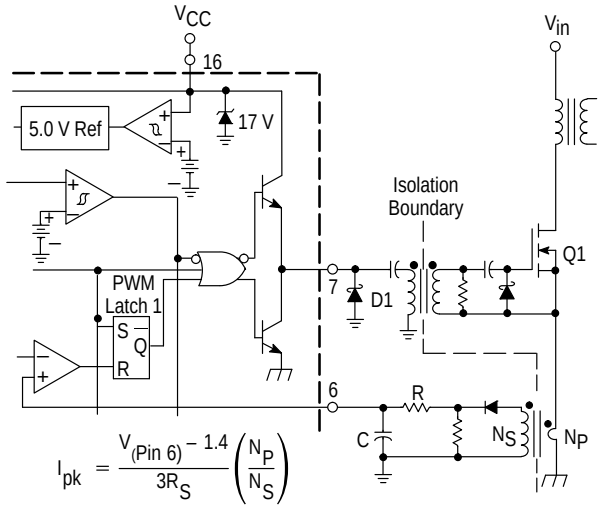
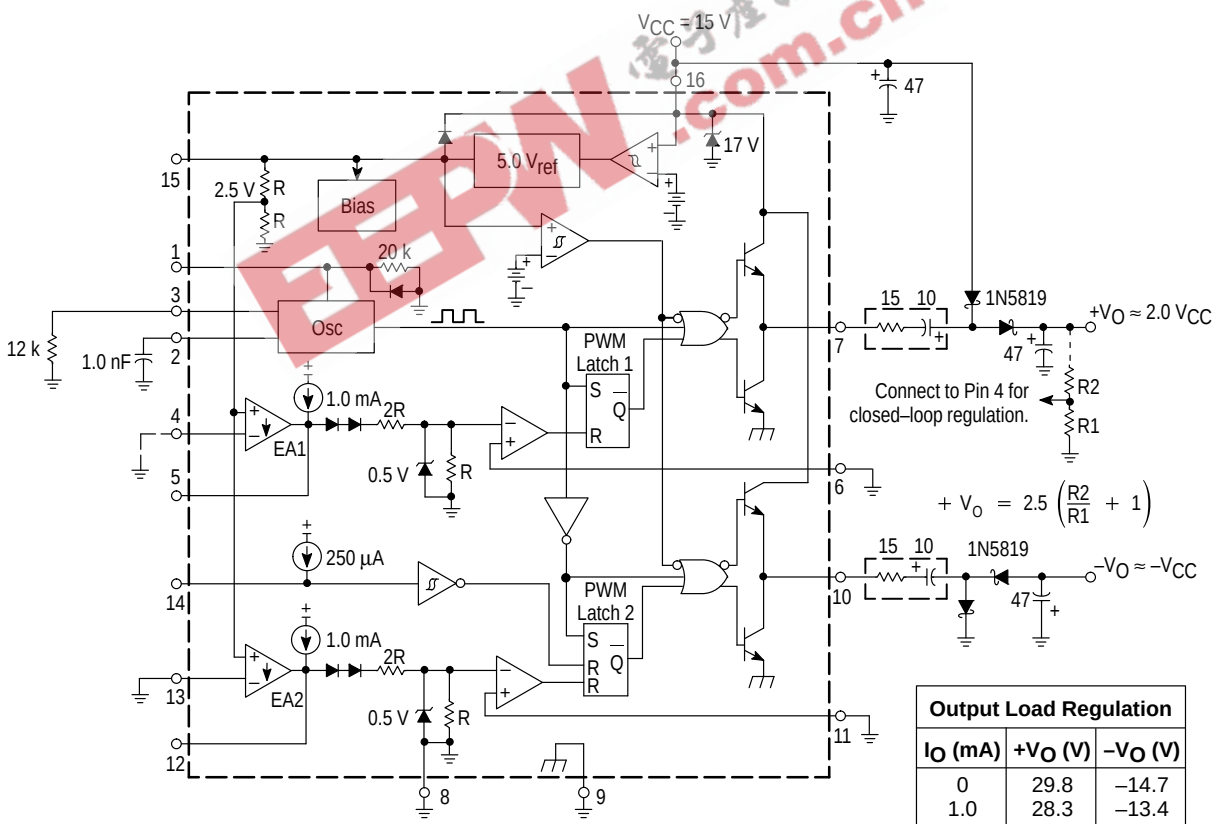


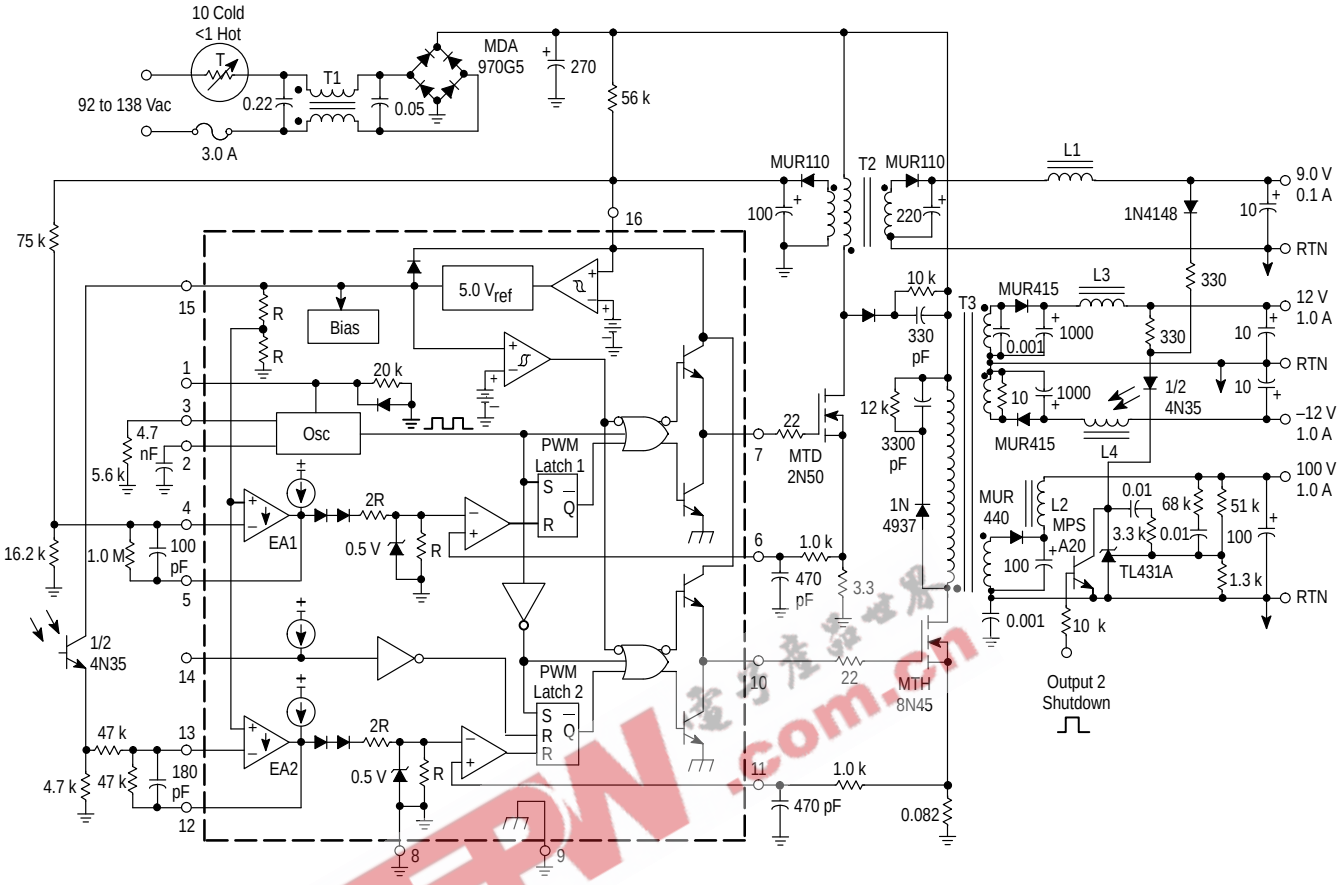
Figure 27. Dual Charge Pump Converter



Output Load Regulation		
I_O (mA)	$+V_O$ (V)	$-V_O$ (V)
0	29.8	–14.7
1.0	28.3	–13.4
5.0	27.9	–12.9
10	27.5	–12.5
50	24.4	–9.5

The capacitor's equivalent series resistance must limit the Drive Output current to 1.0 A. An additional series resistor may be required when using tantalum or other low ESR capacitors. The positive output can provide excellent line and load regulation by connecting the R2/R1 resistor divider as shown.

Figure 28. 125 Watt Off–Line Converter



Test	Conditions	Results
Line Regulation 100 V Output ±12 V Outputs 9.0 V Output	V_{in} = 92 to 138 Vac I_O = 1.0 A I_O = ±1.0 A I_O = 0.1 A	 Δ = 40 mV or ±0.02% Δ = 32 mV or ±0.13% Δ = 55 mV or ±0.31%
Load Regulation 100 V Output ±12 V Outputs 9.0 V Output	V_{in} = 115 Vac I_O = 0.25 A to 1.0 A I_O = ±0.25 A to ±1.0 A I_O = 0.08 A to 0.1 A	 Δ = 50 mV or ±0.025% Δ = 320 mV or ±1.2% Δ = 234 mV or ±1.3%
Output Ripple 100 V Output ±12 V Outputs 9.0 V Output	V_{in} = 115 Vac I_O = 1.0 A I_O = ±1.0 A I_O = 0.1 A	 40 mVpp 100 mVpp 60 mVpp
Short Circuit Current 100 V Output ±12 V Outputs 9.0 V Output	V_{in} = 115 Vac, R_L = 0.1 Ω	 4.3 A 17 A Output Hiccups
Efficiency	Vin = 115 Vac, PO = 125 W	86%

T1 – 468 µH per section at 2.5 A, Coilcraft E3496A.

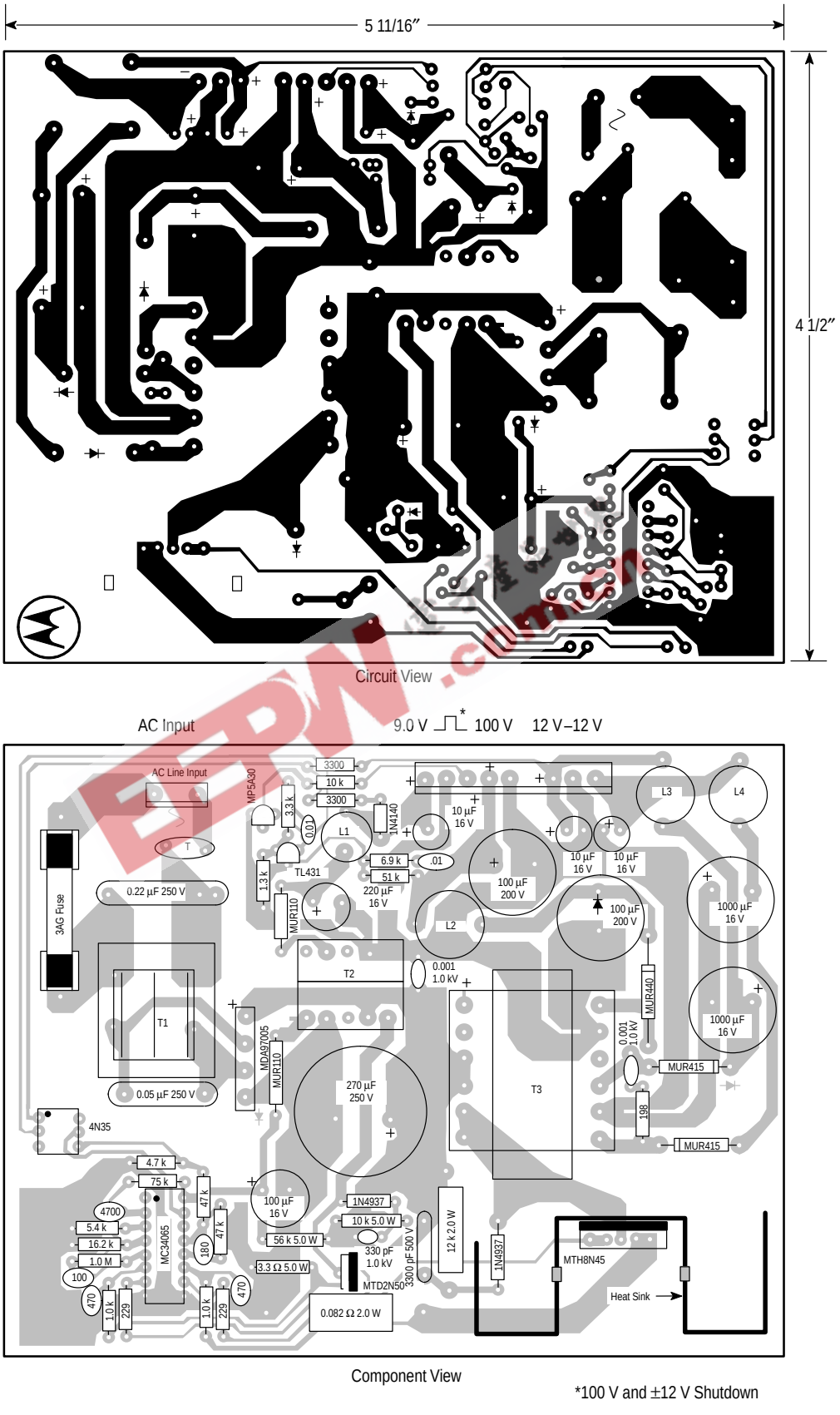
T2 – Primary: 156 Turns, #34 AWG
Primary Feedback: 19 Turns, #34 AWG
Secondary: 17 Turns, #28 AWG
Core: TDK H7C1EE22–Z
Bobbin: BE22–6H
Gap: ≈0.001″ for a primary inductance of 6.8 mH

T3 – Primary: 56 Turns, #23 AWG (2 strands) Bifiliar Wound
Secondary: ±12 V, 4 Turns, #23 AWG (4 strands) Quadfiliar Wound
Secondary 100 V: 32 Turns, #23 AWG (2 strands) Bifiliar Wound
Core: Ferroxcube EEC 40–3C8
Bobbin: Ferroxcube 40–1112CP
Gap: ≈0.030″ for a primary inductance of 212 µH

L1, L3, L4 – 25 µH at 1.0 A, Coilcraft Z7157.

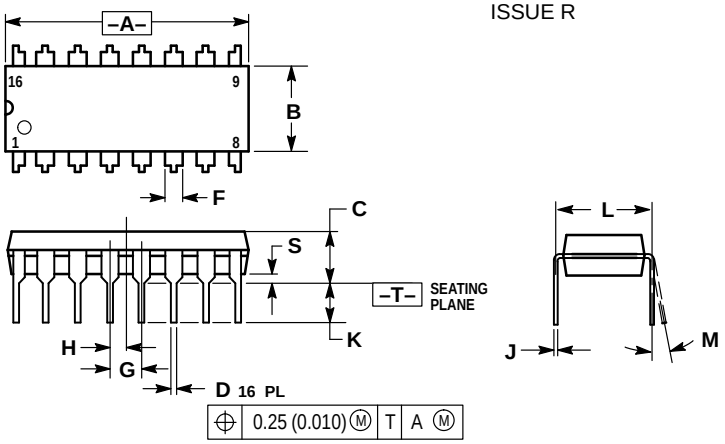
L2 – 10 µH at 3.0 A, Coilcraft PCV–0–010–03.

Figure 29. 125 Watt Off–Line Converter



OUTLINE DIMENSIONS

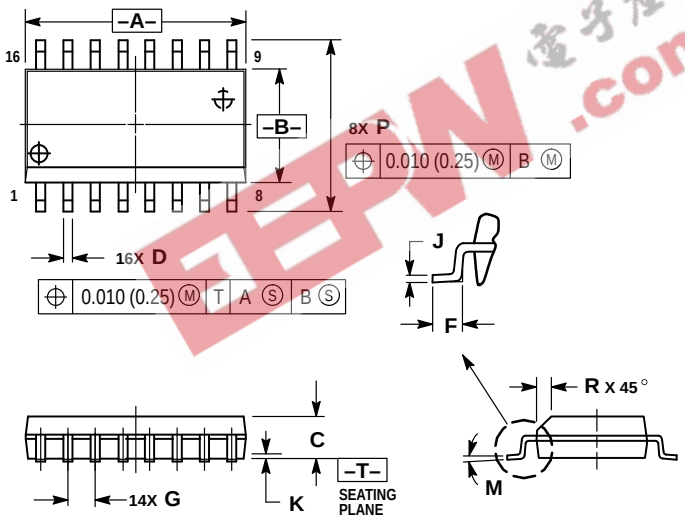
P SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

DW SUFFIX
PLASTIC PACKAGE
CASE 751G–02
(SO–16L)
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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