



MC34181,2,4 MC33181,2,4

Low Power, High Slew Rate, Wide Bandwidth, JFET Input Operational Amplifiers

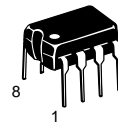
Quality bipolar fabrication with innovative design concepts are employed for the MC33181/2/4, MC34181/2/4 series of monolithic operational amplifiers. This JFET input series of operational amplifiers operates at 210 μA per amplifier and offers 4.0 MHz of gain bandwidth product and 10 $\text{V}/\mu\text{s}$ slew rate. Precision matching and an innovative trim technique of the single and dual versions provide low input offset voltages. With a JFET input stage, this series exhibits high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source/sink AC frequency response.

The MC33181/2/4, MC34181/2/4 series of devices are specified over the commercial or industrial/vehicular temperature ranges. The complete series of single, dual and quad operational amplifiers are available in the plastic DIP as well as the SOIC surface mount packages.

- Low Supply Current: 210 μA (Per Amplifier)
- Wide Supply Operating Range: $\pm 1.5 \text{ V}$ to $\pm 18 \text{ V}$
- Wide Bandwidth: 4.0 MHz
- High Slew Rate: 10 $\text{V}/\mu\text{s}$
- Low Input Offset Voltage: 2.0 mV
- Large Output Voltage Swing: -14 V to $+14 \text{ V}$ (with $\pm 15 \text{ V}$ Supplies)
- Large Capacitance Drive Capability: 0 pF to 500 pF
- Low Total Harmonic Distortion: 0.04%
- Excellent Phase Margin: 67°
- Excellent Gain Margin: 6.7 dB
- Output Short Circuit Protection
- Offered in New TSSOP Package Including the Standard SOIC and DIP Packages

ORDERING INFORMATION

Op Amp Function	Device	Operating Temperature Range	Package
Single	MC34181P MC34181D	$T_A = 0^\circ$ to $+70^\circ\text{C}$	Plastic DIP SO-8
	MC33181P MC33181D	$T_A = -40^\circ$ to $+85^\circ\text{C}$	Plastic DIP SO-8
Dual	MC34182P MC34182D	$T_A = 0^\circ$ to $+70^\circ\text{C}$	Plastic DIP SO-8
	MC33182P MC33182D	$T_A = -40^\circ$ to $+85^\circ\text{C}$	Plastic DIP SO-8
Quad	MC34184P MC34184D MC34184DTB	$T_A = 0^\circ$ to $+70^\circ\text{C}$	Plastic DIP SO-14 TSSOP-14
	MC33184P MC33184D MC33184DTB	$T_A = -40^\circ$ to $+85^\circ\text{C}$	Plastic DIP SO-14 TSSOP-14

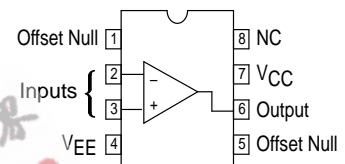


P SUFFIX
PLASTIC PACKAGE
CASE 626

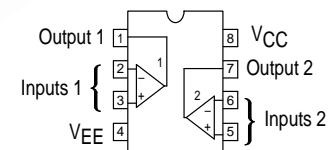


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

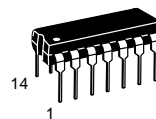
PIN CONNECTIONS



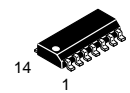
(Single, Top View)



(Dual, Top View)



P SUFFIX
PLASTIC PACKAGE
CASE 646

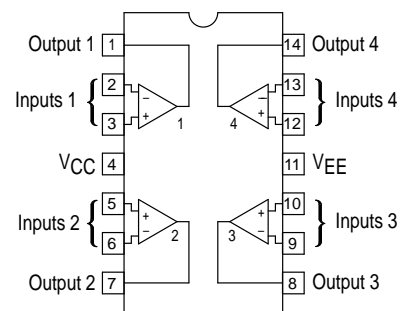


D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)



DTB SUFFIX
PLASTIC PACKAGE
CASE 948G
(TSSOP-14)

PIN CONNECTIONS



(Quad, Top View)

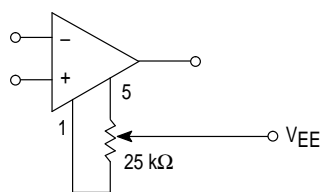
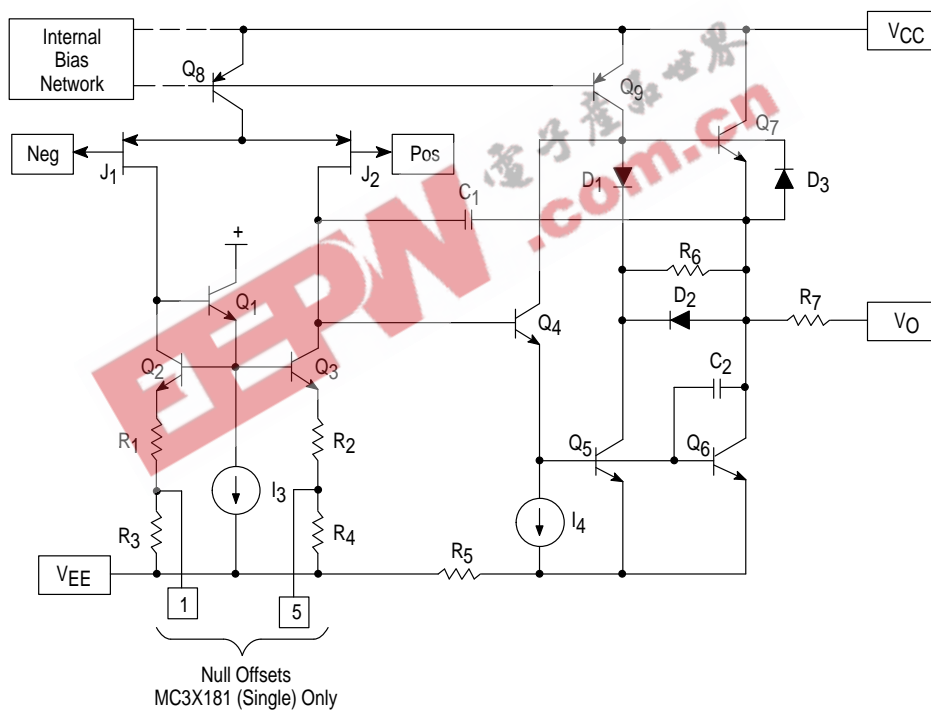
MC34181,2,4 MC33181,2,4

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range	V_{IDR}	Note 1	V
Input Voltage Range	V_{IR}	Note 1	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	-60 to +150	°C

NOTES: 1. Either or both input voltages should not exceed the magnitude of V_{CC} or V_{EE} .
 2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 1).

Representative Schematic Diagram (Each Amplifier)



MC3X181 Input Offset
Voltage Null Circuit

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DC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S = 50\ \Omega$, $V_O = 0\text{ V}$) Single $T_A = +25^\circ\text{C}$ $T_A = 0^\circ$ to $+70^\circ\text{C}$ (MC34181) $T_A = -40^\circ$ to $+85^\circ\text{C}$ (MC33181) Dual $T_A = +25^\circ\text{C}$ $T_A = 0^\circ$ to $+70^\circ\text{C}$ (MC34182) $T_A = -40^\circ$ to $+85^\circ\text{C}$ (MC33182) Quad $T_A = +25^\circ\text{C}$ $T_A = 0^\circ$ to $+70^\circ\text{C}$ (MC34184) $T_A = -40^\circ$ to $+85^\circ\text{C}$ (MC33184)	V_{IO}	—	0.5	2.0	mV
Average Temperature Coefficient of V_{IO} ($R_S = 50\ \Omega$, $V_O = 0\text{ V}$)	$\Delta V_{IO}/\Delta T$	—	10	—	$\mu\text{V}/^\circ\text{C}$
Input Offset Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = 0^\circ$ to $+70^\circ\text{C}$ $T_A = -40^\circ$ to $+85^\circ\text{C}$	I_{IO}	—	0.001	0.05	nA
Input Bias Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = 0^\circ$ to $+70^\circ\text{C}$ $T_A = -40^\circ$ to $+85^\circ\text{C}$	I_{IB}	—	0.003	0.1	nA
Input Common Mode Voltage Range	V_{ICR}	$(V_{EE} + 4.0\text{ V})$ to $(V_{CC} - 2.0\text{ V})$			V
Large Signal Voltage Gain ($R_L = 10\text{ k}\Omega$, $V_O = \pm 10\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to T_{high}	A_{VOL}	25 15	60 —	— —	V/mV
Output Voltage Swing ($V_{ID} = 1.0\text{ V}$, $R_L = 10\text{ k}\Omega$) $T_A = +25^\circ\text{C}$	V_{O+} V_{O-}	+13.5 —	+14 -14	— -13.5	V
Common Mode Rejection ($R_S = 50\ \Omega$, $V_{CM} = V_{ICR}$, $V_O = 0\text{ V}$)	CMR	70	86	—	dB
Power Supply Rejection ($R_S = 50\ \Omega$, $V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$)	PSR	70	84	—	dB
Output Short Circuit Current ($V_{ID} = 1.0\text{ V}$, Output to Ground) Source Sink	I_{SC}	3.0 8.0	8.0 11	— —	mA
Power Supply Current (No Load, $V_O = 0\text{ V}$) Single $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to T_{high} Dual $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to T_{high} Quad $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to T_{high}	I_D	—	210 —	250 250	μA
		—	420 —	500 500	
		—	840 —	1000 1000	

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AC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate ($V_{in} = -10\text{ V}$ to $+10\text{ V}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$) $A_V = +1.0$ $A_V = -1.0$	SR	7.0 —	10 10	— —	$\text{V}/\mu\text{s}$
Settling Time ($A_V = -1.0$, $R_L = 10\text{ k}\Omega$, $V_O = 0\text{ V}$ to $+10\text{ V}$ Step) To Within 0.10% To Within 0.01%	t_s	— —	1.1 1.5	— —	μs
Gain Bandwidth Product ($f = 100\text{ kHz}$)	GBW	3.0	4.0	—	MHz
Power Bandwidth ($A_V = +1.0$, $R_L = 10\text{ k}\Omega$, $V_O = 20\text{ V}_{pp}$, THD = 5.0%)	BW_p	—	120	—	kHz
Phase Margin ($-10\text{ V} < V_O < +10\text{ V}$) $R_L = 10\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	f_m	— —	67 34	— —	Degrees
Gain Margin ($-10\text{ V} < V_O < +10\text{ V}$) $R_L = 10\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	A_m	— —	6.7 3.4	— —	dB
Equivalent Input Noise Voltage $R_S = 100\ \Omega$, $f = 1.0\text{ kHz}$	e_n	—	38	—	$\text{nV}/\sqrt{\text{Hz}}$
Equivalent Input Noise Current $f = 1.0\text{ kHz}$	i_n	—	0.01	—	$\text{pA}/\sqrt{\text{Hz}}$
Differential Input Capacitance	C_i	—	3.0	—	pF
Differential Input Resistance	R_i	—	10^{12}	—	Ω
Total Harmonic Distortion $A_V = 10$, $R_L = 10\text{ k}\Omega$, $2.0\text{ V}_{pp} < V_O < 20\text{ V}_{pp}$, $f = 1.0\text{ kHz}$	THD	—	0.04	—	%
Channel Separation ($R_L = 10\text{ k}\Omega$, $-10\text{ V} < V_O < +10\text{ V}$, $0\text{ Hz} < f < 10\text{ kHz}$)	—	—	120	—	dB
Open Loop Output Impedance ($f = 1.0\text{ MHz}$)	$ Z_o $	—	200	—	Ω

Figure 1. Maximum Power Dissipation versus Temperature for Package Variations

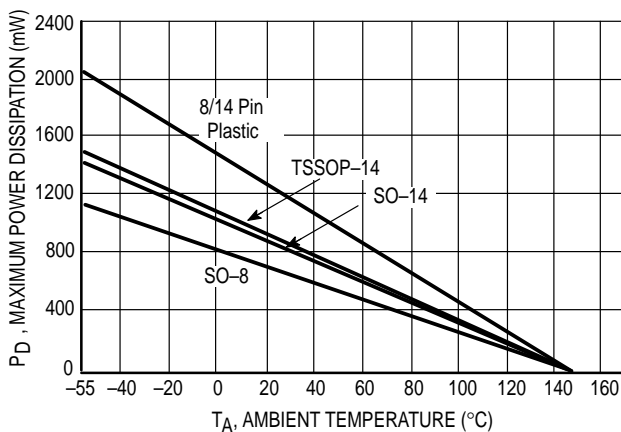
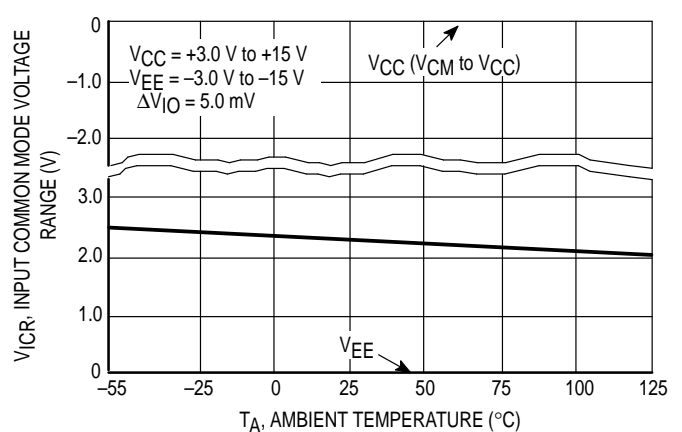


Figure 2. Input Common Mode Voltage Range versus Temperature



MC34181,2,4 MC33181,2,4

Figure 3. Input Bias Current versus Temperature

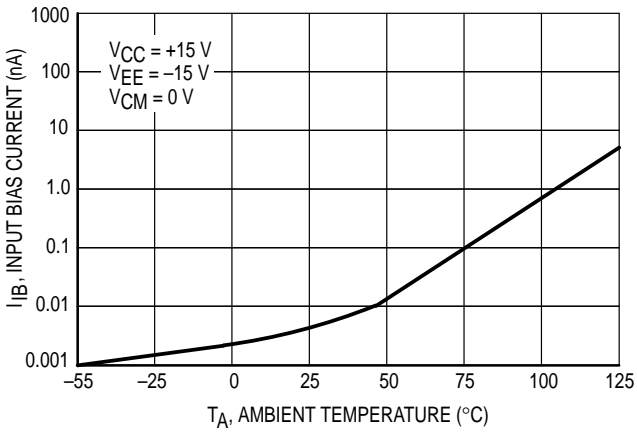


Figure 4. Input Bias Current versus Input Common Mode Voltage

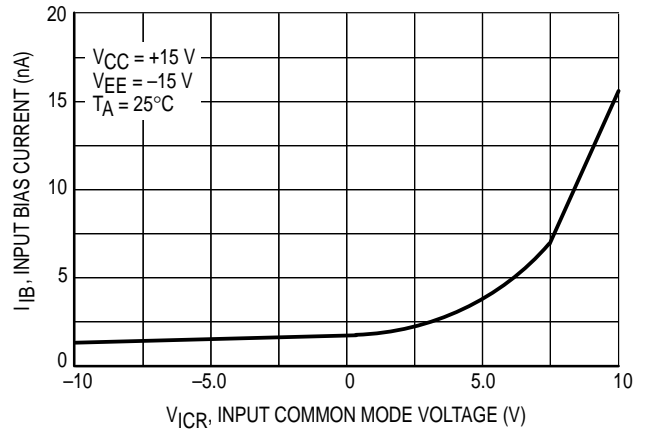


Figure 5. Output Voltage Swing versus Supply Voltage

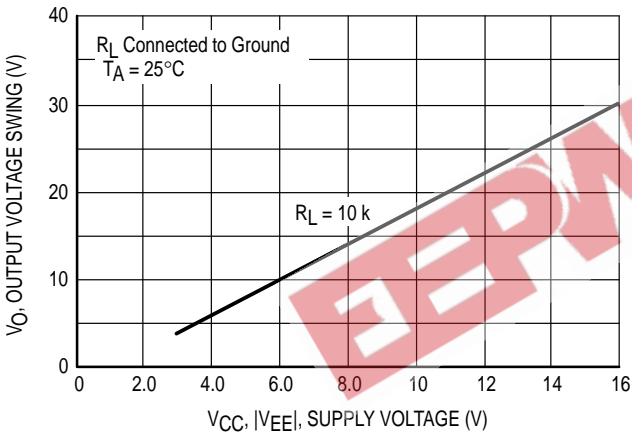


Figure 6. Output Saturation Voltage versus Load Current

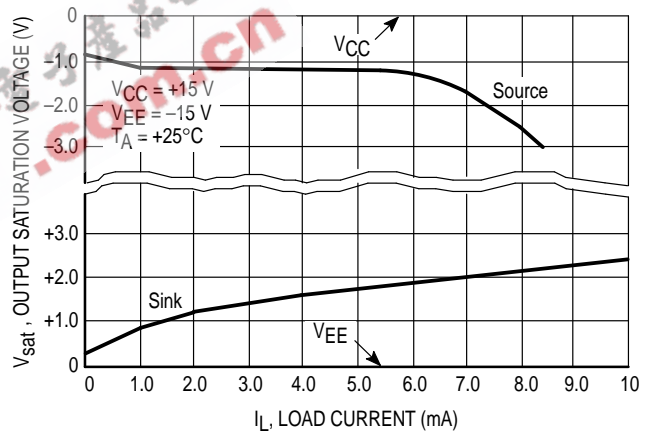


Figure 7. Output Saturation Voltage versus Load Resistance to Ground

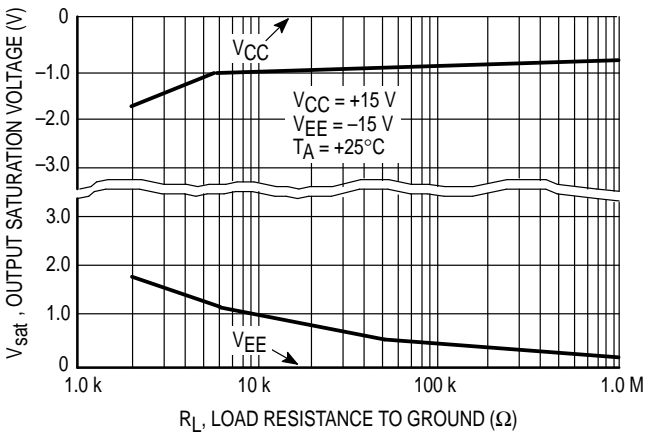
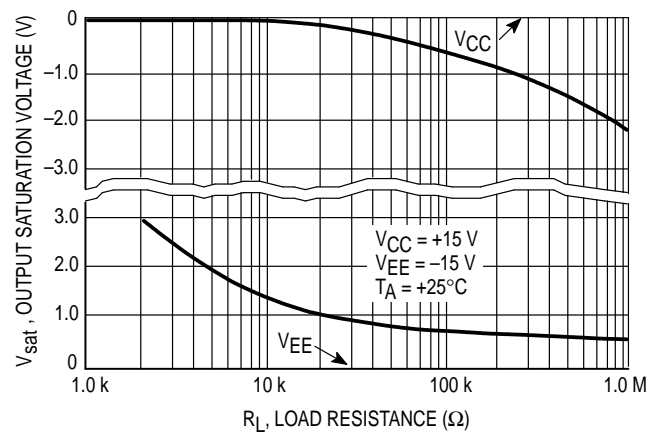


Figure 8. Output Saturation Voltage versus Load Resistance to V_{CC}



MC34181,2,4 MC33181,2,4

Figure 9. Output Short Circuit Current versus Temperature

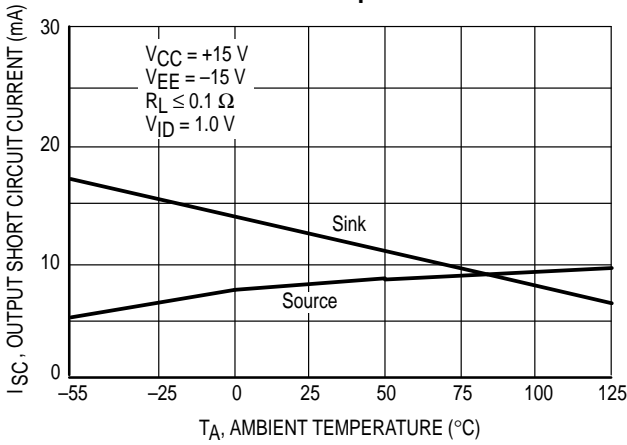


Figure 10. Output Impedance versus Frequency

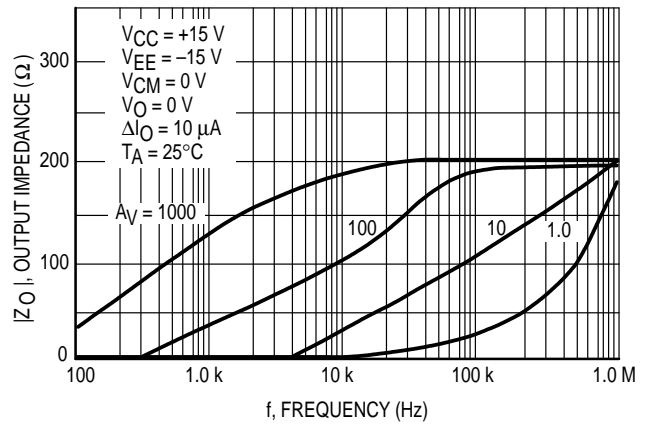


Figure 11. Output Voltage Swing versus Frequency

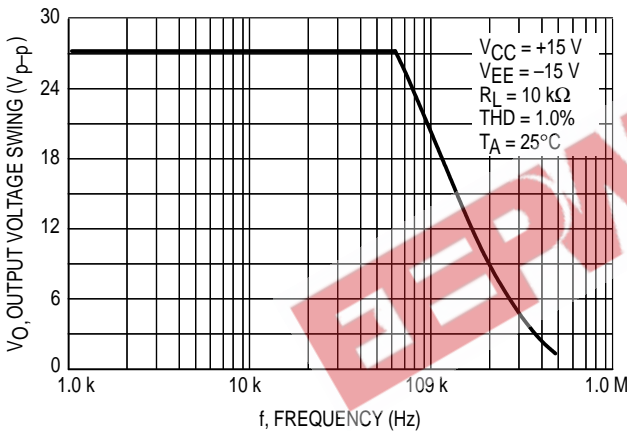


Figure 12. Output Distortion versus Frequency

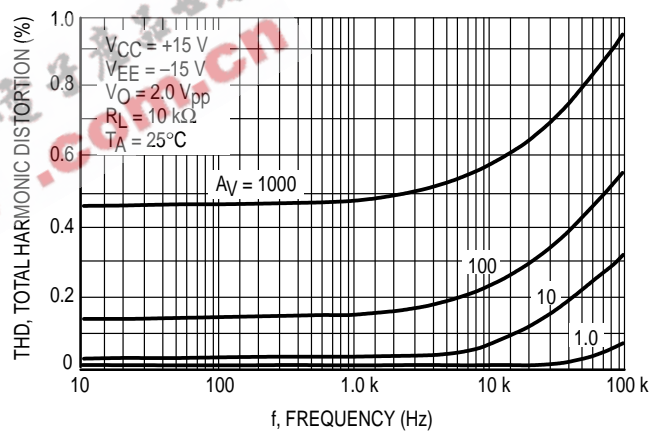


Figure 13. Open Loop Voltage Gain versus Temperature

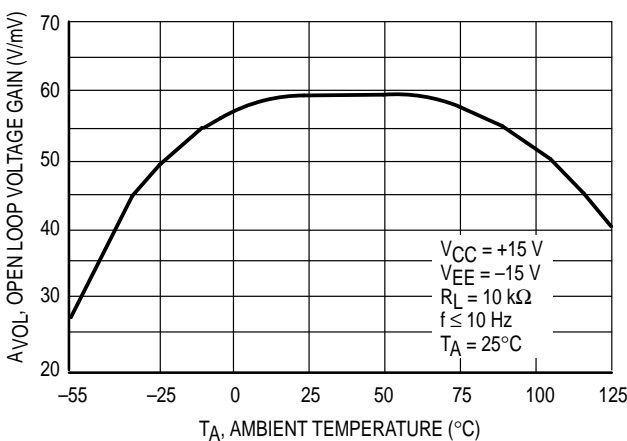
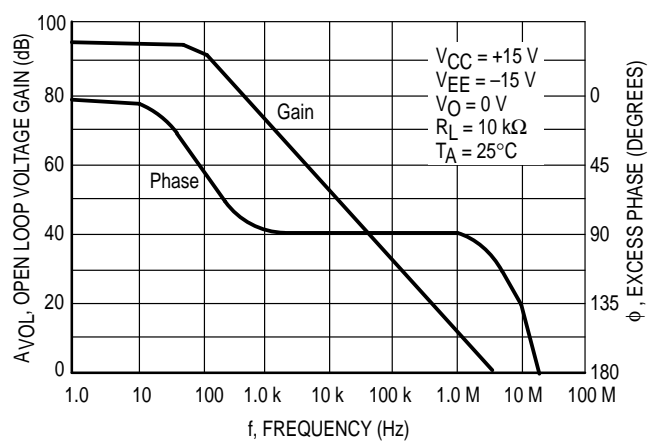


Figure 14. Open Loop Voltage Gain and Phase versus Frequency



MC34181,2,4 MC33181,2,4

Figure 15. Normalized Gain Bandwidth Product versus Temperature

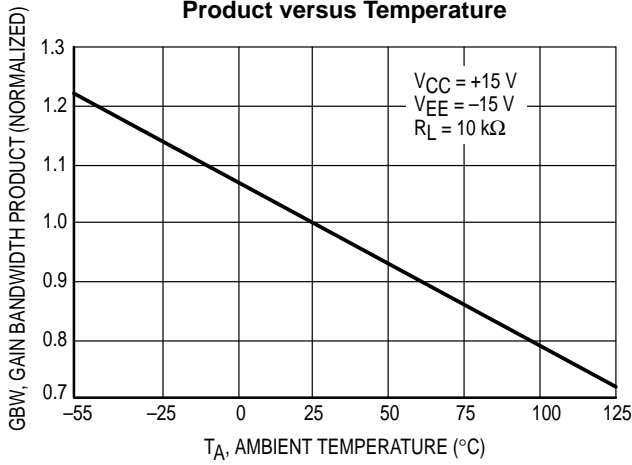


Figure 16. Output Voltage Overshoot versus Load Capacitance

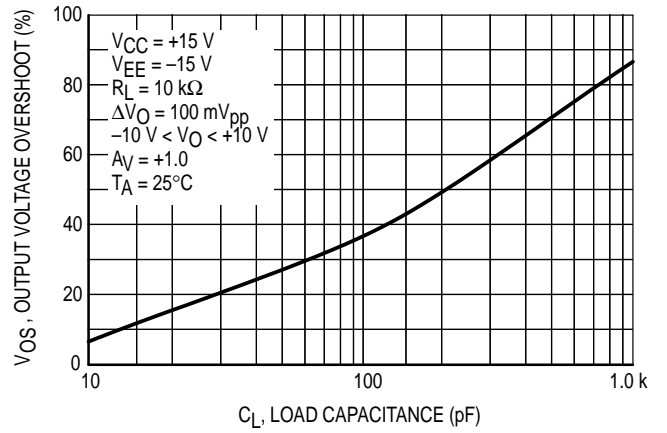


Figure 17. Phase Margin versus Load Capacitance

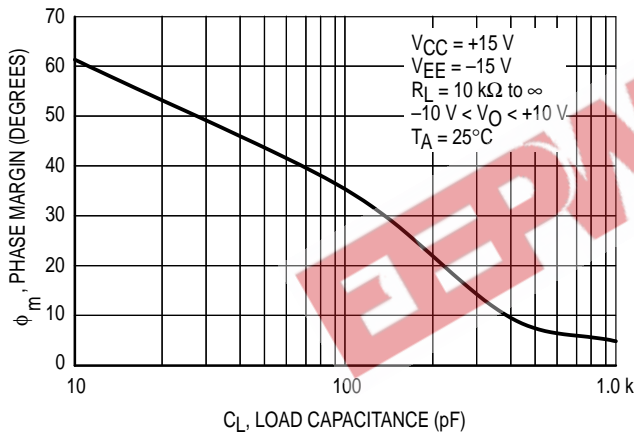


Figure 18. Gain Margin versus Load Capacitance

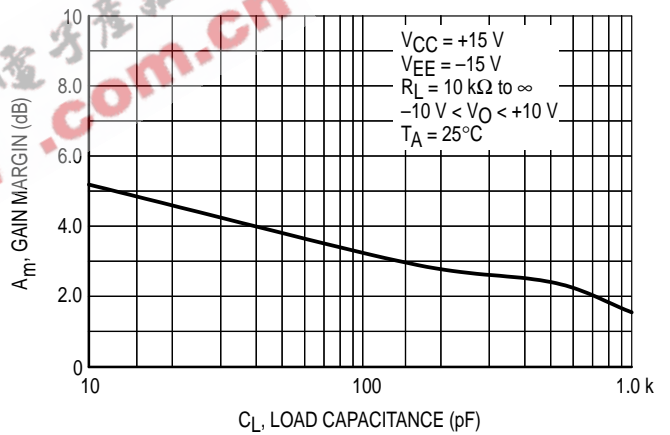


Figure 19. Phase Margin versus Temperature

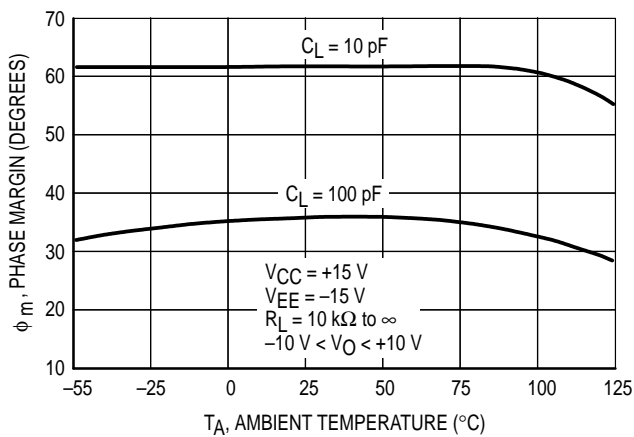
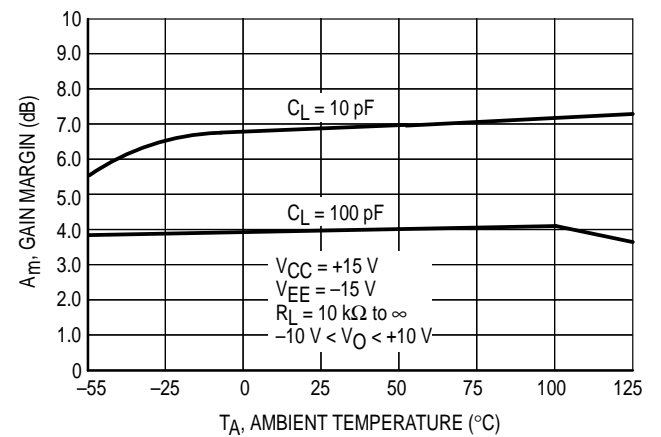


Figure 20. Gain Margin versus Temperature



MC34181,2,4 MC33181,2,4

Figure 21. Normalized Slew Rate versus Temperature

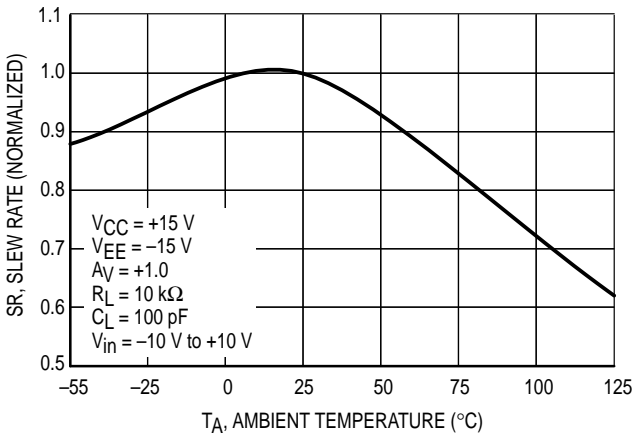


Figure 22. Common Mode Rejection versus Frequency

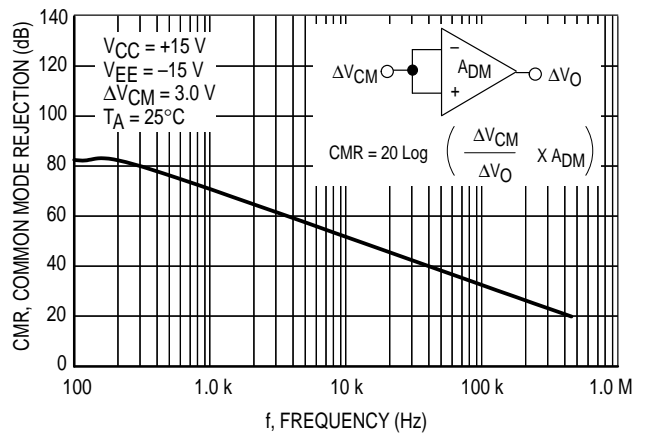


Figure 23. Input Noise Voltage versus Frequency

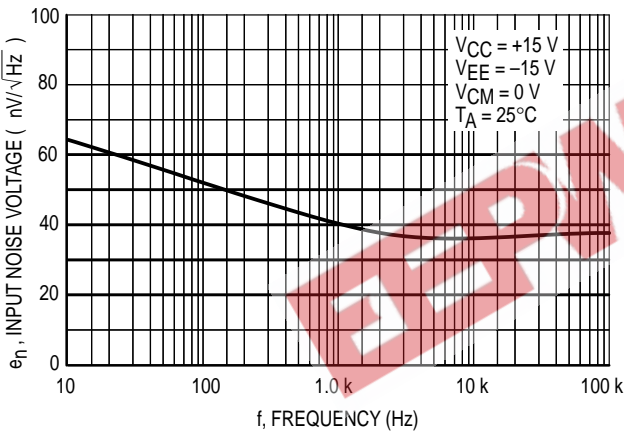


Figure 24. Power Supply Rejection versus Temperature

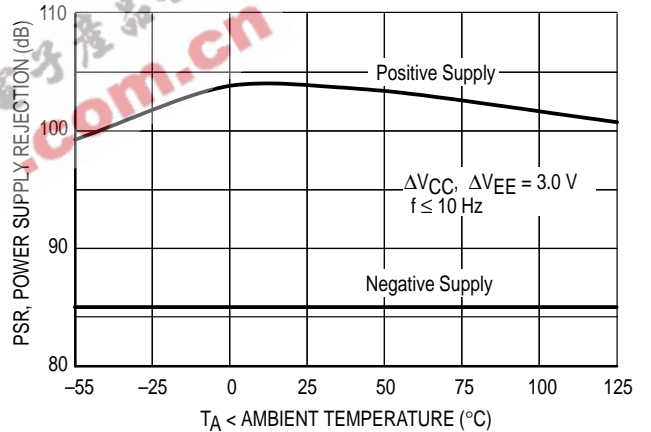


Figure 25. Power Supply Rejection versus Frequency

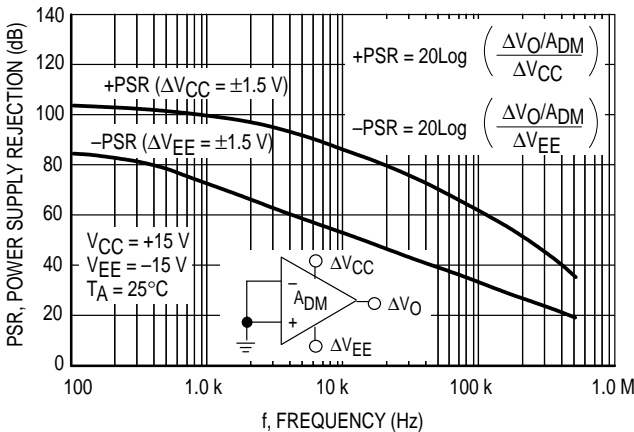
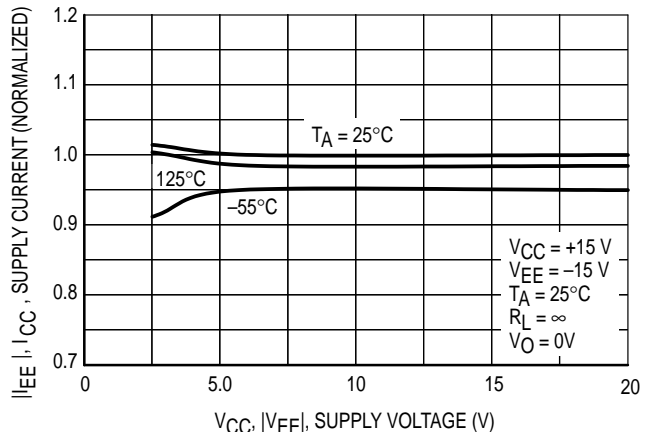


Figure 26. Normalized Supply Current versus Supply Voltage



MC34181,2,4 MC33181,2,4

Figure 27. Channel Separation versus Frequency

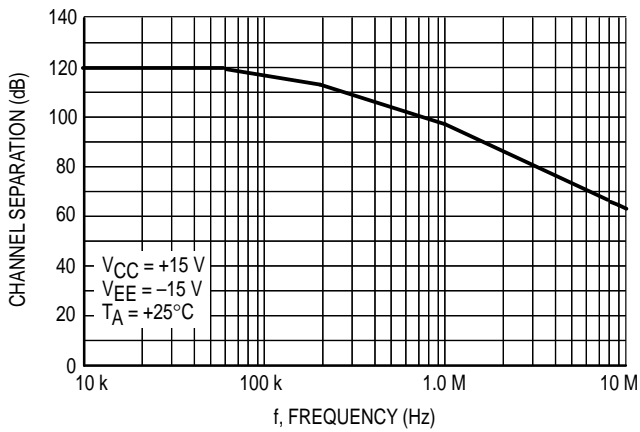


Figure 28. Transient Response

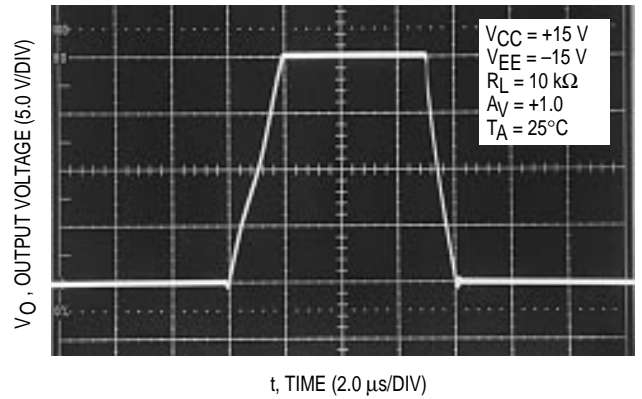
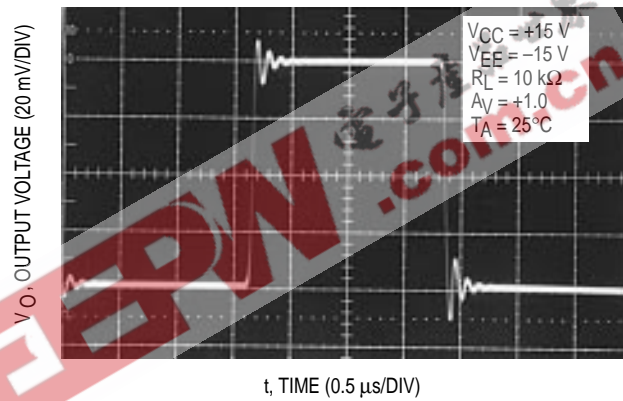


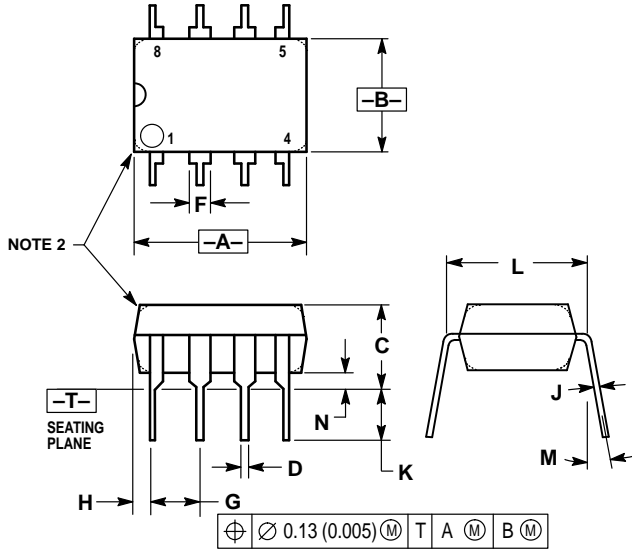
Figure 29. Small Signal Transient Reponse



MC34181,2,4 MC33181,2,4

OUTLINE DIMENSIONS

P SUFFIX
 PLASTIC PACKAGE
 CASE 626-05
 ISSUE K

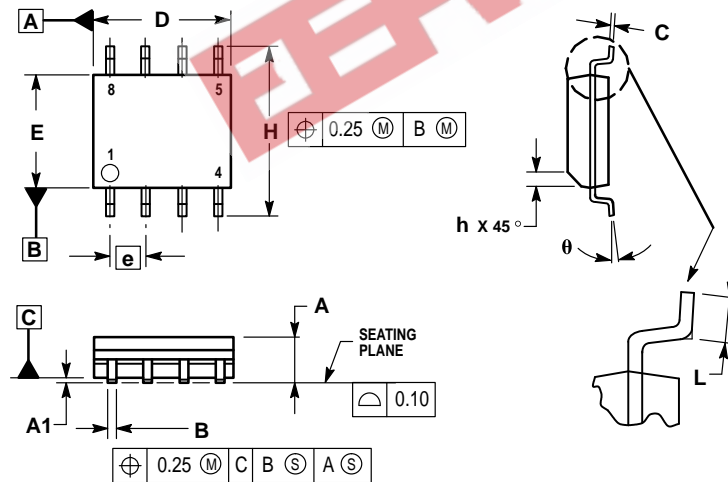


NOTES:

1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	— 10°		— 10°	
N	0.76	1.01	0.030	0.040

D SUFFIX
 PLASTIC PACKAGE
 CASE 751-05
 (SO-8)
 ISSUE R



NOTES:

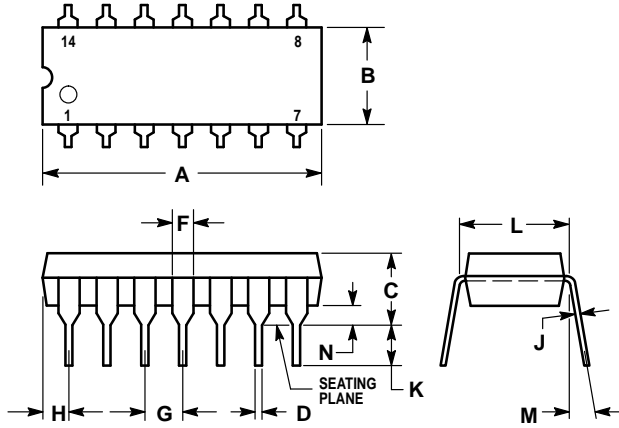
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

MC34181,2,4 MC33181,2,4

OUTLINE DIMENSIONS – continued

P SUFFIX PLASTIC PACKAGE CASE 646-06 ISSUE L

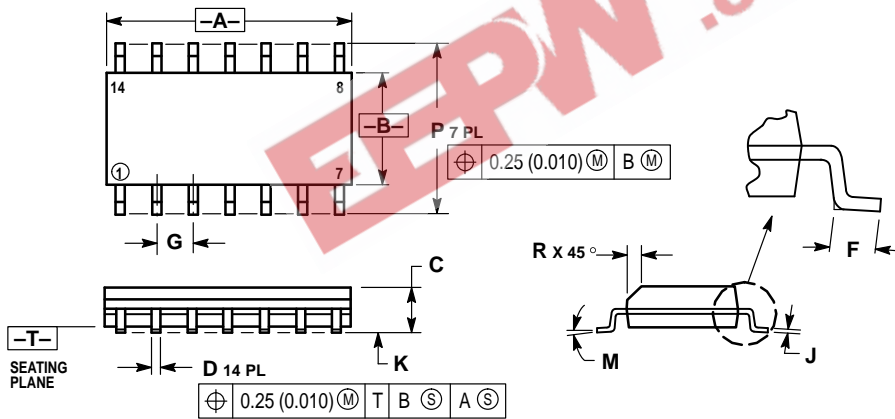


NOTES:

- LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

D SUFFIX PLASTIC PACKAGE CASE 751A-03 (SO-14) ISSUE F




NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

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