

MC1466L

PRECISION WIDE RANGE VOLTAGE AND CURRENT REGULATOR

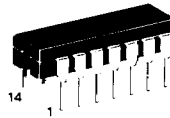
This unique "floating" regulator can deliver hundreds of volts — limited only by the breakdown voltage of the external series pass transistor. Output voltage and output current are adjustable. The MC1466L integrated circuit voltage and current regulator is designed to give "laboratory" power-supply performance.

- Voltage/Current Regulation with Automatic Crossover
- Excellent Line Voltage Regulation, 0.03% + 3.0 mV (Max)
- Excellent Load Voltage Regulation, 0.03% + 3.0 mV (Max)
- Excellent Current Regulation, 0.2% + 1.0 mA
- Short-Circuit Protection
- Output Voltage Adjustable to Zero Volts
- Internal Reference Voltage
- Adjustable Internal Current Source

PRECISION WIDE RANGE VOLTAGE and CURRENT REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

L SUFFIX
 CERAMIC PACKAGE
 CASE 632



3

TYPICAL APPLICATIONS

FIGURE 1 — 0-TO-15 Vdc, 10-AMPERE REGULATOR

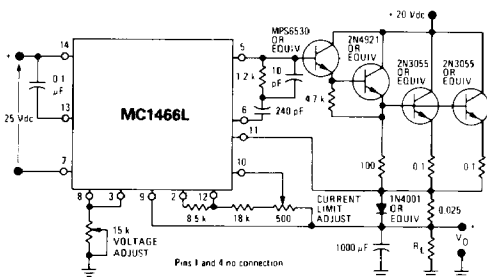


FIGURE 2 — 0-TO-40 Vdc, 0.5-AMPERE REGULATOR

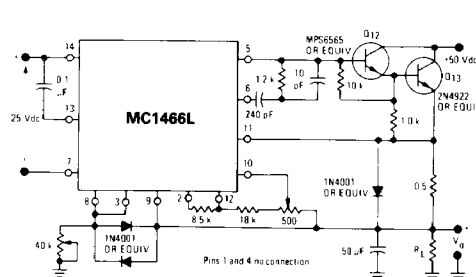


FIGURE 3 — 0-TO-25 Vdc, 0.1-AMPERE REGULATOR

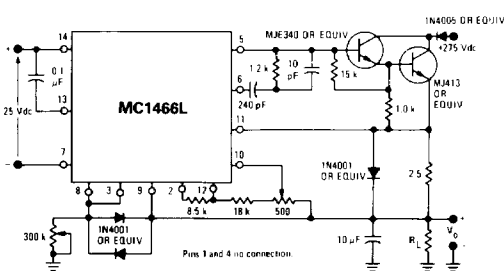
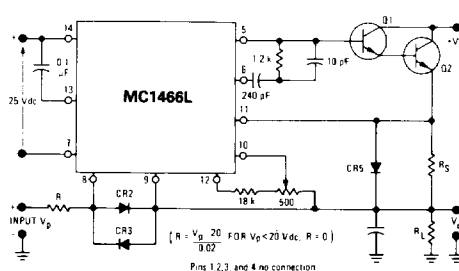


FIGURE 4 — REMOTE PROGRAMMING



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MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Auxiliary Voltage	V_{aux}	30	Vdc
Power Dissipation (Package Limitation) Derate above $T_A = +50^\circ\text{C}$	P_D $1/\theta_{JA}$	750 6.0	mW mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$, $V_{aux} = +25\text{ Vdc}$ unless otherwise noted)

Characteristic Definition	Characteristic	Symbol	Min	Typ	Max	Units
<p>MC1466*</p>	Auxiliary Voltage (See Notes 1 & 2) (Voltage from pin 14 to pin 7)	V_{aux}	21	—	30	Vdc
	Auxiliary Current	I_{aux}	—	9.0	12	mAdc
	Internal Reference Voltage (Voltage from pin 12 to pin 7)	V_{IR}	17.3	18.2	19.7	Vdc
	Reference Current (See Note 3)	I_{ref}	0.8	1.0	1.2	mAdc
	Input Current — Pin 8	I_g	—	6.0	12	μAdc
	Power Dissipation	P_D	—	—	360	mW
<p>MC1466*</p>	Input Offset Voltage, Voltage Control Amplifier (See Note 4)	V_{iov}	0	15	40	mVdc
	Load Voltage Regulation (See Note 5)	ΔV_{iov} $\Delta V_{ref}/V_{ref}$	—	1.0	3.0	mV %
	Line Voltage Regulation (See Note 6)	ΔV_{iov} $\Delta V_{ref}/V_{ref}$	—	1.0	3.0	mV %
	Temperature Coefficient of Output Voltage ($T_A = 0$ to $+75^\circ\text{C}$)	TCV_o	—	0.01	—	%/°C
<p>MC1466*</p>	Input Offset Voltage, Current Control Amplifier (See Note 4) (Voltage from pin 10 to pin 11)	V_{ioi}	0	15	40	mVdc
	Load Current Regulation (See Note 7)	$\Delta I_L/I_L$ ΔI_{ref}	—	0.2	—	% mAdc

*Pins 1 and 4 no connection.

MC1466L

NOTE 1:

The instantaneous input voltage, V_{aux} , must not exceed the maximum value of 30 volts for the MC1466. The instantaneous value of V_{aux} must be greater than 21 volts for the MC1466 for proper internal regulation.

NOTE 2:

The auxiliary supply voltage V_{aux} , must "float" and be electrically isolated from the unregulated high voltage supply, V_{in} .

NOTE 3:

Reference current may be set to any value of current less than 1.2 mA by applying the relationship:

$$I_{ref} \text{ (mA)} = \frac{8.55}{R_1 \text{ (k}\Omega\text{)}}$$

NOTE 4:

A built-in offset voltage (15 mVdc nominal) is provided so that the power supply output voltage or current may be adjusted to zero.

NOTE 5:

Load Voltage Regulation is a function of two additive components, ΔV_{ioV} and ΔV_{ref} , where ΔV_{ioV} is the change in input offset voltage (measured between pins 8 and 9) and ΔV_{ref} is the change in voltage across R2 (measured between pin 8 and ground). Each component may be measured separately or the sum may be measured across the load. The measurement procedure for the test circuit shown is:

- With S1 open ($I_L = 0$) measure the value of $V_{ioV(1)}$ and $V_{ref(1)}$.
- Close S1, adjust R4 so that $I_L = 500 \mu\text{A}$ and note $V_{ioV(2)}$ and $V_{ref(2)}$.

Then $\Delta V_{ioV} = V_{ioV(1)} - V_{ioV(2)}$

% Reference Regulation =

$$\frac{[V_{ref(1)} - V_{ref(2)}]}{V_{ref(1)}} (100\%) = \frac{\Delta V_{ref}}{V_{ref}} (100\%)$$

Load Voltage Regulation =

$$\frac{\Delta V_{ref}}{V_{ref}} (100\%) + \Delta V_{ioV}$$

NOTE 6:

Line Voltage Regulation is a function of the same two additive components as Load Voltage Regulation, ΔV_{ioV} and ΔV_{ref} (see Note 5). The measurement procedure is:

- Set the auxiliary voltage, V_{aux} , to 22 volts. Read the value of $V_{ioV(1)}$ and $V_{ref(1)}$.
- Change the V_{aux} to 28 volts and note the value of $V_{ioV(2)}$ and $V_{ref(2)}$. Then compute Line Voltage Regulation:

$\Delta V_{ioV} = V_{ioV(1)} - V_{ioV(2)}$

% Reference Regulation =

$$\frac{[V_{ref(1)} - V_{ref(2)}]}{V_{ref(1)}} (100\%) = \frac{\Delta V_{ref}}{V_{ref}} (100\%)$$

Line Voltage Regulation =

$$\frac{\Delta V_{ref}}{V_{ref}} (100\%) + \Delta V_{ioV}$$

NOTE 7:

Load Current Regulation is measured by the following procedure:

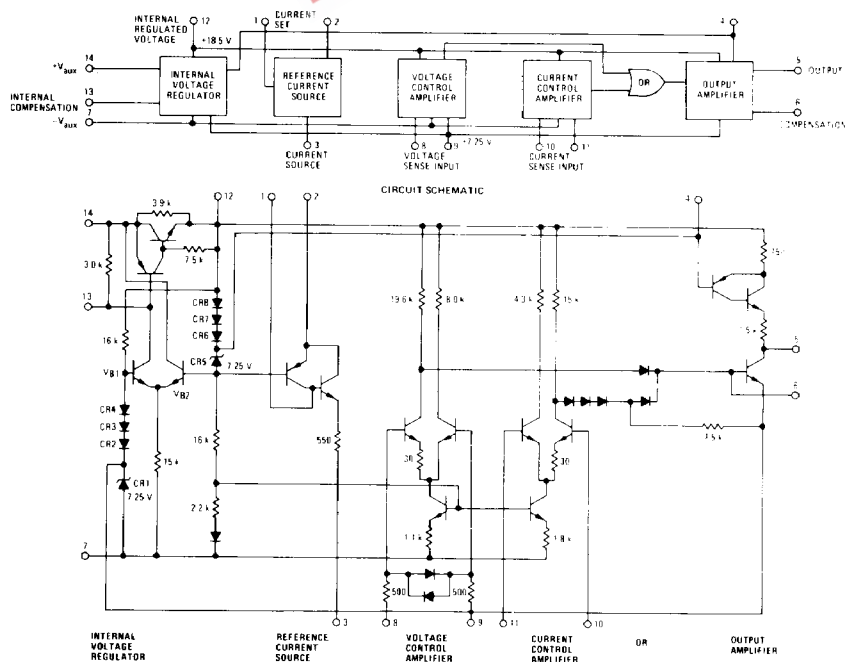
- With S2 open, adjust R3 for an initial load current, $I_{L(1)}$, such that V_o is 8.0 Vdc.
- With S2 closed, adjust R7 for $V_o = 1.0$ Vdc and read $I_{L(2)}$. Then Load Current Regulation =

$$\frac{[I_{L(2)} - I_{L(1)}]}{I_{L(1)}} (100\%) + I_{ref}$$

where I_{ref} is 1.0 mA. Load Current Regulation is specified in this manner because I_{ref} passes through the load in a direction opposite that of load current and does not pass through the current sense resistor, R_s .

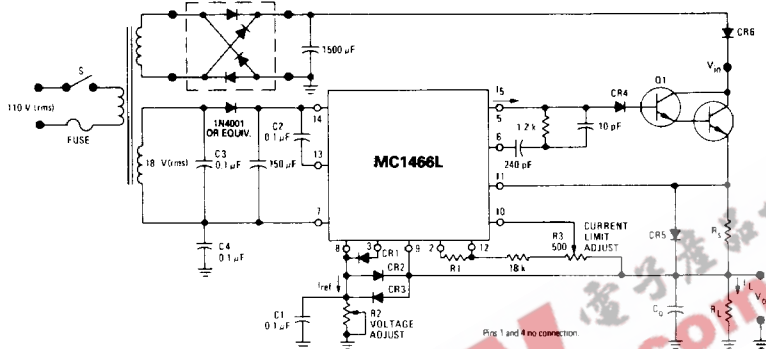


FIGURE 5 — BLOCK DIAGRAM



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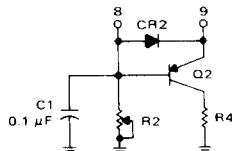
FIGURE 6 – TYPICAL CIRCUIT CONNECTION



NORMAL DESIGN PROCEDURE AND DESIGN CONSIDERATIONS

- Constant Voltage:**
For constant voltage operation, output voltage V_o is given by:
 $V_o = I_{ref} (R_2)$
where R_2 is the resistance from pin 8 to ground and I_{ref} is the output current of pin 3.
The recommended value of I_{ref} is 1.0 mAdc. Resistor R_1 sets the value of I_{ref} :
 $I_{ref} = \frac{8.5}{R_1}$
where R_1 is the resistance between pins 2 and 12.
- Constant Current:**
For constant current operation:
(a) Select R_5 for a 250 mV drop at the maximum desired regulated output current, I_{max} .
(b) Adjust potentiometer R_3 to set constant current output at desired value between zero and I_{max} .
- If V_{in} is greater than 20 Vdc, CR2, CR3, and CR4 are necessary to protect the MC1466 during short circuit or transient conditions.
- In applications where very low output noise is desired, R2 may be bypassed with C1 (0.1 µF to 2.0 µF). When R2 is bypassed, CR1 is necessary for protection during short circuit conditions.
- CR5 is recommended to protect the MC1466 from simultaneous pass transistor failure and output short circuit.
- The RC network (10 pF, 240 pF, 1.2 kΩ) is used for compensation. The values shown are valid for all applications. However, the 10 pF capacitor may be omitted if f_r of Q1 and Q2 is greater than 0.5 MHz.
- For remote sense applications, the positive voltage sense terminal (Pin 9) is connected to the positive load terminal through a separate sense lead; and the negative sense terminal (the ground side of R2) is connected to the negative load terminal through a separate sense lead.
- C_o may be selected by using the relationship:
 $C_o = (100 \mu F) I_{L(max)}$ where $I_{L(max)}$ is the maximum load current in amperes.
- C2 is necessary for the internal compensation of the MC1466.
- For optimum regulation, current out of Pin 5, I_5 should not exceed 0.5 mAdc. Therefore select Q1 and Q2 such that:
 $\frac{I_{max}}{\beta_1 \beta_2} \leq 0.5 \text{ mAdc}$
where: I_{max} = maximum short-circuit load current (mAdc)
 β_1 = minimum beta of Q1
 β_2 = minimum beta of Q2
Although Pin 5 will source up to 1.5 mAdc, $I_5 > 0.5 \text{ mAdc}$ will result in a degradation in regulation.
- CR6 is recommended when $V_o > 150 \text{ Vdc}$ and should be rated such that Peak Inverse Voltage $> V_o$.

- In applications where R2 might be rapidly reduced in value, it is recommended that CR3 be replaced by Q2 and R4.



This design consideration prevents R2 from being destroyed by excessive discharge current from C_o . Components Q2 and R4 should be selected such that:

$$R_4 = \frac{R_2}{10} \text{ and } V_{CEO} \text{ of } Q_2 \geq V_o$$

MC1466L

OPERATION AND APPLICATIONS

This section describes the operation and design of the MC1466 voltage and current regulator and also provides information on useful applications.

THEORY OF OPERATION

The schematic of Figure 5 can be simplified by breaking it down into basic functions, beginning with a simplified version of the voltage reference, Figure 7. Zener diodes CR1 and CR5 with their associated forward biased diodes CR2 through CR4 and CR6 through CR8 form the stable reference needed to balance the differential amplifier. At balance ($V_{B1} = V_{B2}$), the output voltage, ($V_{12} - V_7$), is at a value that is twice the drop across either of the two diode strings: $V_{12} - V_7 = 2(V_{CR1} + V_{CR2} + V_{CR3} + V_{CR4})$. Other voltages, temperature compensated or otherwise, are also derived from these diodes strings for use in other parts of the circuit.

The voltage controlled current source (Figure 8) is a PNP-NPN composite which, due to the high NPN beta,

yields a good working PNP from a lateral device working at a collector current of only a few microamperes. Its base voltage (V_{B2}) is derived from a temperature compensated portion of the diode string and consequently the overall current is dependent on the value of emitter resistor R_1 . Temperature compensation of the base emitter junction of Q3 is not important because approximately 9 volts exists between V_{B2} and V_{12} , making the ΔV_{BE} 's very small in percentage. Circuit reference voltage is derived from the product of I_R and R_R ; if I_R is set at 1 mA ($R_1 = 8.5 \text{ k}\Omega$), then R_R (in $\text{k}\Omega$) = V_O . Other values of current may be used as long as the following restraints are kept in mind: 1) package dissipation will be increased by about 11 mW/mA and 2) bias current for the voltage control amplifier is 3 μA , temperature dependent, and is extracted from the reference current. The reference current should

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FIGURE 7 - REFERENCE VOLTAGE REGULATOR

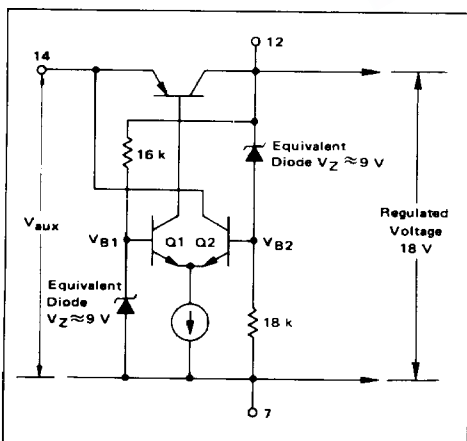
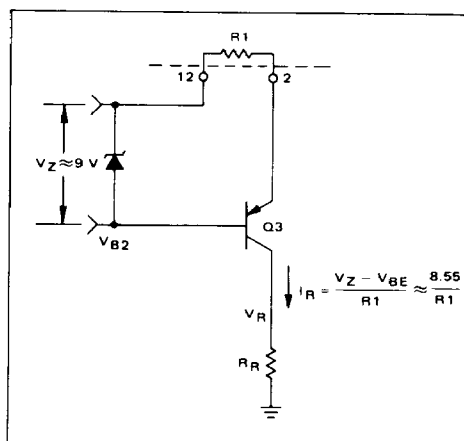


FIGURE 8 - VOLTAGE CONTROLLED CURRENT SOURCE



MC1466L

be at least two orders of magnitude above the largest expected bias current.

Loop amplification in the constant voltage mode is supplied by the voltage controlled amplifier (Figure 9), a standard high gain differential amplifier. The inputs are diode-protected against differential overvoltages and an emitter degenerating resistor, R_{OS} , has been added to one of the transistors. For an emitter current in both Q5 and Q6 of 1/2 milliampere there will exist a preset offset voltage in this differential amplifier of 15 mV to insure that the output voltage will be zero when the reference voltage is zero. Without R_{OS} , the output voltage could be a few millivolts above zero due to the inherent offset. Since the load resistor is so large in this stage compared with the load (Q9) it will be more instructive to look at the gain on a transconductance basis rather than voltage gain. Transconductance of the differential stage is defined for small signals as:

$$g_m \approx \frac{1}{2r_e + R_E} \quad (1)$$

where

$$r_e \approx \frac{0.026}{I_E} \text{ and}$$

R_E = added emitter degenerating resistance.

For $I_E = 0.5 \text{ mA}$,

$$g_m = \frac{1}{104 + 30} = \frac{1}{134} = 7.5 \text{ mA/volt.} \quad (2)$$

FIGURE 9 - VOLTAGE CONTROL AMPLIFIER

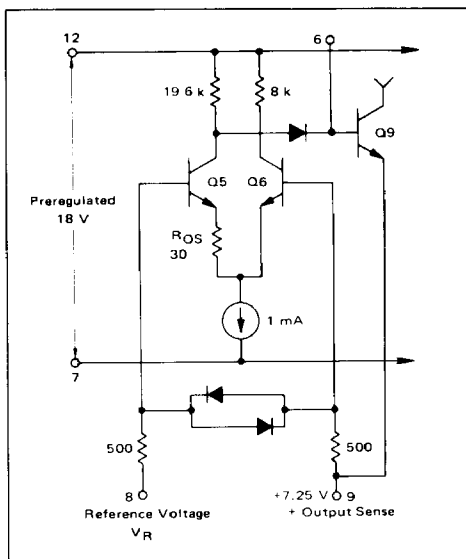
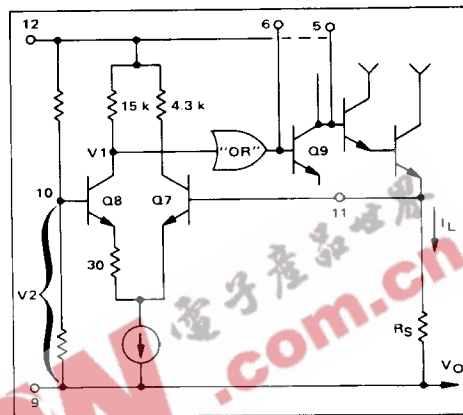


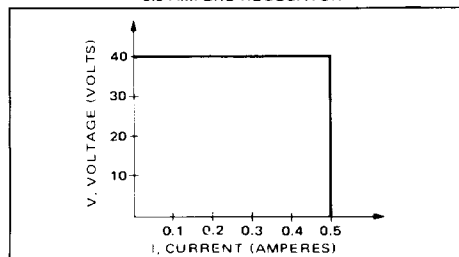
FIGURE 10 - CURRENT CONTROL CIRCUIT



This level is further boosted by the output stage such that in the constant voltage mode overall transconductance is about 300 mA/volt.

A second differential stage nearly identical to the first stage, serves as the current control amplifier (Figure 10). The gain of this stage insures a rapid crossover from the constant voltage to constant current modes and provides a convenient point to control the maximum deliverable load current. In use, a reference voltage derived from the preregulator and a voltage divider is applied to pin 10 while the output current is sampled across R_S by pin 11. When $I_L R_S$ is 15 mV below the reference value, voltage V_1 begins to rapidly rise, eventually gaining complete control of Q9 and limiting output current to a value of V_2/R_S . If V_2 is derived from a variable source, short circuit current may be controlled over the complete output current capability of the regulator. Since the constant-voltage to constant-current change-over requires only a few millivolts the voltage regulation maintains its quality to the current limit and accordingly shows a very sharp "knee" (1% +1 mA, Figure 11). Note that the regulator can switch back into the constant voltage mode if the output voltage reaches a value greater than V_R . Operation through zero milliamperes is guaranteed by the inclusion of another emitter offsetting resistor.

FIGURE 11 - V_1 CURVE FOR 0 TO 40 V, 0.5-AMPERE REGULATOR



MC1466L

Transistor Q9 and five diodes comprise the essential parts of the output stage (Figure 12). The diodes perform an "OR" function which allows only one mode of operation at a time - constant current or constant voltage. However, an additional stage (Q9) must be included to invert the logic and make it compatible with the driving requirements of series pass transistors as well as provide additional gain. A 1.5 mA collector current source sets the maximum deliverable output current and boosts the output impedance to that of the current source.

Note that the negative (substrate) side of the MC1466 is 7.25 volts lower than the output voltage, and the reference regulator guarantees that the positive side is 11 volts above the output. Thus the IC remains at a voltage (relative to ground) solely dependent on the output, "floating" above and below V_O . V_{CE} across Q9 is only two or three V_{BE} 's depending on the number of transistors used in the series pass configuration.

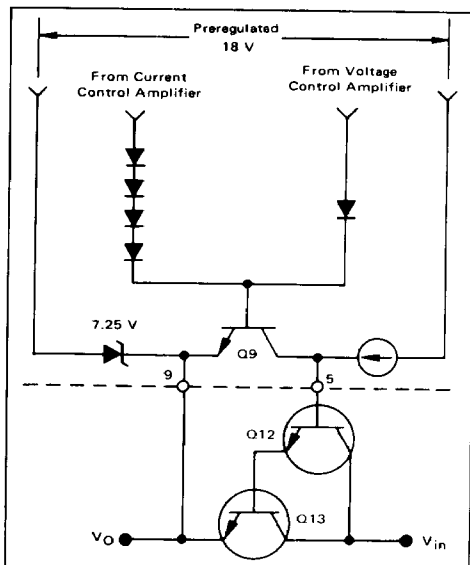
Performance characteristics of the regulator may be approximately calculated for a given circuit (Figure 2). Assuming that the two added transistors (Q12 and Q13) have minimum betas of 20, then the overall regulator transconductance will be:

$$g_{mT} = (400) 300 \text{ mA/volt} = 120 \text{ A/volt.} \quad (3)$$

For a change in current of 500 mA the output voltage will drop only:

$$\Delta V = \frac{0.5}{120} = 4.2 \text{ mV.} \quad (4)$$

FIGURE 12 — MC1466 OUTPUT STAGE



The analysis thus far does not consider changes in V_R due to output current changes. If I_L increases by 500 mA the collector current of Q9 decreases by 1.25 mA, causing the collector current of Q5 to increase by 30 μA . Accordingly, I_R will be decreased by $\approx 0.30 \mu\text{A}$ which will drop the output by 0.03%. This figure may be improved considerably by either using high beta devices as the pass transistors, or by increasing I_R . Note again, however, that the maximum power rating of the package must be kept in mind. For example if $I_R = 4 \text{ mA}$, power dissipation is

$$P_D = 20 \text{ V} (8 \text{ mA}) + (11 \text{ V} \times 3 \text{ mA}) = 193 \text{ mW.} \quad (5)$$

This indicates that the circuit may be safely operated up to 118°C using 20 volts at the auxiliary supply voltage. If, however, the auxiliary supply voltage is 35 volts,

$$P_D = 35 \text{ V} (8 \text{ mA}) + 26 \text{ V} (3 \text{ mA}) = 358 \text{ mW.} \quad (6)$$

which dictates that the maximum operating temperature must be less than 91°C to keep package dissipation within specified limits.

Line voltage regulation is also a function of the voltage change between pins 8 and 9, and the change of V_{ref} . In this case, however, these voltages change due to changes in the internal regulator's voltages, which in turn are caused by changes in V_{aux} . Note that line voltage regulation is not a function of V_{in} . Note also that the instantaneous value of V_{aux} must always be between 20 and 35 volts.

Figure 6 shows six external diodes (CR1 to CR6) added for protective purposes. CR1 should be used if the output voltage is less than 20 volts and CR2, CR3 are absent. For V_O higher than 20 volts, CR1 should be discarded in favor of CR2 and CR3. Diode CR4 prevents IC failure if the series pass transistors develop collector-base shorts while the main power transistor suffers a simultaneous open emitter. If the possibility of such a transistor failure mode seems remote, CR4 may be deleted. To prevent instantaneous differential and common mode breakdown of the current sense amplifier, CR5 must be placed across the current limit resistor R_S .

Load transients occasionally produce a damaging reversal of current flow from output to input $V_O > 150$ volts (which will destroy the IC). Diode CR6 prevents such reversal and renders the circuit immune from destruction for such conditions, e.g., adding a large output capacitor after the supply is turned "on". Diodes CR1, CR2, CR3, and CR5 may be general purpose silicon units such as 1N4001 or equivalent whereas CR4 and CR6 should have a peak inverse voltage rating equal to V_{in} or greater.

APPLICATIONS

Figure 2 shows a typical 0-to-40 volts, 0.5-ampere regulator with better than 0.01% performance. The RC network between pins 5 and 6 and the capacitor between pins 13 and 14 provide frequency compensation for the MC1466. The external pass transistors are used to boost load current, since the output current of the regulator is less than 2 mA.

MC1466L

Figure 1 is a 0-to-15 volts, 10-ampere regulator with the pass transistor configuration necessary to boost the load current to 10 amperes. Note that C_O has been increased to 1000 μF following the general rule:

$$C_O = 100 \mu\text{F}/A I_L$$

The prime advantage of the MC1466 is its use as a high voltage regulator, as shown in Figure 3. This 0-to-250 volts 0.1-ampere regulator is typical of high voltage applications, limited only by the breakdown and safe areas of the output pass transistors.

The primary limiting factor in high voltage series regulators is the pass transistor. Figure 13 shows a safe area curve for the MJ413. Looking at Figure 3, we see that if the output is shorted, the transistor will have a collector current of 100 mA, with a V_{CE} approximately equal to 260 volts. Thus this point falls on the dc line of the safe area curve, insuring that the transistor will not enter secondary breakdown.

In this respect (Safe Operating Area) the foldback circuit of Figure 14 is superior for handling high voltages and yet is short-circuit protected. This is due to the fact that load current is diminished as output voltage drops (V_{CE} increases as V_O drops) as seen in Figure 15. By careful design the load current at a short, I_{SC} can be made low enough such that the combined V_{CE} (V_{in}) and I_{SC} still falls within the dc safe operating area of the transistor. For the illustrated design (Figure 14), an input voltage of 210 volts is com-

patible with a short circuit current of 100 mA. Yet current foldback allows us to design for a maximum regulated load current of 500 mA. the pertinent design equations are:

$$\text{Let } R_2 \text{ (k}\Omega\text{)} = V_O$$

$$\alpha = \frac{0.25}{V_O} \left[\frac{I_k}{I_{SC}} - 1 \right]$$

$$R_1 \text{ (k}\Omega\text{)} = \frac{\alpha}{1 - \alpha} V_O$$

$$R_{SC} = \frac{0.25}{(1 - \alpha) I_{SC}}$$

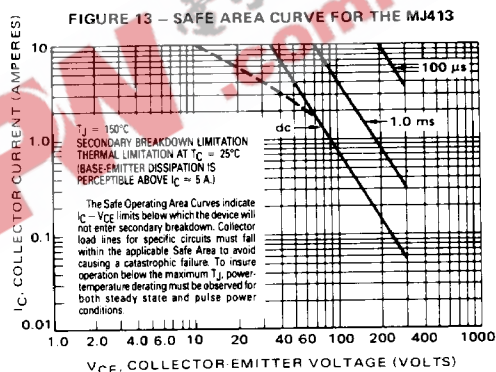
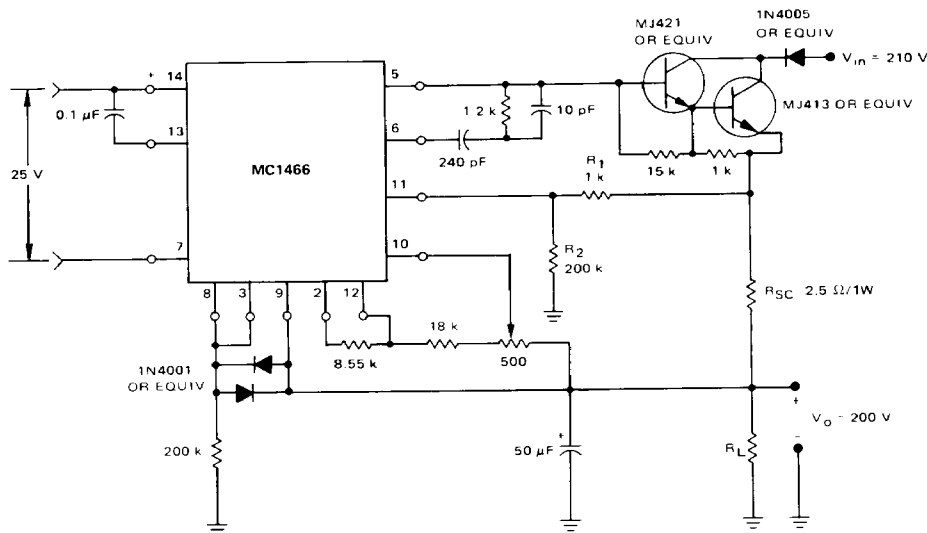


FIGURE 14 - A 200 V, 0.5-AMPERE REGULATOR WITH CURRENT FOLDBACK



MC1466L

The terms I_{SC} and I_k correspond to the short-circuit current and maximum available load current as shown in Figure 15.

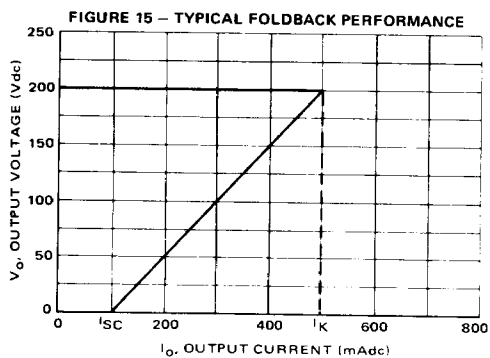


Figure 16 shows a remote sense application which should be used when high current or long wire lengths are used. This type of wiring is recommended for any application where the best possible regulation is desired. Since the sense lines draw only a small current, large voltage drops do not destroy the excellent regulation of the MC1466.

TRANSIENT FAILURES

In industrial areas where electrical machinery is used

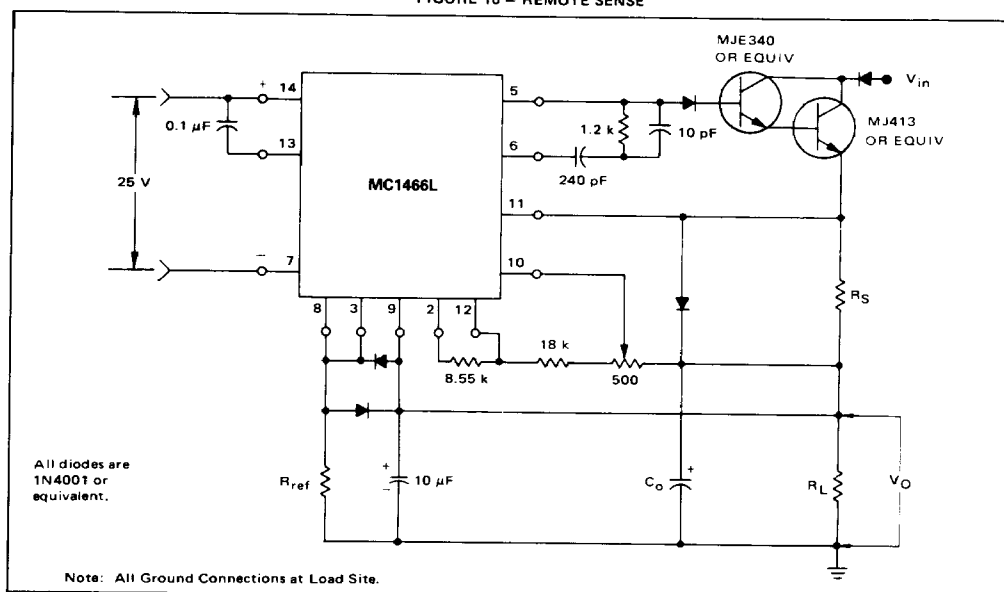
the normal ac line often contains bursts of voltage running from hundreds to thousands of volts in magnitude and only microseconds in duration. Under some conditions this energy is dissipated across the internal zener connected between pins 9 and 7. This transient condition may produce a total failure of the regulator device without any apparent explanation. This type of failure is identified by absence of the 7 volt zener (CR1) between pin 9 and pin 7. To prevent this failure mode the use of a shielded power transformer is recommended, as shown in Figure 6. In addition, it is recommended that C1, C3 and C4 be included to aid in transient repression. These capacitors should have good high frequency characteristics.

If the possibility of transients on the output exists, the addition of a resistor and zener diode between pins 9 and 7 as shown on Figure 17 should be added.

VOLTAGE/CURRENT MODE INDICATOR

There may be times when it is desirable to know when the MC1466 is in the constant current mode or constant voltage mode. A mode indicator signal circuit can be easily added to provide this feature. Figure 18 shows how a PNP transistor has replaced a protection diode between pins 8 and 9 of Figure 2. When the MC1466 goes from constant voltage mode to constant current mode, V_O will drop below V_g and the PNP transistor will turn on. The 1 mA current supplied by pin 8 will now be shunted to base of Q1 thereby providing a mode signal output.

FIGURE 16 – REMOTE SENSE



MC1466L

FIGURE 17 - A 0-TO-250 VOLT, 0.1-AMPERE REGULATOR

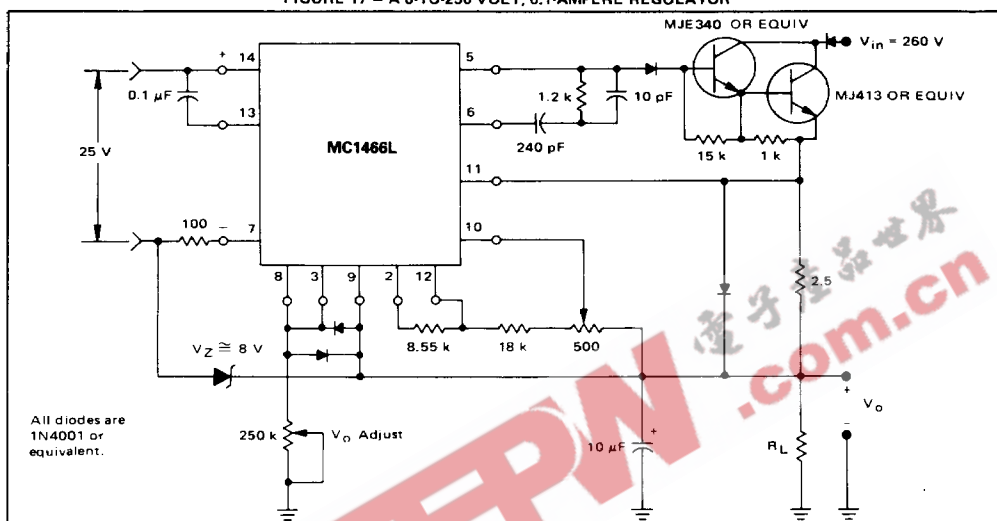
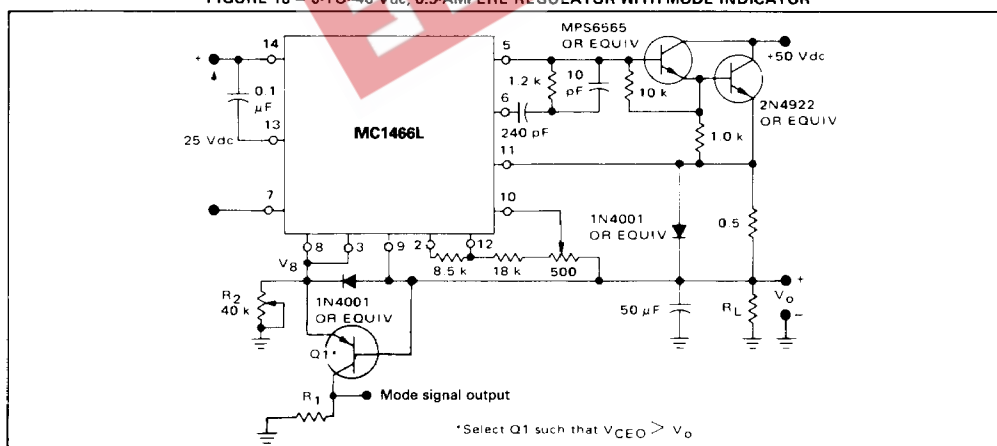


FIGURE 18 - 0-TO-40 Vdc, 0.5-AMPERE REGULATOR WITH MODE INDICATOR



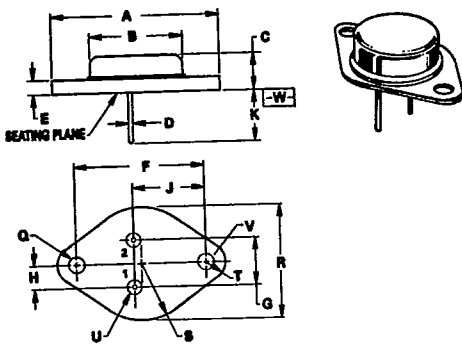
SECTION 19
PACKAGE OUTLINE DIMENSIONS

T-90-20

**K SUFFIX
METAL PACKAGE
CASE 1-03**
 $R_{\theta JA} = 45^{\circ}\text{C/W (TYP)}$
(TO-3)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	—	22.23	—	0.875
C	0.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.48 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	7.92	—	0.312	—
Q	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.189
V	3.84	4.09	0.151	0.161

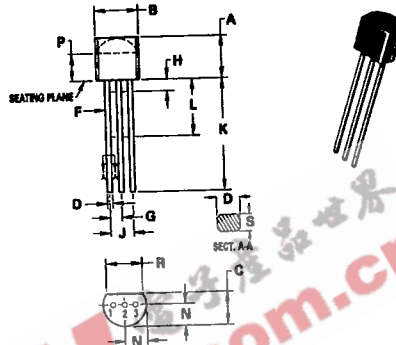
- NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
 $\text{M} \begin{matrix} \text{M} \\ \text{M} \end{matrix} \phi 0.25 (0.010) \text{ (M)} \text{ W} \begin{matrix} \text{V} \\ \text{V} \end{matrix} \text{ (M)}$
3. POSITIONAL TOLERANCE FOR LEADS:
 $\text{M} \begin{matrix} \text{M} \\ \text{M} \end{matrix} \phi 0.30 (0.012) \text{ (M)} \text{ W} \begin{matrix} \text{V} \\ \text{V} \end{matrix} \text{ (M)} \text{ U} \begin{matrix} \text{U} \\ \text{U} \end{matrix}$



**LP, P, Z SUFFIX
PLASTIC PACKAGE
CASE 29-04**
 $R_{\theta JA} = 200^{\circ}\text{C/W (TYP)}$
(TO-226AA/TO-92)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.20	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.55	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.15	1.39	0.045	0.055
H	—	2.54	—	0.100
J	2.42	2.68	0.095	0.105
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.04	2.68	0.080	0.105
P	2.93	—	0.115	—
R	3.43	—	0.135	—
S	0.39	0.50	0.015	0.020

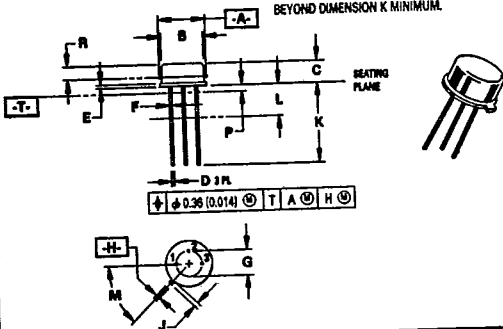
- NOTES:
1. CONTOUR OF PACKAGE BEYOND ZONE "P" IS UNCONTROLLED.
2. DIM "F" APPLIES BETWEEN "H" AND "L". DIM "D" & "S" APPLIES BETWEEN "L" & 12.70mm (0.5") FROM SEATING PLANE. LEAD DIM IS UNCONTROLLED IN "H" & BEYOND 12.70mm (0.5") FROM SEATING PLANE.
3. CONTROLLING DIM: INCH.



**G, H SUFFIX
METAL PACKAGE
CASE 79-05**
 $R_{\theta JA} = 185^{\circ}\text{C/W (TYP)}$
(TO-39)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.02	9.29	0.355	0.366
B	8.01	8.50	0.315	0.335
C	4.20	4.57	0.165	0.180
D	0.44	0.53	0.017	0.021
E	0.44	0.68	0.017	0.035
F	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.72	0.86	0.028	0.034
J	0.74	1.01	0.029	0.040
K	12.70	19.05	0.500	0.750
L	6.35	—	0.250	—
M	45° BSC		45° BSC	
P	—	1.27	—	0.050
R	2.54	—	0.100	—

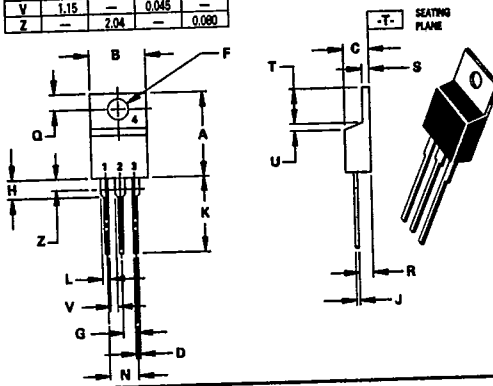
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION J MEASURED FROM DIMENSION A MAXIMUM.
4. DIMENSION B SHALL NOT VARY MORE THAN 0.25 (0.010) IN ZONE R. THIS ZONE CONTROLLED FOR AUTOMATIC HANDLING.
5. DIMENSION F APPLIES BETWEEN DIMENSION P AND L. DIMENSION D APPLIES BETWEEN DIMENSION L AND K. MINIMUM LEAD DIAMETER IS UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.



**KC, T SUFFIX
PLASTIC PACKAGE
CASE 221A-04**
 $R_{\theta JA} = 65^{\circ}\text{C/W (TYP)}$
(TO-220AB)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.81	3.73	0.142	0.147
G	2.42	2.68	0.095	0.105
H	2.90	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

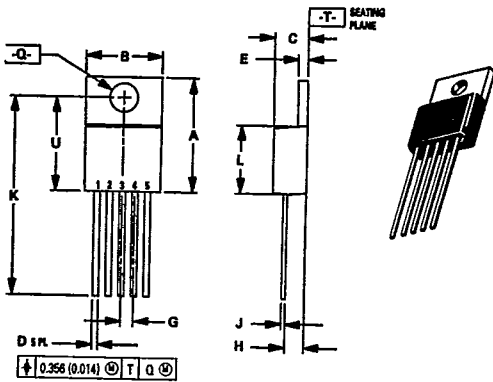


PACKAGE OUTLINE DIMENSIONS (continued)

**T SUFFIX
PLASTIC PACKAGE
CASE 314D-02**

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.529	15.570	0.572	0.613
B	9.938	10.541	0.390	0.415
C	4.318	4.572	0.170	0.180
D	0.635	0.965	0.025	0.038
E	1.169	1.397	0.046	0.055
G	1.702 BSC		0.067 BSC	
H	2.109	2.717	0.083	0.107
J	0.381	0.635	0.015	0.025
K	25.807	26.670	1.016	1.050
L	8.052	9.398	0.317	0.370
Q	3.556	3.937	0.140	0.155
U	11.889	12.827	0.468	0.505

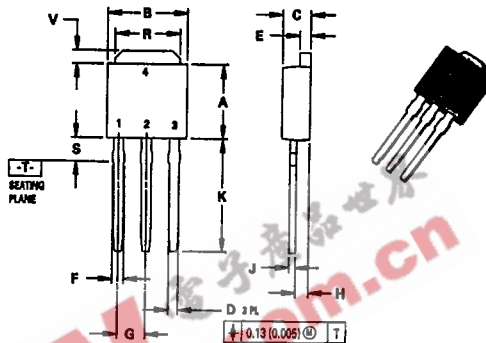
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.



**DT-1 SUFFIX
PLASTIC PACKAGE
CASE 369-03**

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.84	0.94	0.033	0.037
F	0.77	1.14	0.030	0.045
G	2.29 BSC		0.090 BSC	
H	0.97	1.06	0.038	0.042
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
R	5.21	5.46	0.205	0.215
S	1.91	2.29	0.075	0.090
V	0.89	1.27	0.035	0.050

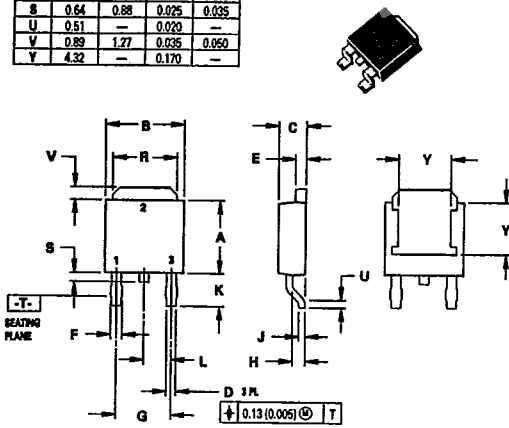
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.



**DT SUFFIX
PLASTIC PACKAGE
CASE 369A-03
DPAK**

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.84	0.94	0.033	0.037
F	0.77	1.14	0.030	0.045
G	4.58 BSC		0.180 BSC	
H	0.97	1.06	0.038	0.042
J	0.46	0.58	0.018	0.023
K	2.60	2.89	0.102	0.114
L	2.29 BSC		0.090 BSC	
R	5.21	5.46	0.205	0.215
S	0.64	0.88	0.025	0.035
U	0.51	—	0.020	—
V	0.89	1.27	0.035	0.050
Y	4.32	—	0.170	—

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

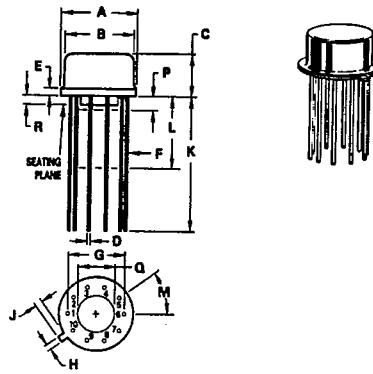


**H, G SUFFIX
METAL PACKAGE
CASE 603-04
RθJA = 160°C/W
(TO-100)**

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.51	0.305	0.335
C	4.19	4.70	0.165	0.186
D	0.407	0.533	0.016	0.021
E	—	1.02	—	0.040
F	0.406	0.483	0.016	0.019
G	5.84 BSC		0.230 BSC	
H	0.712	0.864	0.028	0.034
J	0.737	1.14	0.029	0.045
K	12.70	—	0.500	—
L	6.35	12.70	0.250	0.500
M	36° BSC		36° BSC	
P	—	1.27	—	0.050
Q	3.56	4.06	0.140	0.160
R	0.254	1.02	0.010	0.040

NOTE:
LEADS WITHIN 0.18 mm (0.007) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

All JEDEC Dimensions and Notes Apply.

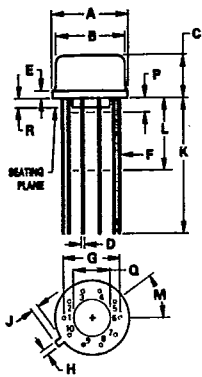


PACKAGE OUTLINE DIMENSIONS (continued)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.51	0.305	0.335
C	4.19	6.73	0.165	0.265
D	0.407	0.533	0.016	0.021
E	—	1.02	—	0.040
F	0.406	0.483	0.016	0.019
G	5.84 BSC	—	0.230 BSC	—
H	0.712	0.854	0.028	0.034
J	0.737	1.14	0.029	0.045
K	12.70	—	0.500	—
L	6.35	12.70	0.250	0.500
M	36° BSC	—	36° BSC	—
P	—	1.27	—	0.050
Q	3.56	4.06	0.140	0.160
R	0.254	1.02	0.010	0.040

**G SUFFIX
METAL PACKAGE
CASE 603C-01**
R θ JA = 150°C/W (TYP)
(TO-100)

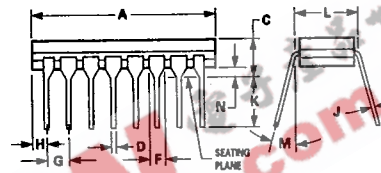
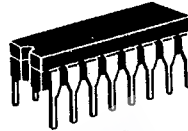
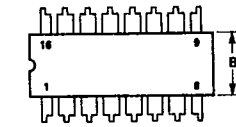
- NOTES:
1. LEADS WITHIN 0.18 mm (0.007) RADIUS OF TRUE POSITION TO DIM. "A" & "H" AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. LEAD DIA UNCONTROLLED BEYOND DIM "K" MIN.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.43	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC	—	0.100 BSC	—
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC	—	0.300 BSC	—
M	—	15°	—	15°
N	0.51	1.02	0.020	0.040

**DP2, D, J, L, N SUFFIX
CERAMIC PACKAGE
CASE 620-10**
R θ JA = 100°C/W (TYP)

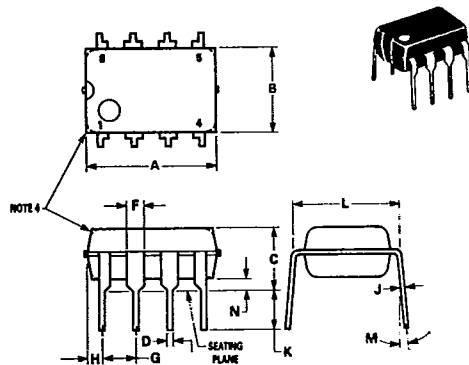
- NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PACKAGE INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIM "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.
5. DIM "F" MAY NARROW TO 0.76 mm (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.



**N, P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05**
R θ JA = 100°C/W (TYP)

- NOTES:
1. LEAD POSITIONAL TOLERANCE:
 ± 0.13 (0.005) T A B
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
4. DIMENSIONS A AND B ARE DATUMS.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

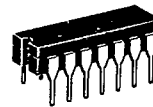
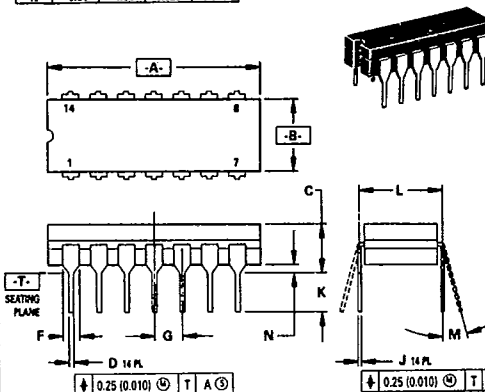
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.50	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC	—	0.100 BSC	—
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC	—	0.300 BSC	—
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040



**L SUFFIX
CERAMIC PACKAGE
CASE 632-08**
R θ JA = 100°C/W (TYP)
(TO-116)

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.23	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.39	0.50	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC	—	0.100 BSC	—
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC	—	0.300 BSC	—
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

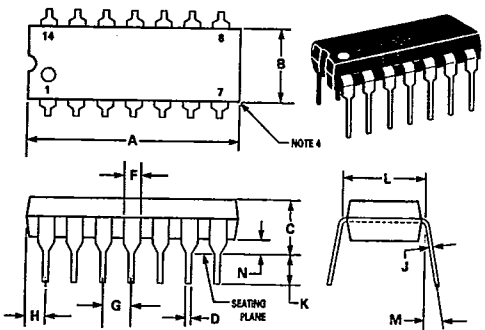


PACKAGE OUTLINE DIMENSIONS (continued)

**N, P, N-14, P2 SUFFIX
PLASTIC PACKAGE
CASE 646-06
R_{θJA} = 100°C/W (TYP)**

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.039

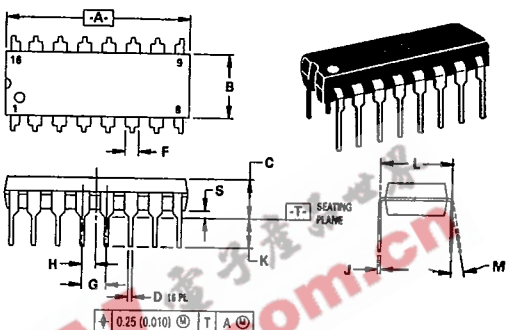
- NOTES:
 1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
 4. ROUNDED CORNERS OPTIONAL.



**N, P SUFFIX
PLASTIC PACKAGE
CASE 648-08
R_{θJA} = 100°C/W (TYP)**

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.56	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.60	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

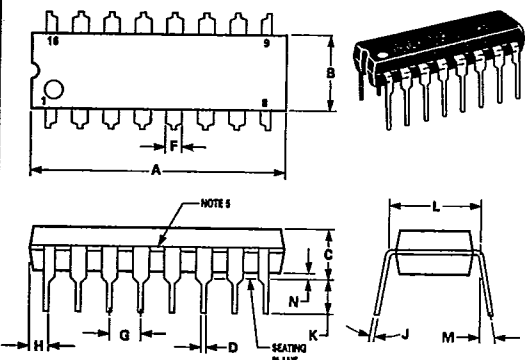
- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.



**P SUFFIX
PLASTIC PACKAGE
CASE 648C-02**

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.040

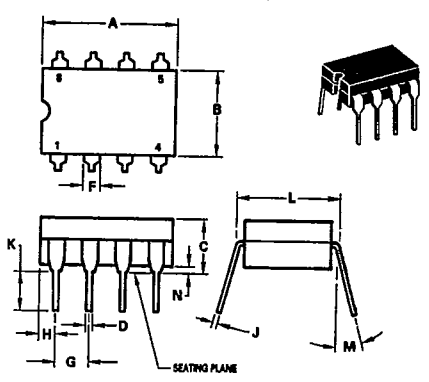
- NOTES:
 1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
 4. ROUNDED CORNERS OPTIONAL.
 5. EXTERNAL LEAD CONNECTION, BETWEEN 4 AND 5, 12 AND 13 AS SHOWN.



**J-8, J, JG, U, Z SUFFIX
CERAMIC PACKAGE
CASE 693-02
R_{θJA} = 100°C/W (TYP)**

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.91	10.92	0.390	0.430
B	6.22	6.89	0.245	0.275
C	4.32	5.08	0.170	0.200
D	0.41	0.51	0.016	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	1.14	1.65	0.045	0.065
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	—	15°	—	15°
N	0.51	1.02	0.020	0.040

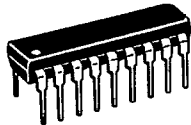
- NOTES:
 1. LEADS WITHIN 0.13 mm (0.005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.



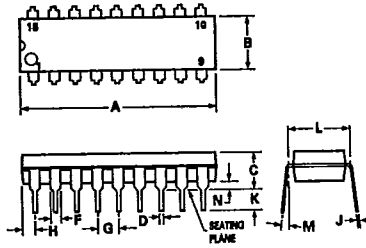
PACKAGE OUTLINE DIMENSIONS (continued)

**A, B, N, P SUFFIX
PLASTIC PACKAGE
CASE 707-02**
R θ JA = 100°C/W (TYP)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.38	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040



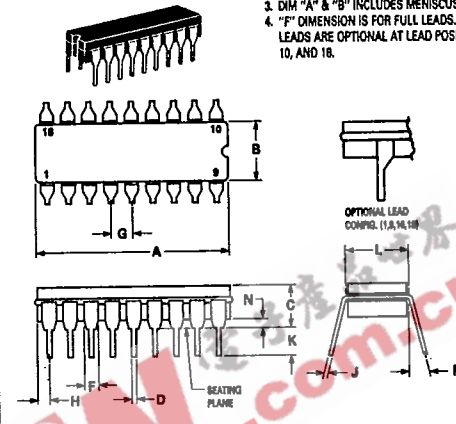
- NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
 2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.35	23.11	0.880	0.910
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

**J, L SUFFIX
CERAMIC PACKAGE
CASE 726-04**
R θ JA = 100°C/W (TYP)

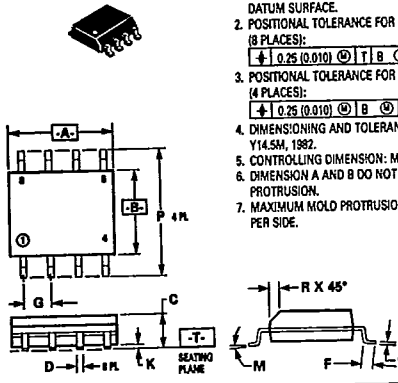
- NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
 2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. DIM "A" & "B" INCLUDES MENISCUS.
 4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.



**D SUFFIX
PLASTIC PACKAGE
CASE 751-03**
SO-8, SOP-8
R θ JA = 190°C/W (SO-8)
R θ JA = 160°C/W (SOP-8)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

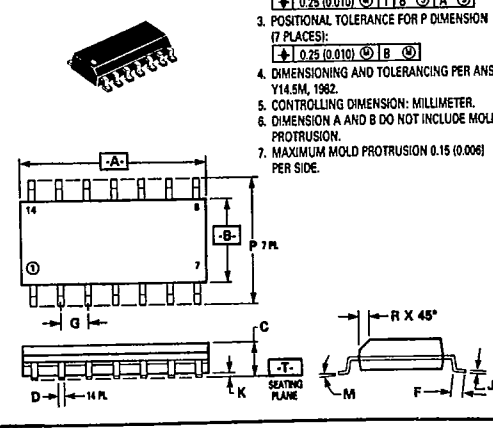
- NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
 2. POSITIONAL TOLERANCE FOR D DIMENSION (8 PLACES):
+0.25 (0.010) (M) T B (M) A (M)
 3. POSITIONAL TOLERANCE FOR P DIMENSION (4 PLACES):
+0.25 (0.010) (M) B (M)
 4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 5. CONTROLLING DIMENSION: MILLIMETER.
 6. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 7. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.



**D SUFFIX
PLASTIC PACKAGE
CASE 751A-02**
SO-14
R θ JA = 145°C/W (TYP)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

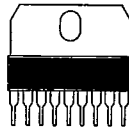
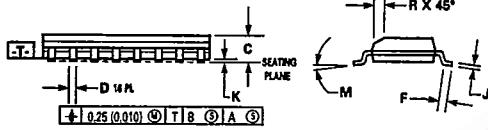
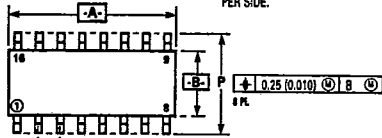
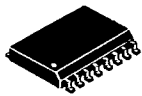
- NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
 2. POSITIONAL TOLERANCE FOR D DIMENSION (14 PLACES):
+0.25 (0.010) (M) T B (M) A (M)
 3. POSITIONAL TOLERANCE FOR P DIMENSION (7 PLACES):
+0.25 (0.010) (M) B (M)
 4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 5. CONTROLLING DIMENSION: MILLIMETER.
 6. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 7. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.



**DW SUFFIX
PLASTIC PACKAGE
CASE 751G-01
SO-16L**

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.25	2.65	0.083	0.104
D	0.25	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
	0.25	0.75	0.010	0.029

- NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
 2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 3. CONTROLLING DIMENSION: MILLIMETER.
 4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.



**CASE 762-01
PLASTIC MEDIUM
POWER PACKAGE
SIP-9**

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.40	23.00	0.877	0.907
B	8.40	8.80	0.332	0.347
C	3.45	3.65	0.136	0.143
D	0.40	0.55	0.016	0.021
E	0.25	0.40	0.009	0.015
F	1.40	1.60	0.055	0.062
G	2.54 BSC		0.100 BSC	
H	1.51	1.71	0.059	0.067
J	0.380	0.400	0.014	0.015
K	3.95	4.20	0.155	0.165
M	30° BSC		30° BSC	
N	2.50	2.70	0.099	0.106
O	3.15	3.45	0.124	0.136
R	13.80	13.90	0.543	0.547
S	1.65	1.95	0.065	0.076
U	23.00	22.20	0.905	0.874
V	0.55	0.75	0.021	0.029
W	2.89 BSC		0.113 BSC	
X	0.85	0.75	0.033	0.029
Y	2.70	2.80	0.106	0.110

- NOTES:
1. DIMENSIONS A AND C ARE DATUMS AND T IS A DATUM PLANE.
 2. POSITIONAL TOLERANCE FOR LEAD DIMENSION D: $\pm 0.25 (0.010) \text{ } \textcircled{D} \text{ } \textcircled{T} \text{ } \textcircled{A} \text{ } \textcircled{M}$
 3. POSITIONAL TOLERANCE FOR LEAD DIMENSION J: $\pm 0.25 (0.010) \text{ } \textcircled{J} \text{ } \textcircled{T} \text{ } \textcircled{C} \text{ } \textcircled{M}$
 4. POSITIONAL TOLERANCE FOR LEAD DIMENSION G: $\pm 0.25 (0.010) \text{ } \textcircled{G} \text{ } \textcircled{T} \text{ } \textcircled{A} \text{ } \textcircled{M}$
 5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
 6. CONTROLLING DIMENSION: MILLIMETER.

