

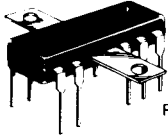
\*MC660 P,L Series (-30°C to +75°C)

\*MC660TL Series (-55°C to +125°C)

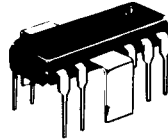
Motorola's MHTL integrated circuits are especially designed to meet the requirements of industrial applications because of the outstanding noise immunity. MHTL circuits provide error-free operation in high noise environments far beyond the tolerance of other integrated circuit families. Multifunction packages and broad operating temperature range further tailor this device family to the industrial designer's requirements.

\*MHTL ceramic dual in-line devices are available with specification over the -55°C to +125°C temperature range and/or with hi-rel processing on special order. See your Motorola representative for pricing.

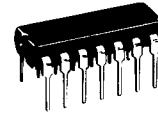
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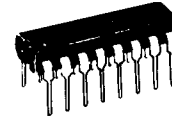
P SUFFIX  
PLASTIC PACKAGE  
CASE 675



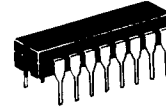
PC SUFFIX  
PLASTIC PACKAGE  
CASE 676



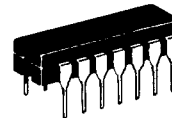
P SUFFIX  
PLASTIC PACKAGE  
CASE 646



P SUFFIX  
PLASTIC PACKAGE  
CASE 648



TL, L SUFFIX  
CERAMIC PACKAGE  
CASE 620



TL, L SUFFIX  
CERAMIC PACKAGE  
CASE 632

### FUNCTIONS AND CHARACTERISTICS ( $V_{CC} = 15 V \pm 1.0 V_{dc}$ , $T_A = 25^\circ C$ )

Function	Type	Loading Factor Each Output	Propagation Delay ns typ	Power Dissipation mW typ/pkg	Case
Expandable Dual 4-Input NAND Gate (active pullup)	MC660	10	110	88/26 ②	632,646
Expandable Dual 4-Input NAND Gate (passive pullup)	MC661	10	125	88/26 ②	632,646
Expandable Dual 4-Input Line Driver (NAND)	MC662	30	140	180/26 ②	632,646
Dual J-K Flip-Flop	MC663	9	3.0 MHz ③	200	632,646
Master-Slave R-S Flip-Flop	MC664	8	3.0 MHz ③	160	632,646
Triple Level Translator	MC665	MDTL = 8 MTTL III = 5.5 MRTL = 5	40	83 (MDTL) 104 (MRTL)	632,646
Triple Level Translator	MC666	10	75	105	632,646
Dual Monostable Multivibrator	MC667	10	140	240	632,646
Quad 2-Input NAND Gate (passive pullup)	MC668	10	125	176/52 ②	632,646
Dual 4-Input Expander	MC669	-	-	-	632,646
Triple 3-Input NAND Gate (passive pullup)	MC670	10	125	132/39 ②	632,646
Triple 3-Input NAND Gate (active pullup)	MC671	10	110	132/39 ②	632,646
Quad 2-Input NAND Gate (active pullup)	MC672	10	110	176/52 ②	632,646
Dual 2-Input AND-OR-INVERT Gate (active pullup)	MC673	10	110	160/50 ②	632,646
Dual 2-Input AND-OR-INVERT Gate (passive pullup)	MC674	10	125	160/50 ②	632,646
Dual Pulse Stretcher/Multivibrator	MC675	10	150 (pins 1,6) 110 (pins 5,6)	180	632,646
BCD-To-Decimal Decoder-Driver	MC676	-	500	380	620,648
Hex Inverter With Strobe (active pullup)	MC677	10	110	246/96 ②	620,648
Hex Inverter With Strobe (without output resistors)	MC678	10	125	192/96 ②	620,648
Dual Lamp/Line Driver	MC679,B	125	0.5 $\mu s$ typ	250/30 ②	632,646
Hex Inverter (active pullup)	MC680	10	110	246/96 ②	632,646
Hex Inverter (open collector)	MC681	10	125	192/96 ②	632,646
Quad Latch	MC682	10	250	375	620,648
Quad 2-Input Exclusive OR Gate	MC683	10	-	380	632,646
Decade Counter	MC684	10	0.5 MHz ③	480	620,648
Binary Counter	MC685	10	0.5 MHz ③	480	620,648
4-Bit Shift Register	MC686	10	0.5 MHz ③	480	620,648
Dual J-K Flip-Flop	MC688	10	2.5 MHz ③	375	620,648
Hex Inverter (high voltage)	MC689	10	150	173/55 ②	632,646
Hex Inverter (active pullup)	MC690	10	150	173/55 ②	632,646
Hex Inverter/Interface Element	MC691	10	300	500/150 ②	632,646
250 mA Quad 2-Input NAND Gate (Schmitt Trigger)	MC693	200	400	300	620,648
Dual Interface Element, Line Driver/Receiver (Schmitt Trigger)	MC696	10 @ 10 V $V_{CC}$ 15 @ 25 V $V_{CC}$	400	225/60 ②	620,648
Hex Inverter (Passive Pull-up)	MC697	10	125	246/96 ②	632,646
500 mA Dual 2-Input AND Gate (Schmitt Trigger)	MC699	400	400	450	675,676

① L suffix denotes Dual In-Line Ceramic Package, P denotes Dual In-Line Plastic Package (i.e., MC660L = Dual In-Line Ceramic, MC660P = Dual In-Line Plastic Package)

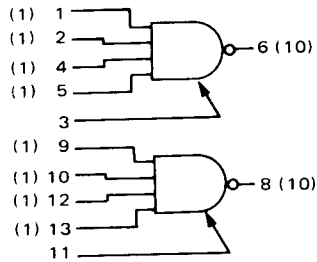
②  $t_{OH}$  High Input Low

③  $f_{Tog}$

# MHTL LOGIC DIAGRAMS

## GATES

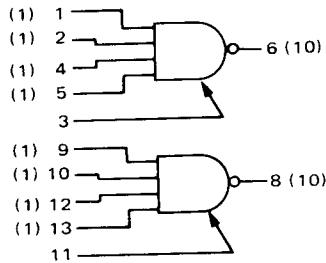
**MC660**  
Expandable  
Dual 4-Input NAND Gate  
(active output pullup)



$$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5} \cdot [3]$$

$t_{pd} = 110 \text{ ns typ}$   
 $P_D = 88 \text{ mW typ/pkg (Inputs High)}$   
 $26 \text{ mW typ/pkg (Input Low)}$

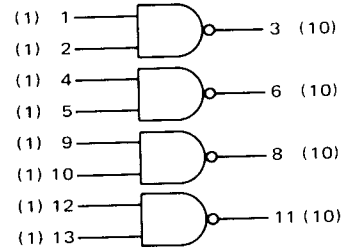
**MC661**  
Expandable  
Dual 4-Input NAND Gate  
(passive output pullup)



$$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5} \cdot [3]$$

$t_{pd} = 125 \text{ ns typ}$   
 $P_D = 88 \text{ mW typ/pkg (Inputs High)}$   
 $26 \text{ mW typ/pkg (Input Low)}$

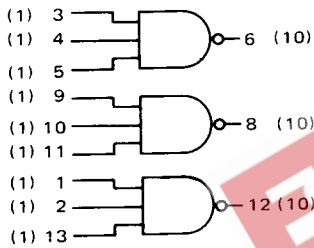
**MC668**  
Quad 2-Input NAND Gate  
(passive output pullup)



$$3 = \overline{1 \cdot 2}$$

$t_{pd} = 125 \text{ ns typ}$   
 $P_D = 176 \text{ mW typ/pkg (Inputs High)}$   
 $52 \text{ mW typ/pkg (Input Low)}$

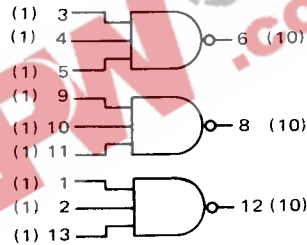
**MC670**  
Triple 3-Input NAND Gate  
(passive output pullup)



$$6 = \overline{3 \cdot 4 \cdot 5}$$

$t_{pd} = 125 \text{ ns typ}$   
 $P_D = 132 \text{ mW typ/pkg (Inputs High)}$   
 $39 \text{ mW typ/pkg (Input Low)}$

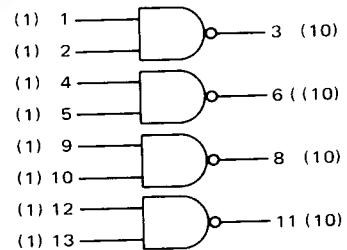
**MC671**  
Triple 3-Input NAND Gate  
(active output pullup)



$$6 = \overline{3 \cdot 4 \cdot 5}$$

$t_{pd} = 110 \text{ ns typ}$   
 $P_D = 132 \text{ mW typ/pkg (Inputs High)}$   
 $39 \text{ mW typ/pkg (Input Low)}$

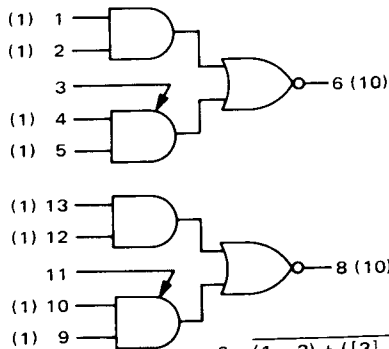
**MC672**  
Quad 2-Input NAND Gate  
(active output pullup)



$$3 = \overline{1 \cdot 2}$$

$t_{pd} = 110 \text{ ns typ}$   
 $P_D = 176 \text{ mW typ/pkg (Inputs High)}$   
 $52 \text{ mW typ/pkg (Input Low)}$

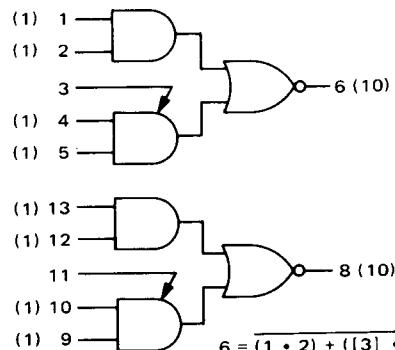
**MC673**  
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate  
(active output pullup)



$$6 = \overline{(1 \cdot 2) + ([3] \cdot 4 \cdot 5)}$$

$t_{pd} = 110 \text{ ns typ}$   
 $P_D = 160 \text{ mW typ/pkg (Inputs High)}$   
 $50 \text{ mW typ/pkg (Input Low)}$

**MC674**  
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate  
(passive output pullup)



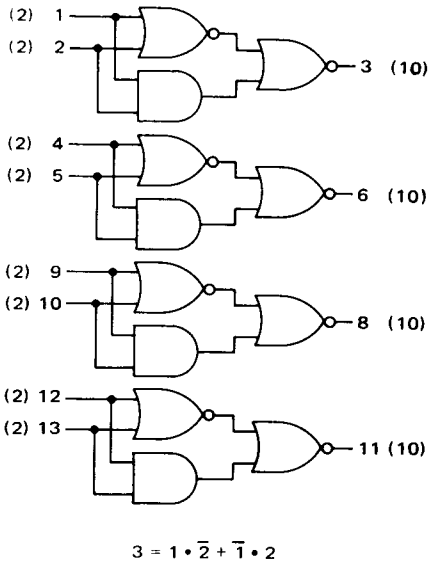
$$6 = \overline{(1 \cdot 2) + ([3] \cdot 4 \cdot 5)}$$

$t_{pd} = 125 \text{ ns typ}$   
 $P_D = 160 \text{ mW typ/pkg (Inputs High)}$   
 $50 \text{ mW typ/pkg (Input Low)}$

Numbers at ends of terminals represent pin numbers.  
 Numbers in parenthesis indicate loading.  
 (V<sub>CC</sub> = Pin 14, Gnd = Pin 7 for Case 646 and 632; V<sub>CC</sub> = Pin 16, Gnd = Pin 8 for Case 648 and 620.)

### GATES (continued)

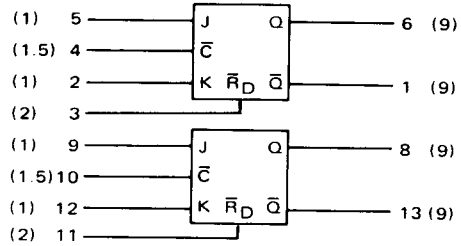
**MC683**  
 Quad 2-Input Exclusive OR



P<sub>D</sub> = 380 mW typ/pkg

### FLIP-FLOPS

**MC663**  
 Dual J-K Flip-Flop



f<sub>Tog</sub> = 3.0 MHz typ  
 P<sub>D</sub> = 200 mW typ/pkg

TRUTH TABLE

t <sub>n</sub>		t <sub>n+1</sub>	
J	K	Q	Q̄
0	0	Q <sub>n</sub>	Q̄ <sub>n</sub>
1	0	1	0
0	1	0	1
1	1	Q̄ <sub>n</sub>	Q <sub>n</sub>

Direct input ( $\bar{R}_D$ ) must be high.

- 0 = low state
- 1 = high state

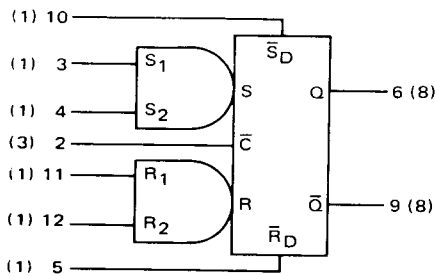
t<sub>n</sub> = time period prior to negative transition of clock pulse

t<sub>n+1</sub> = time period subsequent to negative transition of clock pulse

Q<sub>n</sub> = state of Q output in time period t<sub>n</sub>

NOTE: A low state "0" at the direct reset  $\bar{R}_D$  causes a low state "0" at the Q output and the complement at the  $\bar{Q}$  output.

**MC664**  
 Master-Slave R-S Flip-Flop



f<sub>Tog</sub> = 3.0 MHz typ  
 P<sub>D</sub> = 160 mW typ/pkg

DIRECT INPUT OPERATION

$\bar{R}_D$	$\bar{S}_D$	Q	Q̄
1	1	NC	NC
1	0	1	0
0	1	0	1
0	0	NA	NA

Clock Input ( $\bar{C}$ ) must be low

- 0 = low state
- 1 = high state

NC = No change  
 NA = Not allowed

X = state of input does not affect state of the circuit  
 U = indeterminate state

t<sub>n</sub> = time period prior to negative transition of clock pulse

t<sub>n+1</sub> = time period subsequent to negative transition of clock pulse

Q<sub>n</sub> = state of Q output in time period t<sub>n</sub>

CLOCKED OPERATION

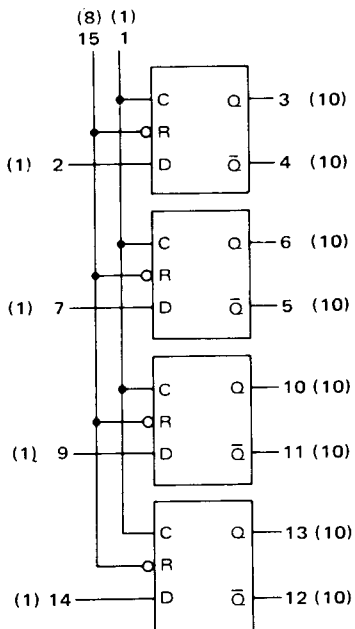
t <sub>n</sub>		t <sub>n+1</sub>		
S <sub>1</sub>	S <sub>2</sub>	R <sub>1</sub>	R <sub>2</sub>	Q
0	X	0	X	Q <sub>n</sub>
0	X	X	0	Q <sub>n</sub>
X	0	0	X	Q <sub>n</sub>
X	0	X	0	Q <sub>n</sub>
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

Direct inputs ( $\bar{R}_D$ ,  $\bar{S}_D$ ) must be high.

(continued)

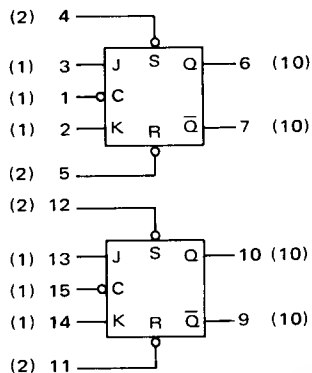
## FLIP-FLOPS (continued)

**MC682**  
Quad Latch



$t_{pd} = 250 \text{ ns typ}$   
 $P_D = 375 \text{ mW typ/pkg}$

**MC688**  
Dual J-K Flip-Flop



**TRUTH TABLE**

R	S	$t_n$		$t_{n+1}$	
		J	K	Q	$\bar{Q}$
0	1	x	x	0	1
1	0	x	x	1	0
1	1	0	0	$Q_n$	$\bar{Q}_n$
1	1	1	1	$\bar{Q}_n$	$Q_n$

0 = Low state

1 = High state

x = Don't care

$t_n$  = Time period prior to negative transition of clock pulse.

$t_{n+1}$  = Time period subsequent to negative transition of clock pulse.

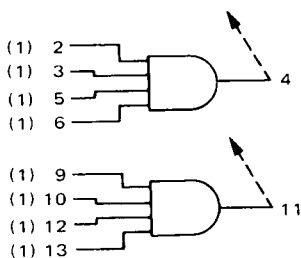
$Q_n$  = State of Q output in time period  $t_n$ .

\* = Clock pulse must be in low state

$f_{Tog} = 2.5 \text{ MHz typ}$   
 $P_D = 375 \text{ mW typ/pkg}$

## EXPANDER

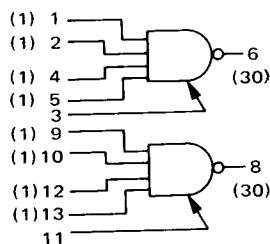
**MC669**  
Dual 4-Input Expander



$$4 = 2 \cdot 3 \cdot 5 \cdot 6$$

## DRIVERS

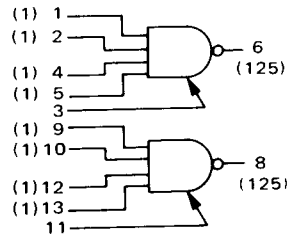
**MC662**  
Expandable  
Dual 4-Input Line Driver  
(active output pullup)



$$6 = 1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]$$

$t_{pd} = 140 \text{ ns typ}$   
 $P_D = 180 \text{ mW typ/pkg (Inputs High)}$   
 $26 \text{ mW typ/pkg (Input Low)}$

**MC679, MC679B**  
Dual Lamp Driver

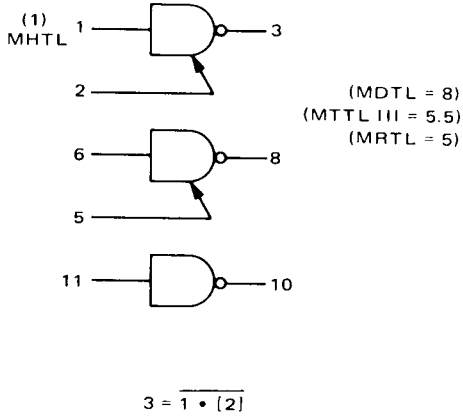


$$6 = 1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]$$

$t_{pd} = 0.5 \mu\text{s typ}$   
 $P_D = 250 \text{ mW (Inputs High)}$   
 $30 \text{ mW (Input Low)}$

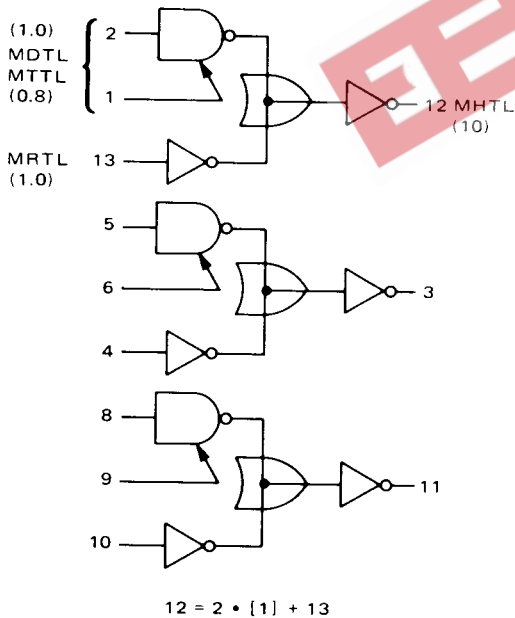
# TRANSLATORS

**MC665**  
Triple Level Translator



$t_{pd} = 40 \text{ ns typ}$   
 $P_D = 83 \text{ mW typ/pkg (MDTL)}$   
 $104 \text{ mW typ/pkg (MRTL)}$

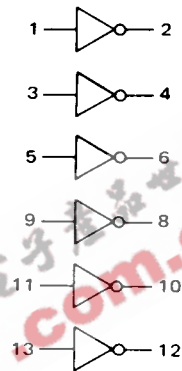
**MC666**  
Triple Level Translator



$t_{pd} = 75 \text{ ns typ}$   
 $P_D = 105 \text{ mW typ/pkg}$

# INVERTERS

**MC691**  
Hex Inverter/Translator  
(low level to high level)



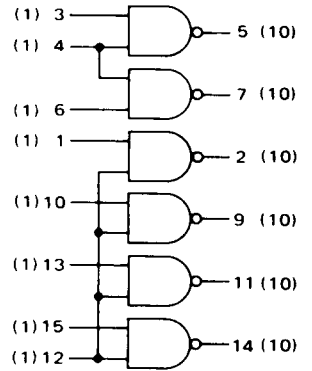
Positive Logic:  $2 = \bar{1}$

Input Loading Factor = 0.4  
Output Loading Factor = 10  
Propagation Delay Time:

$t_{+-} = 150 \text{ ns typ}$   
 $t_{+} = 300 \text{ ns typ}$

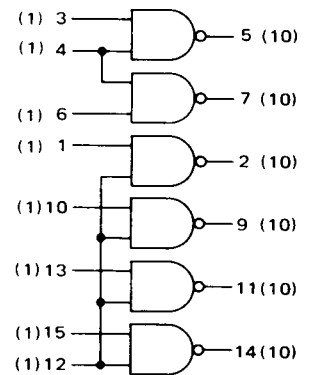
Typical Total Power Dissipation:  
Inputs High = 500 mW typ/pkg  
Input Low = 150 mW typ/pkg

**MC677**  
Hex Inverter With/Strobe  
(active pullup)



$t_{pd} = 110 \text{ ns typ}$   
 $P_D = 246 \text{ mW typ/pkg (Inputs High)}$   
 $96 \text{ mW typ/pkg (Input Low)}$

**MC678**  
Hex Inverter With/Strobe  
(without output resistors)



























$t_{pd} = 125 \text{ ns typ}$   
 $P_D = 192 \text{ mW typ/pkg (Inputs High)}$   
 $96 \text{ mW typ/pkg (Inputs Low)}$

(continued)















# MHTL LOGIC DIAGRAMS

## INVERTERS (continued)

<p><b>MC680</b> Hex Inverter (active pullup)</p> <p>(1) 1 —  — 2 (10)</p> <p>(1) 3 —  — 4 (10)</p> <p>(1) 5 —  — 6 (10)</p> <p>(1) 9 —  — 8 (10)</p> <p>(1) 11 —  — 10 (10)</p> <p>(1) 13 —  — 12 (10)</p> <p style="text-align: right;"><math>2 = \bar{1}</math></p> <p><math>t_{pd} = 110 \text{ ns typ}</math>  <math>P_D = 246 \text{ mW typ/pkg (Inputs High)}</math>  <math>96 \text{ mW typ/pkg (Input Low)}</math></p>	<p><b>MC681</b> Hex Inverter (open collector)</p> <p>(1) 1 —  — 2 (10)</p> <p>(1) 3 —  — 4 (10)</p> <p>(1) 5 —  — 6 (10)</p> <p>(1) 9 —  — 8 (10)</p> <p>(1) 11 —  — 10 (10)</p> <p>(1) 13 —  — 12 (10)</p> <p style="text-align: right;"><math>2 = \bar{1}</math></p> <p><math>t_{pd} = 125 \text{ ns typ}</math>  <math>P_D = 192 \text{ mW typ/pkg (Inputs High)}</math>  <math>96 \text{ mW typ/pkg (Input Low)}</math></p>
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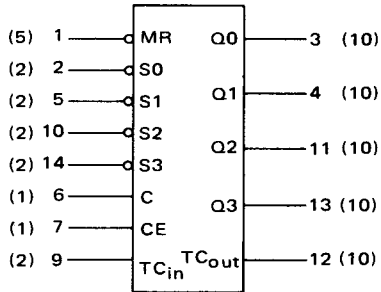
<p><b>MC689</b> Hex Inverter (high voltage)</p> <p>(1) 1 —  — 2 (10)</p> <p>(1) 3 —  — 4 (10)</p> <p>(1) 5 —  — 6 (10)</p> <p>(1) 9 —  — 8 (10)</p> <p>(1) 11 —  — 10 (10)</p> <p>(1) 13 —  — 12 (10)</p> <p style="text-align: right;"><math>2 = \bar{1}</math></p> <p><math>t_{pd} = 150 \text{ ns typ}</math>  <math>P_D = 173 \text{ mW typ/pkg (Inputs High)}</math>  <math>55 \text{ mW typ/pkg (Inputs Low)}</math></p>	<p><b>MC690</b> Hex Inverter (active pullup)</p> <p>(1) 1 —  — 2 (10)</p> <p>(1) 3 —  — 4 (10)</p> <p>(1) 5 —  — 6 (10)</p> <p>(1) 9 —  — 8 (10)</p> <p>(1) 11 —  — 10 (10)</p> <p>(1) 13 —  — 12 (10)</p> <p style="text-align: right;"><math>2 = \bar{1}</math></p> <p><math>t_{pd} = 150 \text{ ns typ}</math>  <math>P_D = 173 \text{ mW typ/pkg (Inputs High)}</math>  <math>55 \text{ mW typ/pkg (Inputs Low)}</math></p>
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## MULTIVIBRATORS

<p><b>MC667</b> Dual Monostable Multivibrator</p> <p>(1) 1 —  — 2 (10)</p> <p>0 — 6 (10)</p> <p>(1) 13 —  — 12 (10)</p> <p>0 — 8 (10)</p> <p><math>t_{pd} = 140 \text{ ns typ}</math>  <math>P_D = 240 \text{ mW typ/pkg}</math></p>	<p><b>MC675</b> Dual Pulse Stretcher/Multivibrator</p> <p>(1) 1 —  —  — 6 (10)</p> <p>(1) 2 —  —  — 6 (10)</p> <p>(1) 5 —  —  — 6 (10)</p> <p>(1) 12 —  —  — 8 (10)</p> <p>(1) 13 —  —  — 8 (10)</p> <p>(1) 9 —  —  — 8 (10)</p> <p><math>t_{pd} = 150 \text{ ns typ (Pins 1, 6)}</math>  <math>110 \text{ ns typ (Pins 5, 6)}</math>  <math>P_D = 180 \text{ mW typ/pkg}</math></p>
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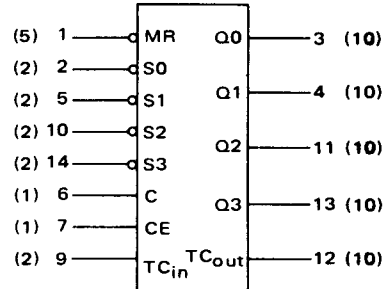
## COUNTERS

**MC684**  
Decade Counter



$f_{Tog} = 0.5 \text{ MHz min}$   
 $P_D = 480 \text{ mW typ/pkg}$

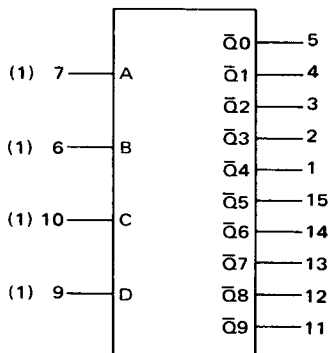
**MC685**  
Binary Counter



$f_{Tog} = 0.5 \text{ MHz min}$   
 $P_D = 480 \text{ mW typ/pkg}$

## DECODER

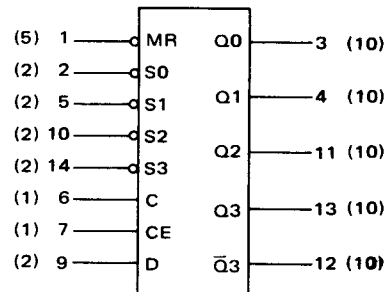
**MC676**  
BCD-To-Decimal Decoder-Driver



$t_{pd} = 500 \text{ ns Typ}$   
Power Dissipation = 380 mW typ/pkg

## SHIFT REGISTER

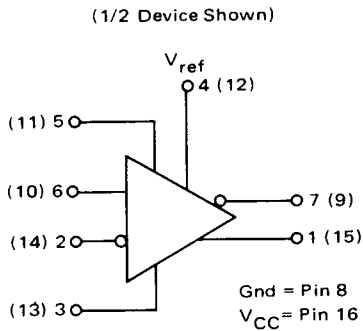
**MC686**  
4-Bit Shift Register



$f_{Tog} = 0.5 \text{ MHz min}$   
 $P_D = 480 \text{ mW typ/pkg}$

## — LINE DRIVER/RECEIVER

**MC696**  
Dual Interface Element,  
Line Driver/Receiver



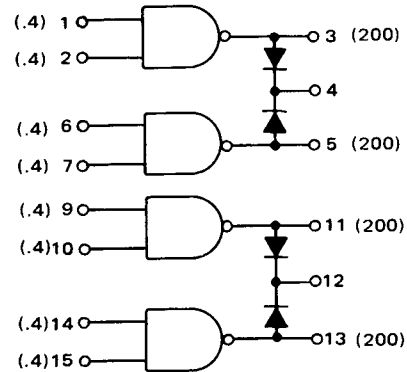
Numbers in parenthesis denotes pin numbers for other half of device.

$t_{pd} = 400 \text{ ns typ}$   
 $P_D = 225 \text{ mW typ/pkg (Inputs High)}$   
 $96 \text{ mW typ/pkg (Inputs Low)}$

## DRIVERS

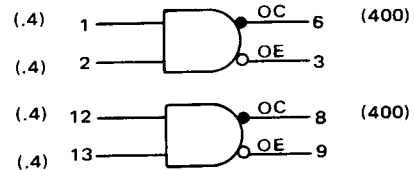
**MC693**

**250 mA Quad 2-Input NAND Driver**  
(open collector, high voltage output with inductive load clamp)  
(Schmitt Trigger Inputs)



$t_{pd} = 400 \text{ ns Typ}$   
 $P_D = 300 \text{ mW Typ/Pkg.}$

**MC699**  
**500 mA Dual 2-Input AND Gate/Driver**  
(high voltage output)  
(Schmitt Trigger Inputs)



OE = Open Emitter  
 OC = Open Collector

Positive Logic (with Pin 3 at Gnd):  $6 = 1 \cdot 2$   
 Input Loading Factor =  $0.415^*$   
 Propagation Delay Time =  $360 \text{ ns typ}^*$   
 Typical Total Power Dissipation =  $450 \text{ mW typ/pkg}^*$   
 $* = V_{CC} = 15 \text{ V}$

### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC}$	18	Vdc
Continuous		18	
Pulsed, 1.0 s		20	
Input Voltage	$V_{in}$	-1.0 to +6.0	Vdc
MC666 MDTL		-4.0 to +4.0	
MRTL		-1.0 to +18	
All Others			
Output Current (into outputs)	—		mA <sub>dc</sub>
MC662		60	
MC663		28	
MC664		26	
MC669		30	
All Others except Power Drivers			
Input Reverse Current @ 18 V	$I_R$	0.5	mA <sub>dc</sub>
Forward Current (individual) MC669P	$I_F$	30	mA <sub>dc</sub>
Operating Temperature Range	$T_A$	-30 to +75	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-55 to +125	$^\circ\text{C}$