MC74HC4046A

Phase-Locked Loop

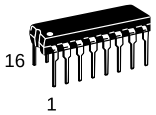
High–Performance Silicon–Gate CMOS

The MC574HC4046A is similar in function to the MC14046 Metal gate CMOS device. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

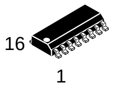
The HC4046A phase–locked loop contains three phase comparators, a voltage–controlled oscillator (VCO) and unity gain op–amp DEM$_{OUT}$. The comparators have two common signal inputs, COMP$_{IN}$, and SIG$_{IN}$. Input SIG$_{IN}$ and COMP$_{IN}$ can be used directly coupled to large voltage signals, or indirectly coupled (with a series capacitor to small voltage signals). The self–bias circuit adjusts small voltage signals in the linear region of the amplifier. Phase comparator 1 (an exclusive OR gate) provides a digital error signal PC1$_{OUT}$ and maintains 90 degrees phase shift at the center frequency between SIG$_{IN}$ and COMP$_{IN}$ signals (both at 50% duty cycle). Phase comparator 2 (with leading–edge sensing logic) provides digital error signals PC2$_{OUT}$ and PCP$_{OUT}$ and maintains a 0 degree phase shift between SIG$_{IN}$ and COMP$_{IN}$ signals (duty cycle is immaterial). The linear VCO produces an output signal VCO$_{OUT}$ whose frequency is determined by the voltage of input VCO$_{IN}$ signal and the capacitor and resistors connected to pins C1A, C1B, R1 and R2. The unity gain op–amp output DEM$_{OUT}$ with an external resistor is used where the VCO$_{IN}$ signal is needed but no loading can be tolerated. The inhibit input, when high, disables the VCO and all op–amps to minimize standby power consumption.

Applications include FM and FSK modulation and demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage–to–frequency conversion and motor speed control.

- Output Drive Capability: 10 LSTTL Loads
- Low Power Consumption Characteristic of CMOS Devices
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 3.0 to 6.0 V
- Low Input Current: 1.0 µA Maximum (except SIG$_{IN}$ and COMP$_{IN}$)
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Low Quiescent Current: 80 µA Maximum (VCO disabled)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on all Inputs
- Chip Complexity: 279 FETs or 70 Equivalent Gates



N SUFFIX
PLASTIC PACKAGE
CASE 648–08



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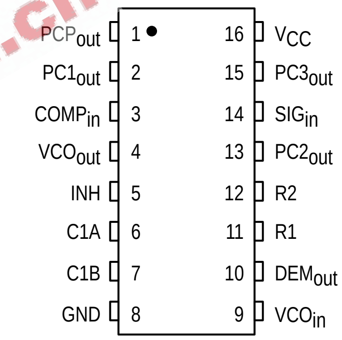
SOIC PACKAGE
CASE 751B–05

ORDERING INFORMATION

MC74HCXXXXAN	Plastic
MC74HCXXXXAD	SOIC

PIN ASSIGNMENT



Pin No.	Symbol	Name and Function
1	PCP$_{OUT}$	Phase Comparator Pulse Output
2	PC1$_{OUT}$	Phase Comparator 1 Output
3	COMP$_{IN}$	Comparator Input
4	VCO$_{OUT}$	VCO Output
5	INH	Inhibit Input
6	C1A	Capacitor C1 Connection A
7	C1B	Capacitor C1 Connection B
8	GND	Ground (0 V) V$_{SS}$
9	VCO$_{IN}$	VCO Input
10	DEM$_{OUT}$	Demodulator Output
11	R1	Resistor R1 Connection
12	R2	Resistor R2 Connection
13	PC2$_{OUT}$	Phase Comparator 2 Output
14	SIG$_{IN}$	Signal Input
15	PC3$_{OUT}$	Phase Comparator 3 Output
16	V$_{CC}$	Positive Supply Voltage

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 1.5 to V_{CC} + 1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air Plastic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP and SOIC Package†	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0	6.0	V
V_{CC}	DC Supply Voltage (Referenced to GND) NON–VCO	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Pin 5) V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

[Phase Comparator Section]

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} Volts	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage DC Coupled SIG_{IN}, $COMP_{IN}$	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \le 20\ \mu A$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage DC Coupled SIG_{IN}, $COMP_{IN}$	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \le 20\ \mu A$	2.0 4.5 6.0	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage PCP_{OUT}, PCn_{OUT}	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \le 20\ \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \le 4.0$ mA $\|I_{out}\| \le 5.2$ mA	4.5 6.0	3.98 5.48	3.84 5.34	3.7 5.2	

(continued)

[Phase Comparator Section]

DC ELECTRICAL CHARACTERISTICS – continued (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} Volts	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{OL}	Maximum Low–Level Output Voltage Qa–Qh PCP_{OUT}, PCn_{OUT}	V_{out} = 0.1 V or V_{CC} – 0.1 V $\lvert I_{out} \rvert \le 20\ \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL}					
		$\lvert I_{out} \rvert \le 4.0$ mA	4.5	0.26	0.33	0.4	
		$\lvert I_{out} \rvert \le 5.2$ mA	6.0	0.26	0.33	0.4	
I_{in}	Maximum Input Leakage Current SIG_{IN}, $COMP_{IN}$	$V_{in} = V_{CC}$ or GND	2.0 3.0 4.5 6.0	± 3.0 ± 7.0 ± 18.0 ± 30.0	± 4.0 ± 9.0 ± 23.0 ± 38.0	± 5.0 ± 11.0 ± 27.0 ± 45.0	µA
I_{OZ}	Maximum Three–State Leakage Current $PC2_{OUT}$	Output in High–Impedance State $V_{in} = V_{IH}$ or V_{IL} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10	µA
I_{CC}	Maximum Quiescent Supply Current (per Package) (VCO disabled) Pins 3, 5 and 14 at V_{CC} Pin 9 at GND; Input Leakage at Pins 3 and 14 to be excluded	$V_{in} = V_{CC}$ or GND $\lvert I_{out} \rvert = 0\ \mu A$	6.0	4.0	40	160	µA

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

[Phase Comparator Section]

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} Volts	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, SIG_{IN}/$COMP_{IN}$ to $PC1_{OUT}$ (Figure 1)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, SIG_{IN}/$COMP_{IN}$ to PCP_{OUT} (Figure 1)	2.0 4.5 6.0	340 68 58	425 85 72	510 102 87	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, SIG_{IN}/$COMP_{IN}$ to $PC3_{OUT}$ (Figure 1)	2.0 4.5 6.0	270 54 46	340 68 58	405 81 69	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, SIG_{IN}/$COMP_{IN}$ Output Disable Time to $PC2_{OUT}$ (Figures 2 and 3)	2.0 4.5 6.0	200 40 34	250 50 43	300 60 51	ns
t_{PZH}, t_{PZL}	Maximum Propagation Delay, SIG_{IN}/$COMP_{IN}$ Output Enable Time to $PC2_{OUT}$ (Figures 2 and 3)	2.0 4.5 6.0	230 46 39	290 58 49	345 69 59	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time (Figure 1)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns

[VCO Section]

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} Volts	Guaranteed Limit						Unit
				– 55 to 25°C		≤ 85°C		≤ 125°C		
V_{IH}	Minimum High–Level Input Voltage INH	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \le 20\ \mu A$	3.0 4.5 6.0	2.1 3.15 4.2		2.1 3.15 4.2		2.1 3.15 4.2		V
V_{IL}	Maximum Low–Level Input Voltage INH	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \le 20\ \mu A$	3.0 4.5 6.0	0.90 1.35 1.8		0.9 1.35 1.8		0.9 1.35 1.8		V
V_{OH}	Minimum High–Level Output Voltage VCO_{OUT}	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20\ \mu A$	3.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		1.9 4.4 5.9		V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 4.0$ mA $\|I_{out}\| \le 5.2$ mA	4.5 6.0	3.98 5.48		3.84 5.34		3.7 5.2		
V_{OL}	Maximum Low–Level Output Voltage VCO_{OUT}	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \le 20\ \mu A$	3.0 4.5 6.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1		V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 4.0$ mA $\|I_{out}\| \le 5.2$ mA	4.5 6.0	0.26 0.26		0.33 0.33		0.4 0.4		
I_{in}	Maximum Input Leakage Current INH, VCO_{IN}	V_{in} = V_{CC} or GND	6.0	0.1		1.0		1.0		µA
				Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$V_{VCO_{IN}}$	Operating Voltage Range at VCO_{IN} over the range specified for R1; For linearity see Fig. 15A, Parallel value of R1 and R2 should be > 2.7 kΩ	INH = V_{IL}	3.0 4.5 6.0	0.1 0.1 0.1	1.0 2.5 4.0	0.1 0.1 0.1	1.0 2.5 4.0	0.1 0.1 0.1	1.0 2.5 4.0	V
R1	Resistor Range		3.0 4.5 6.0	3.0 3.0 3.0	300 300 300	3.0 3.0 3.0	300 300 300	3.0 3.0 3.0	300 300 300	kΩ
R2			3.0 4.5 6.0	3.0 3.0 3.0	300 300 300	3.0 3.0 3.0	300 300 300	3.0 3.0 3.0	300 300 300	
C1	Capacitor Range		3.0 4.5 6.0	40 40 40	No Limit					pF

[VCO Section]

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6.0 ns)

Symbol	Parameter	V_{CC} Volts	Guaranteed Limit						Unit
			– 55 to 25°C		≤ 85°C		≤ 125°C		
			Min	Max	Min	Max	Min	Max	
Δf/T	Frequency Stability with Temperature Changes (Figure 13A, B, C)	3.0 4.5 6.0							%/K
fo	VCO Center Frequency (Duty Factor = 50%) (Figure 14A, B, C, D)	3.0 4.5 6.0	3 11 13						MHz
ΔfVCO	VCO Frequency Linearity	3.0 4.5 6.0	See Figures 15A, B, C						%
∂ VCO	Duty Factor at VCO$_{OUT}$	3.0 4.5 6.0	Typical 50%						%

[Demodulator Section]

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} Volts	Guaranteed Limit						Unit
				– 55 to 25°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
RS	Resistor Range	At RS > 300 kΩ the Leakage Current can Influence VDEM$_{OUT}$	3.0 4.5 6.0	50 50 50	300 300 300					kΩ
V_{OFF}	Offset Voltage VCO$_{IN}$ to VDEM$_{OUT}$	Vi = VVCO$_{IN}$ = 1/2 V_{CC}; Values taken over RS Range.	3.0 4.5 6.0	See Figure 12						mV
RD	Dynamic Output Resistance at DEM$_{OUT}$	VDEM$_{OUT}$ = 1/2 V_{CC}	3.0 4.5 6.0	Typical 25 Ω						Ω

SWITCHING WAVEFORMS

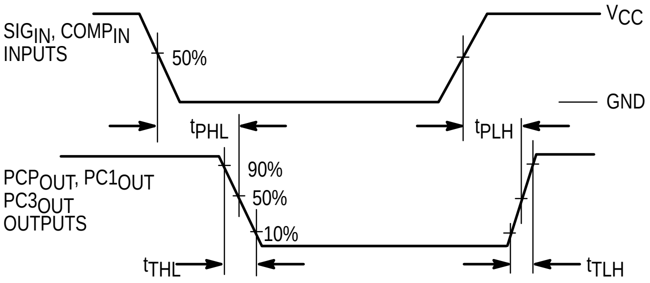


Figure 1.

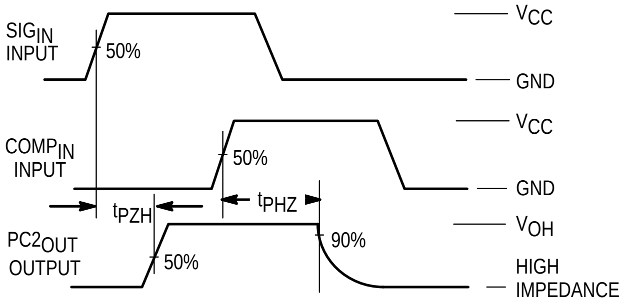


Figure 2.

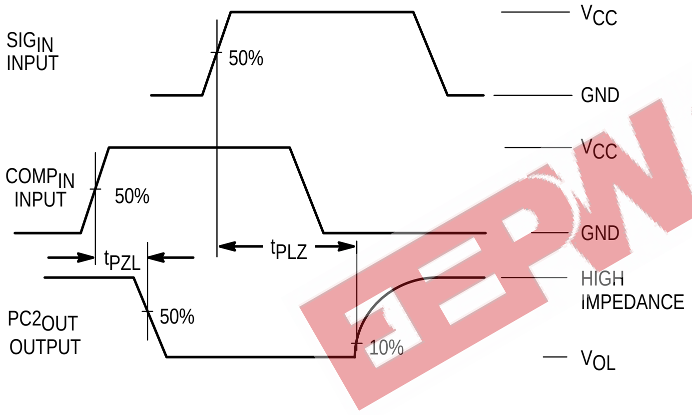
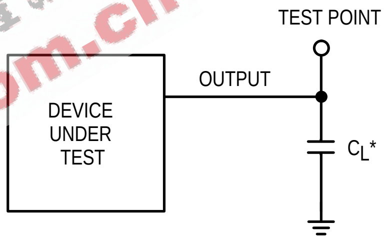


Figure 3.



*INCLUDES ALL PROBE AND JIG CAPACITANCE

Figure 4. Test Circuit

DETAILED CIRCUIT DESCRIPTION

Voltage Controlled Oscillator/Demodulator Output

The VCO requires two or three external components to operate. These are R1, R2, C1. Resistor R1 and Capacitor C1 are selected to determine the center frequency of the VCO (see typical performance curves Figure 14). R2 can be used to set the offset frequency with 0 volts at VCO input. For example, if R2 is decreased, the offset frequency is increased. If R2 is omitted the VCO range is from 0 Hz. The effect of R2 is shown in Figure 24, typical performance curves. By increasing the value of R2 the lock range of the PLL is increased and the gain (volts/Hz) is decreased. Thus, for a narrow lock range, large swings on the VCO input will cause less frequency variation.

Internally, the resistors set a current in a current mirror, as shown in Figure 5. The mirrored current drives one side of the capacitor. Once the voltage across the capacitor charges up to V_{ref} of the comparators, the oscillator logic flips the capacitor which causes the mirror to charge the opposite side of the capacitor. The output from the internal logic is then taken to VCO output (Pin 4).

The input to the VCO is a very high impedance CMOS input and thus will not load down the loop filter, easing the filters design. In order to make signals at the VCO input accessible without degrading the loop performance, the VCO input voltage is buffered through a unity gain Op–amp to Demod Output. This Op–amp can drive loads of 50K ohms or more and provides no loading effects to the VCO input voltage (see Figure 12).

An inhibit input is provided to allow disabling of the VCO and all Op–amps (see Figure 5). This is useful if the internal VCO is not being used. A logic high on inhibit disables the VCO and all Op–amps, minimizing standby power consumption.

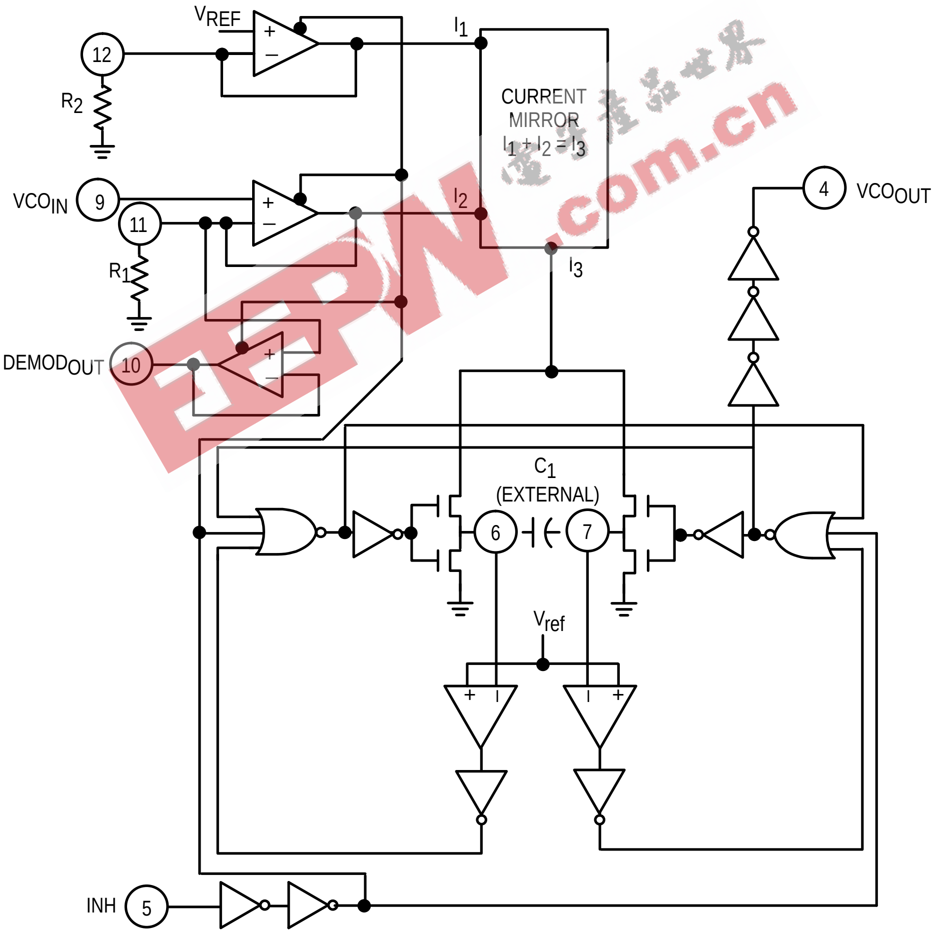


Figure 5. Logic Diagram for VCO

The output of the VCO is a standard high speed CMOS output with an equivalent LS–TTL fan out of 10. The VCO output is approximately a square wave. This output can either directly feed the $COMP_{IN}$ of the phase comparators or feed external prescalers (counters) to enable frequency synthesis.

Phase Comparators

All three phase comparators have two inputs, SIG_{IN} and $COMP_{IN}$. The SIG_{IN} and $COMP_{IN}$ have a special DC bias network that enables AC coupling of input signals. If the signals are not AC coupled, standard 54HC/74HC input levels are required. Both input structures are shown in Figure 6. The outputs of these comparators are essentially standard 54HC/74HC outputs (comparator 2 is TRI–STATEABLE). In normal operation V_{CC} and ground voltage levels are fed to the loop filter. This differs from some phase detectors which supply a current to the loop filter and should be considered in the design. (The MC14046 also provides a voltage).

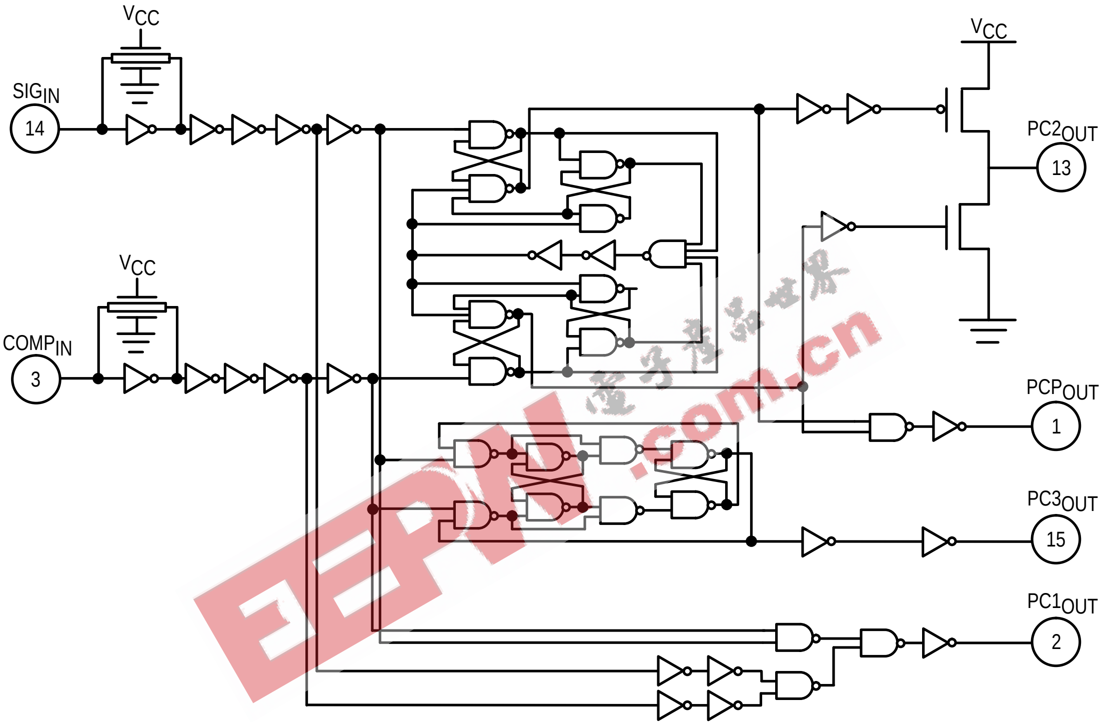


Figure 6. Logic Diagram for Phase Comparators

Phase Comparator 1

This comparator is a simple XOR gate similar to the 54/74HC86. Its operation is similar to an overdriven balanced modulator. To maximize lock range the input frequencies must have a 50% duty cycle. Typical input and output waveforms are shown in Figure 7. The output of the phase detector feeds the loop filter which averages the output voltage. The frequency range upon which the PLL will lock onto if initially out of lock is defined as the capture range. The capture range for phase detector 1 is dependent on the loop filter design. The capture range can be as large as the lock range, which is equal to the VCO frequency range.

To see how the detector operates, refer to Figure 7. When two square wave signals are applied to this comparator, an output waveform (whose duty cycle is dependent on the phase difference between the two signals) results. As the phase difference increases, the output duty cycle increases and the voltage after the loop filter increases. In order to achieve lock when the PLL input frequency increases, the VCO input voltage must increase and the phase difference between $COMP_{IN}$ and SIG_{IN} will increase. At an input frequency equal to f_{min}, the VCO input is at 0 V. This requires the phase detector output to be grounded; hence, the two input signals must be in phase. When the input frequency is f_{max}, the VCO input must be V_{CC} and the phase detector inputs must be 180 degrees out of phase.

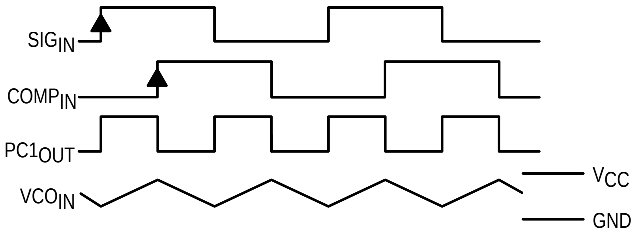


Figure 7. Typical Waveforms for PLL Using Phase Comparator 1

The XOR is more susceptible to locking onto harmonics of the SIG$_{IN}$ than the digital phase detector 2. For instance, a signal 2 times the VCO frequency results in the same output duty cycle as a signal equal to the VCO frequency. The difference is that the output frequency of the 2f example is twice that of the other example. The loop filter and VCO range should be designed to prevent locking on to harmonics.

Phase Comparator 2

This detector is a digital memory network. It consists of four flip–flops and some gating logic, a three state output and a phase pulse output as shown in Figure 6. This comparator acts only on the positive edges of the input signals and is independent of duty cycle.

Phase comparator 2 operates in such a way as to force the PLL into lock with 0 phase difference between the VCO output and the signal input positive waveform edges. Figure 8 shows some typical loop waveforms. First assume that SIG$_{IN}$ is leading the COMP$_{IN}$. This means that the VCO's frequency must be increased to bring its leading edge into proper phase alignment. Thus the phase detector 2 output is set high. This will cause the loop filter to charge up the VCO input, increasing the VCO frequency. Once the leading edge of the COMP$_{IN}$ is detected, the output goes TRI–STATE holding the VCO input at the loop filter voltage. If the VCO still lags the SIG$_{IN}$ then the phase detector will again charge up the VCO input for the time between the leading edges of both waveforms.

If the VCO leads the SIG$_{IN}$ then when the leading edge of the VCO is seen; the output of the phase comparator goes low. This discharges the loop filter until the leading edge of the SIG$_{IN}$ is detected at which time the output disables itself again. This has the effect of slowing down the VCO to again make the rising edges of both waveforms coincidental.

When the PLL is out of lock, the VCO will be running either slower or faster than the SIG$_{IN}$. If it is running slower the phase detector will see more SIG$_{IN}$ rising edges and so the output of the phase comparator will be high a majority of the time, raising the VCO's frequency. Conversely, if the VCO is running faster than the SIG$_{IN}$, the output of the detector will be low most of the time and the VCO's output frequency will be decreased.

As one can see, when the PLL is locked, the output of phase comparator 2 will be disabled except for minor corrections at the leading edge of the waveforms. When PC$_2$ is TRI–STATED, the PCP output is high. This output can be used to determine when the PLL is in the locked condition.

This detector has several interesting characteristics. Over the entire VCO frequency range there is no phase difference between the COMP$_{IN}$ and the SIG$_{IN}$. The lock range of the PLL is the same as the capture range. Minimal power was consumed in the loop filter since in lock the detector output is a high impedance. When no SIG$_{IN}$ is present, the detector will see only VCO leading edges, so the comparator output will stay low, forcing the VCO to f$_{min}$.

Phase comparator 2 is more susceptible to noise, causing the PLL to unlock. If a noise pulse is seen on the SIG$_{IN}$, the comparator treats it as another positive edge of the SIG$_{IN}$ and will cause the output to go high until the VCO leading edge is seen, potentially for an entire SIG$_{IN}$ period. This would cause the VCO to speed up during that time. When using PC$_1$, the output of that phase detector would be disturbed for only the short duration of the noise spike and would cause less upset.

Phase Comparator 3

This is a positive edge–triggered sequential phase detector using an RS flip–flop as shown in Figure 6. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG$_{IN}$ and COMP$_{IN}$ are not important. It has some similar characteristics to the edge sensitive comparator. To see how this detector works, assume input pulses are applied to the SIG$_{IN}$ and COMP$_{IN}$'s as shown in Figure 9. When the SIG$_{IN}$ leads the COMP$_{IN}$, the flop is set. This will charge the loop filter and cause the VCO to speed up, bringing the comparator into phase with the SIG$_{IN}$. The phase angle between SIG$_{IN}$ and COMP$_{IN}$ varies from 0° to 360° and is 180° at f$_0$. The voltage swing for PC$_3$ is greater than for PC$_2$ but consequently has more ripple in the signal to the VCO. When no SIG$_{IN}$ is present the VCO will be forced to f$_{max}$ as opposed to f$_{min}$ when PC$_2$ is used.

The operating characteristics of all three phase comparators should be compared to the requirements of the system design and the appropriate one should be used.

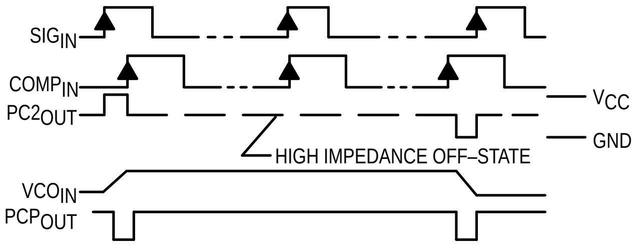


Figure 8. Typical Waveforms for PLL Using Phase Comparator 2

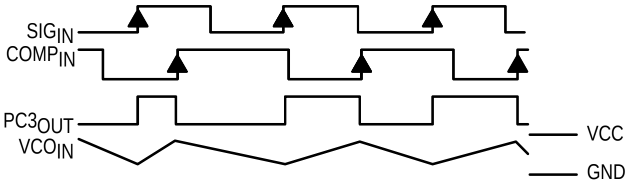


Figure 9. Typical Waveform for PLL Using Phase Comparator 3

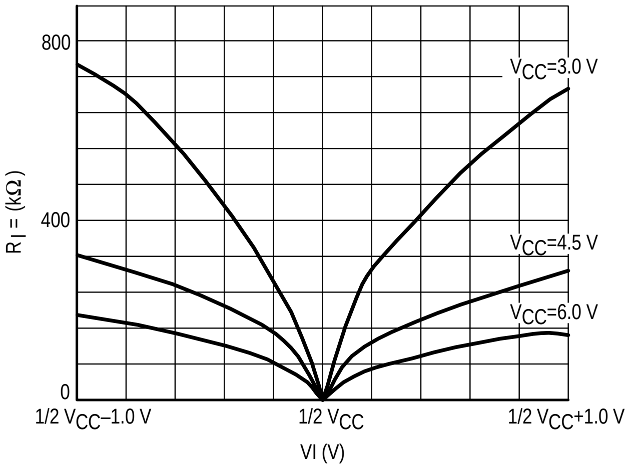


Figure 10. Input Resistance at SIG_{IN}, $COMP_{IN}$ with ΔV_I = 1.0 V at Self–Bias Point

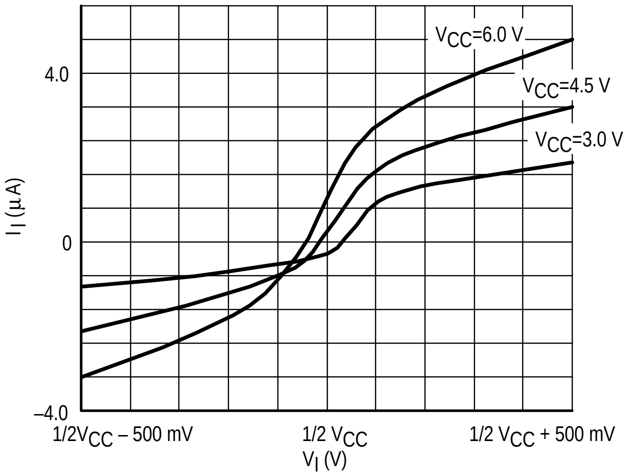


Figure 11. Input Current at SIG_{IN}, $COMP_{IN}$ with ΔV_I = 500 mV at Self–Bias Point

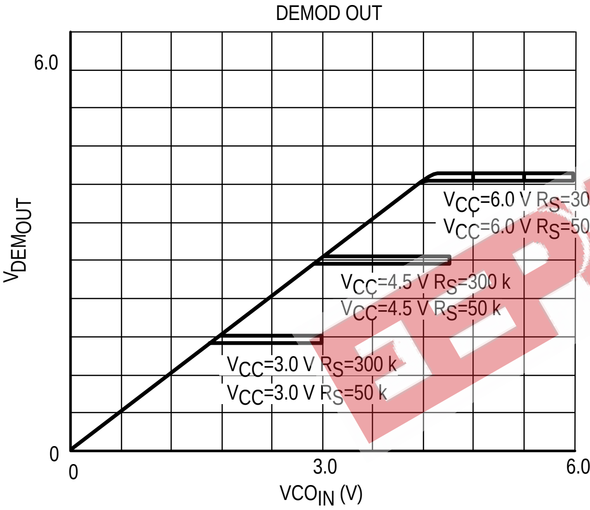


Figure 12. Offset Voltage at Demodulator Output as a Function of VCO_{IN} and R_S

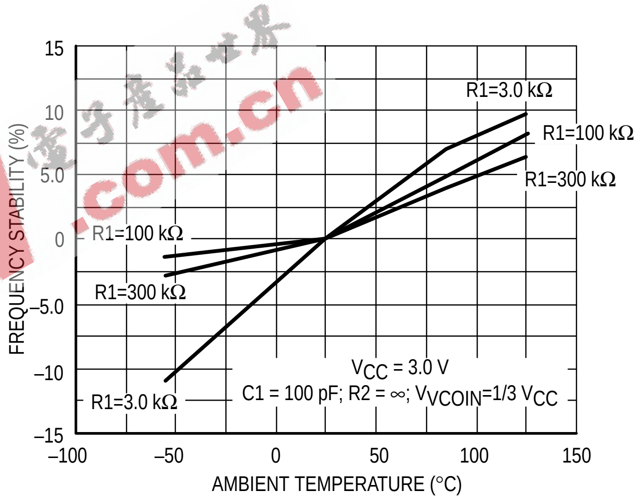


Figure 13A. Frequency Stability versus Ambient Temperature: V_{CC} = 3.0 V

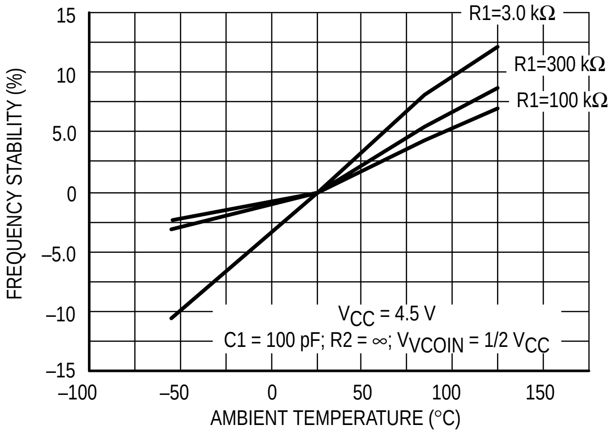


Figure 13B. Frequency Stability versus Ambient Temperature: V_{CC} = 4.5 V

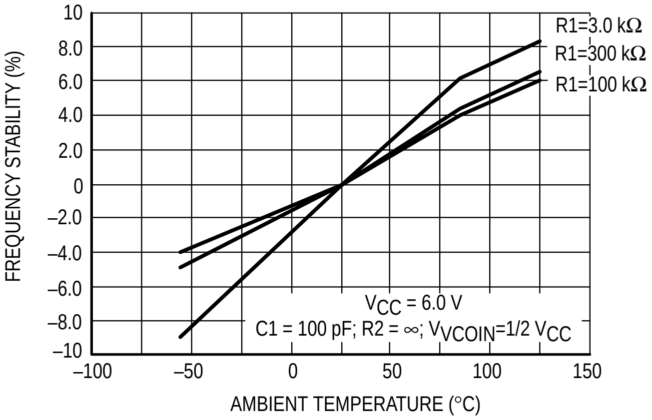


Figure 13C. Frequency Stability versus Ambient Temperature: V_{CC} = 6.0 V

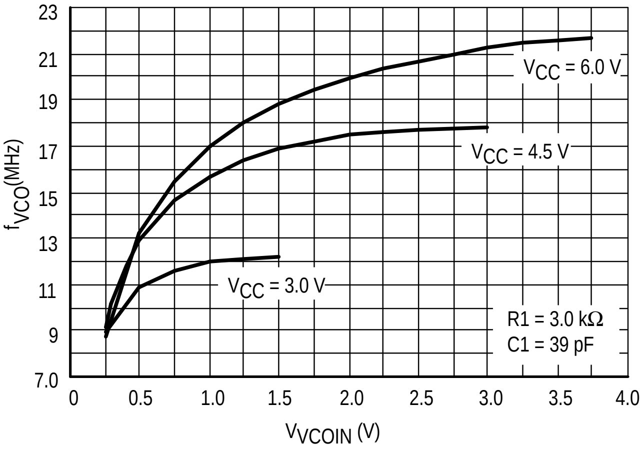


Figure 14A. VCO Frequency (f_{VCO}) as a Function of the VCO Input Voltage (V_{VCOIN})

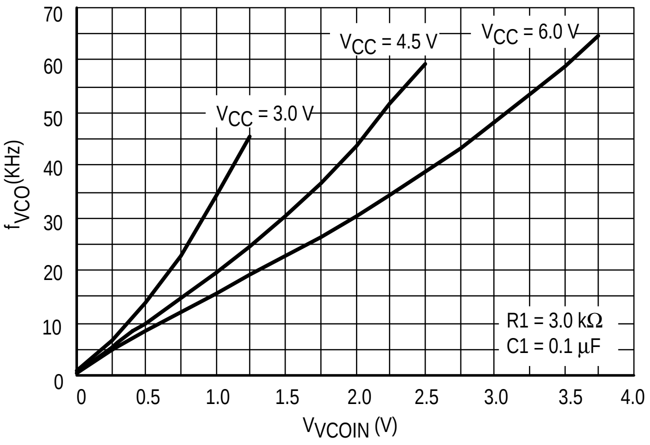


Figure 14B. VCO Frequency (f_{VCO}) as a Function of the VCO Input Voltage (V_{VCOIN})

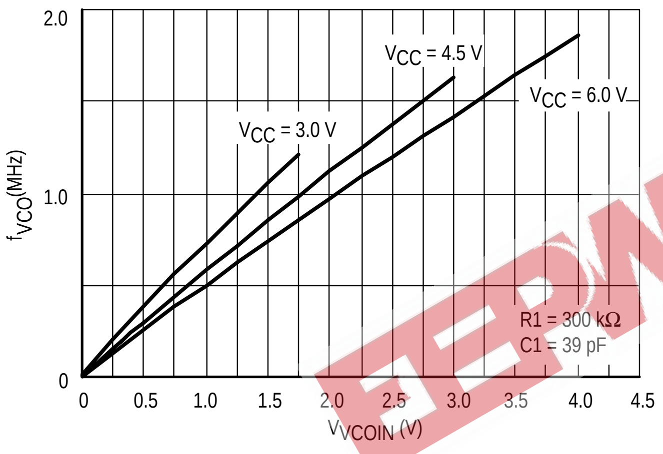


Figure 14C. VCO Frequency (f_{VCO}) as a Function of the VCO Input Voltage (V_{VCOIN})

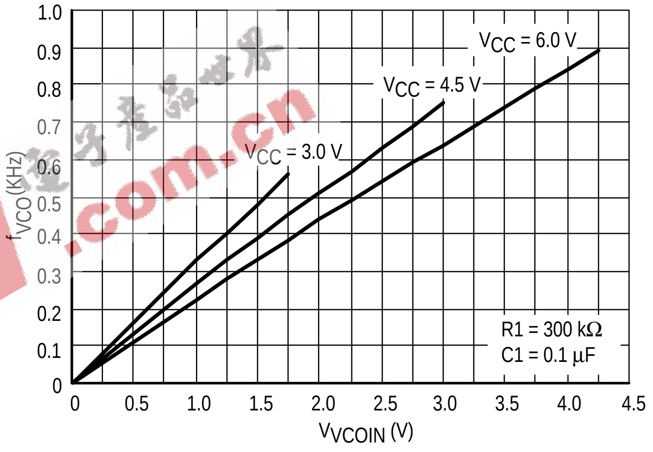


Figure 14D. VCO Frequency (f_{VCO}) as a Function of the VCO Input Voltage (V_{VCOIN})

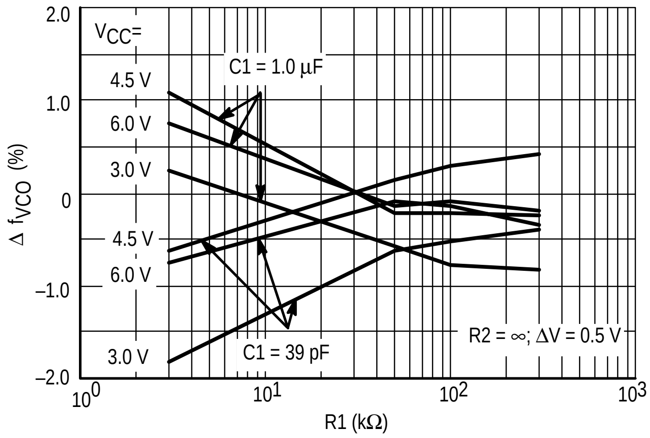
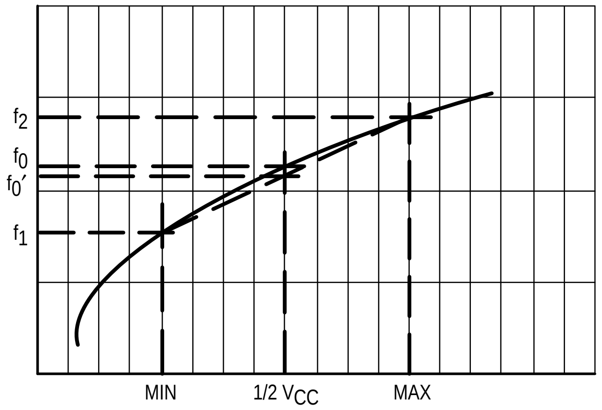


Figure 15A. Frequency Linearity versus R1, C1 and V_{CC}



ΔV = 0.5 V OVER THE V_{CC} RANGE:
FOR VCO LINEARITY

$f_0' = (f_1 + f_2) / 2$

LINEARITY = $(f_0' - f_0) / f_0'$ x 100%

Figure 15B. Definition of VCO Frequency Linearity

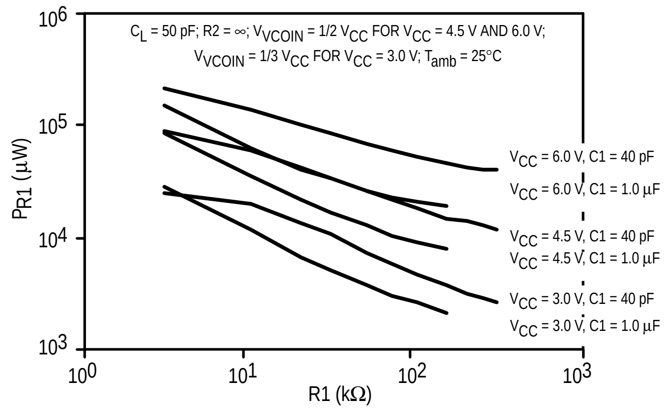


Figure 16. Power Dissipation versus R1

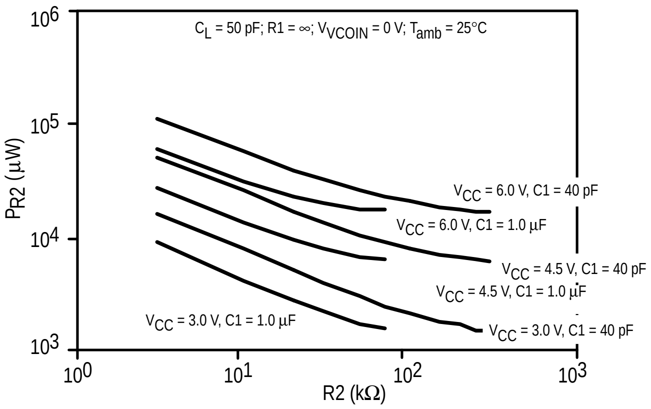


Figure 17. Power Dissipation versus R2

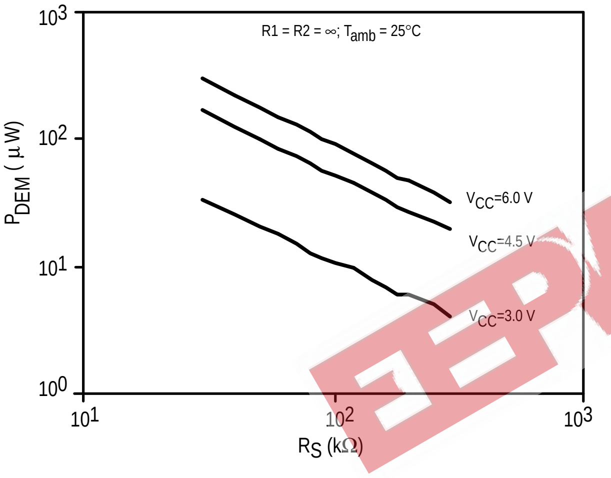


Figure 18. DC Power Dissipation of Demodulator versus R_S

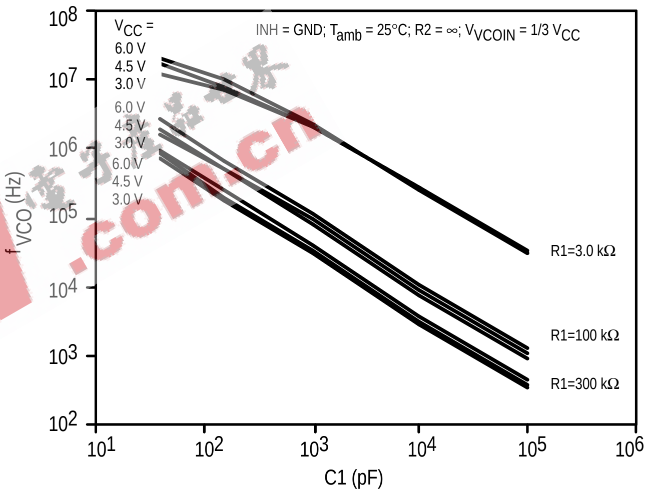


Figure 19. VCO Center Frequency versus C1

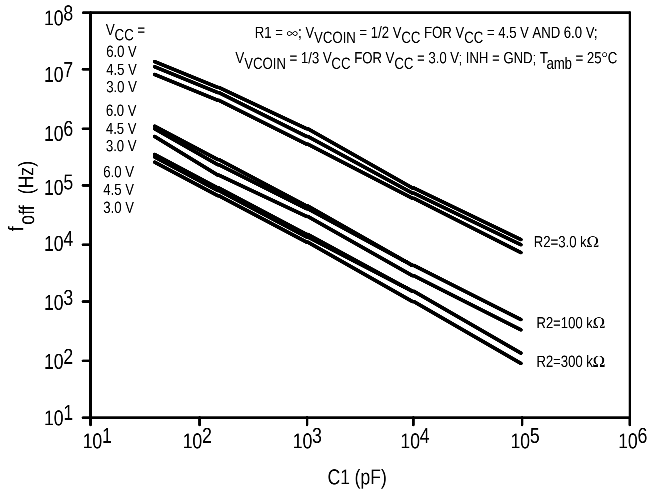


Figure 20. Frequency Offset versus C1

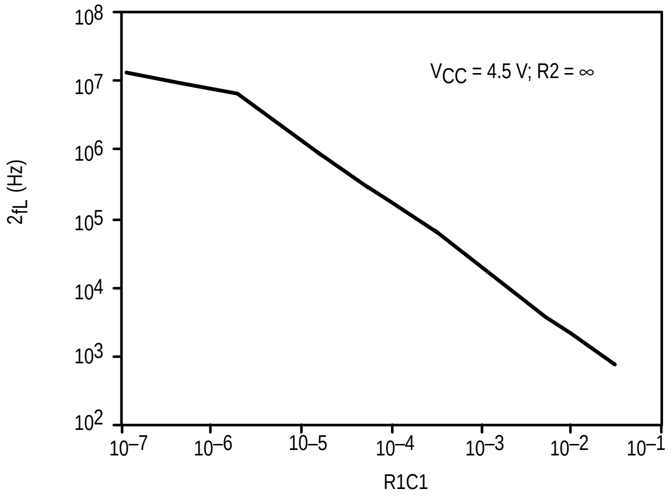


Figure 21. Typical Frequency Lock Range ($2f_L$) versus R_1C_1

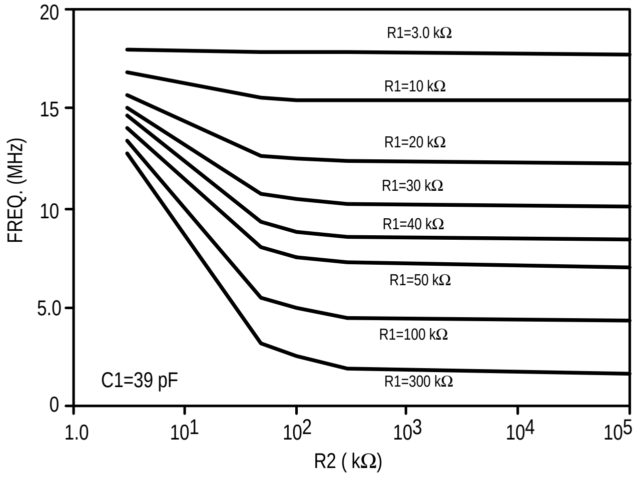


Figure 22. R2 versus f_{max}

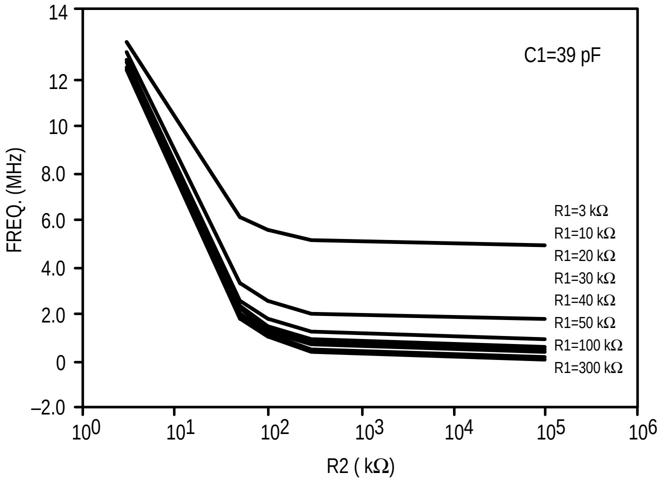


Figure 23. R2 versus f_{min}

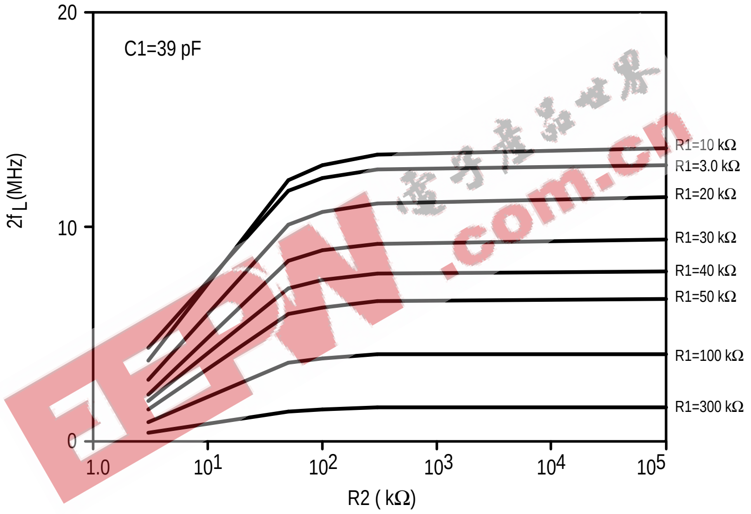


Figure 24. R2 versus Frequency Lock Range ($2f_L$)

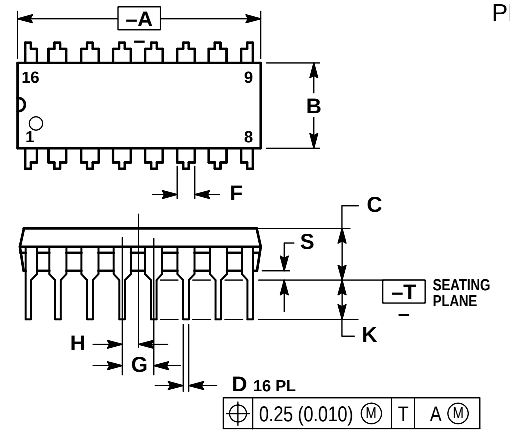
APPLICATION INFORMATION

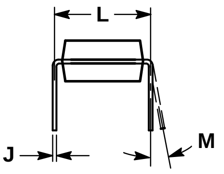
The following information is a guide for approximate values of R1, R2, and C1. Figures 19, 20, and 21 should be used as references as indicated below, also the values of R1, R2, and C1 should not violate the Maximum values indicated in the DC ELECTRICAL CHARACTERISTICS tables.

Phase Comparator 1		**Phase Comparator 2**		**Phase Comparator 3**	
$R_2 = \infty$	**$R_2 \neq \infty$**	**$R_2 = \infty$**	**$R_2 \neq \infty$**	**$R_2 = \infty$**	**$R_2 \neq \infty$**
• Given f0 • Use f0 with Figure 19 to determine R1 and C1. (see Figure 23 for characteristics of the VCO operation)	• Given f0 and fL • Calculate f_{min} f_{min} = f0–fL • Determine values of C1 and R2 from Figure 20. • Determine R1–C1 from Figure 21. • Calculate value of R1 from the value of C1 and the product of R1C1 from Figure 21. (see Figure 24 for characteristics of the VCO operation)	• Given f_{max} and f0 • Determine the value of R1 and C1 using Figure 19 and use Figure 21 to obtain 2fL and then use this to calculate f_{min}.	• Given f0 and fL • Calculate f_{min} f_{min} = f0–fL • Determine values of C1 and R2 from Figure 20. • Determine R1–C1 from Figure 21. • Calculate value of R1 from the value of C1 and the product of R1C1 from Figure 21. (see Figure 24 for characteristics of the VCO operation)	• Given f_{max} and f0 • Determine the value of R1 and C1 using Figure 19 and Figure 21 to obtain 2fL and then use this to calculate f_{min}.	• Given f0 and fL • Calculate f_{min}: f_{min} = f0–fL • Determine values of C1 and R2 from Figure 20. • Determine R1–C1 from Figure 21. • Calculate value of R1 from the value of C1 and the product of R1C1 from Figure 21. (see Figure 24 for characteristics of the VCO operation)

OUTLINE DIMENSIONS

N SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R

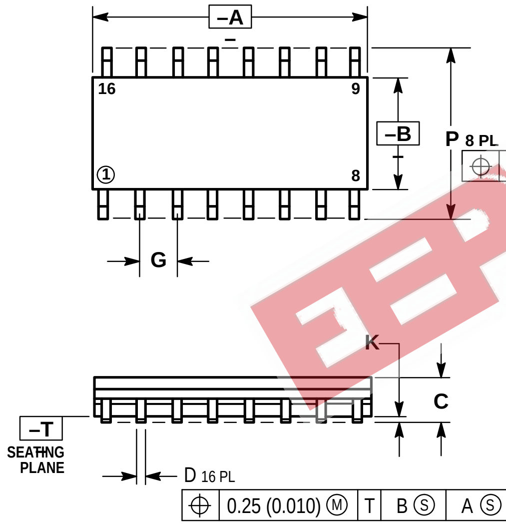


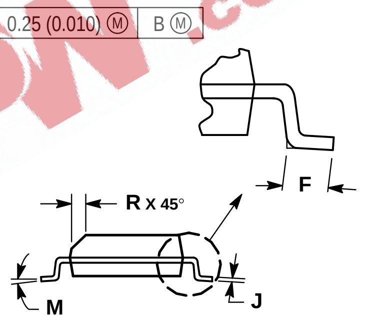


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J





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NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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