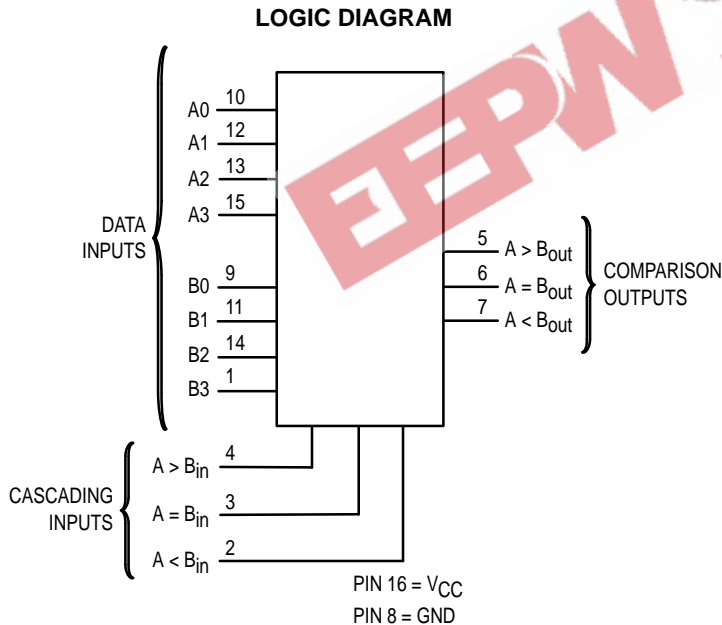


4-Bit Magnitude Comparator High-Performance Silicon-Gate CMOS

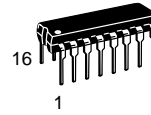
The MC74HC85 is identical in pinout and function to the LS85. This device is similar in function to the MM74C85 and L85, but has a different pinout. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This 4-Bit Magnitude Comparator compares two 4-bit nibbles and gives a high voltage level on either the $A > B_{out}$, $A = B_{out}$, or $A < B_{out}$ output, leaving the other two at a low voltage level. This device also has $A > B_{in}$, $A = B_{in}$, and $A < B_{in}$ inputs, eliminating the need for external gates when cascading.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 248 FETs or 62 Equivalent Gates



MC74HC85



N SUFFIX
PLASTIC PACKAGE
CASE 648-08



DT SUFFIX
TSSOP PACKAGE
CASE 948F-01

ORDERING INFORMATION

MC74HCXXN	Plastic
MC74HCXXDT	TSSOP

PIN ASSIGNMENT

B3	1	16	V_{CC}
$A < B_{in}$	2	15	A3
$A = B_{in}$	3	14	B2
$A > B_{in}$	4	13	A2
$A > B_{out}$	5	12	A1
$A = B_{out}$	6	11	B1
$A < B_{out}$	7	10	A0
GND	8	9	B0



MC74HC85

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	- 1.5 to V _{CC} + 1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Current, per Pin	± 25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 50	mA
P _D	Power Dissipation in Still Air Plastic DIP† TSSOP Package†	750 450	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or TSSOP)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C

TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	- 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				- 55 to 25 °C	≤ 85 °C	≤ 125 °C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	2.0	± 0.1	± 1.0	± 1.0	μA
			4.5				
			6.0				
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	2.0	8	80	160	μA
			4.5				
			6.0				

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Inputs A or B to Outputs A > B or A < B (Figures 1 and 2)	2.0	230	290	345	ns
		4.5	46	58	69	
		6.0	39	49	59	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Inputs A or B to Output A = B (Figures 1 and 2)	2.0	200	250	300	ns
		4.5	40	50	60	
		6.0	34	43	51	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Inputs A < B or A = B to Output A > B (Figures 1 and 2)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Inputs A > B or A = B to Output A < B (Figures 1 and 2)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A = B to Output A = B (Figures 1 and 2)	2.0	145	180	220	ns
		4.5	29	36	44	
		6.0	25	31	38	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).
- Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

C _{PD}	Power Dissipation Capacitance (Per Package)*	Typical @ 25°C, V _{CC} = 5.0 V	pF
		50	

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

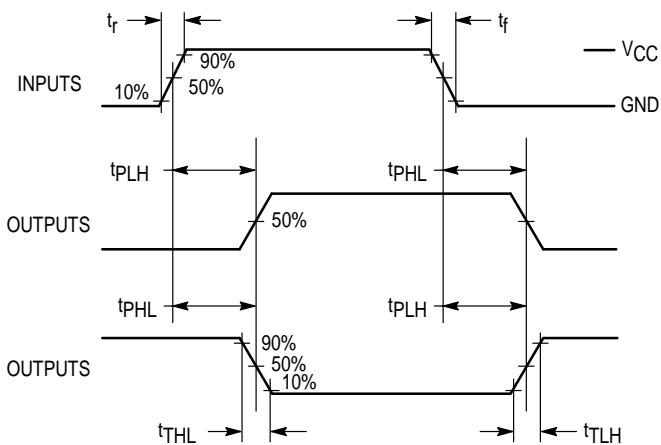
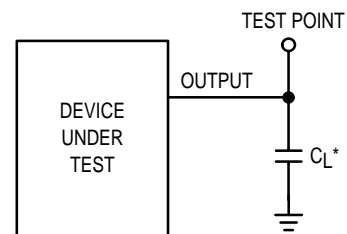


Figure 1. Switching Waveforms



* Includes all probe and jig capacitance

Figure 2. Test Circuit

PIN DESCRIPTIONS

INPUTS

A0, A1, A2, A3 (Pins 10, 12, 13, 15)

Data Nibble A Inputs. The data nibble present at these inputs is compared to Data Nibble B. A3 is the most significant bit and A0 is the least significant bit.

B0, B1, B2, B3 (Pins 9, 11, 14, 1)

Data Nibble B Inputs. The data nibble present at these inputs is compared to Data Nibble A. B3 is the most significant bit and B0 is the least significant bit.

CONTROLS

A > B_{in}, A = B_{in}, A < B_{in} (Pins 4, 3, 2)

Cascading Inputs. These inputs determine the states of the outputs only when Data Nibble A equals Data Nibble B. The A = B_{in} input overrides both the A > B_{in} and A < B_{in} inputs.

For single stage operation or for the least significant stage in cascaded operation, the A < B_{in} and A > B_{in} inputs should be tied to ground and the A = B_{in} input tied to V_{CC}. Between cascaded comparators, the A < B_{out}, A = B_{out}, and A > B_{out}

outputs should be tied to A < B_{in}, A = B_{in}, and A > B_{in}, respectively, of the succeeding stage.

OUTPUTS

A > B_{out} (Pin 5)

A–Greater–Than–B Output. This output is at a high voltage level when Nibble A is greater than Nibble B, regardless of the data present at the cascading inputs. This output is also high when Nibble A equals Nibble B and the A > B_{in} input is high (A < B_{in} and A = B_{in} are at a low voltage level).

A = B_{out} (Pin 6)

A–Equals–B Output. This output is high when Nibble A equals Nibble B and the A = B_{in} input is high. A < B_{in} and A > B_{in} have no effect when the comparator is in this condition and A = B_{in} is at a high voltage level.

A < B_{out} (Pin 7)

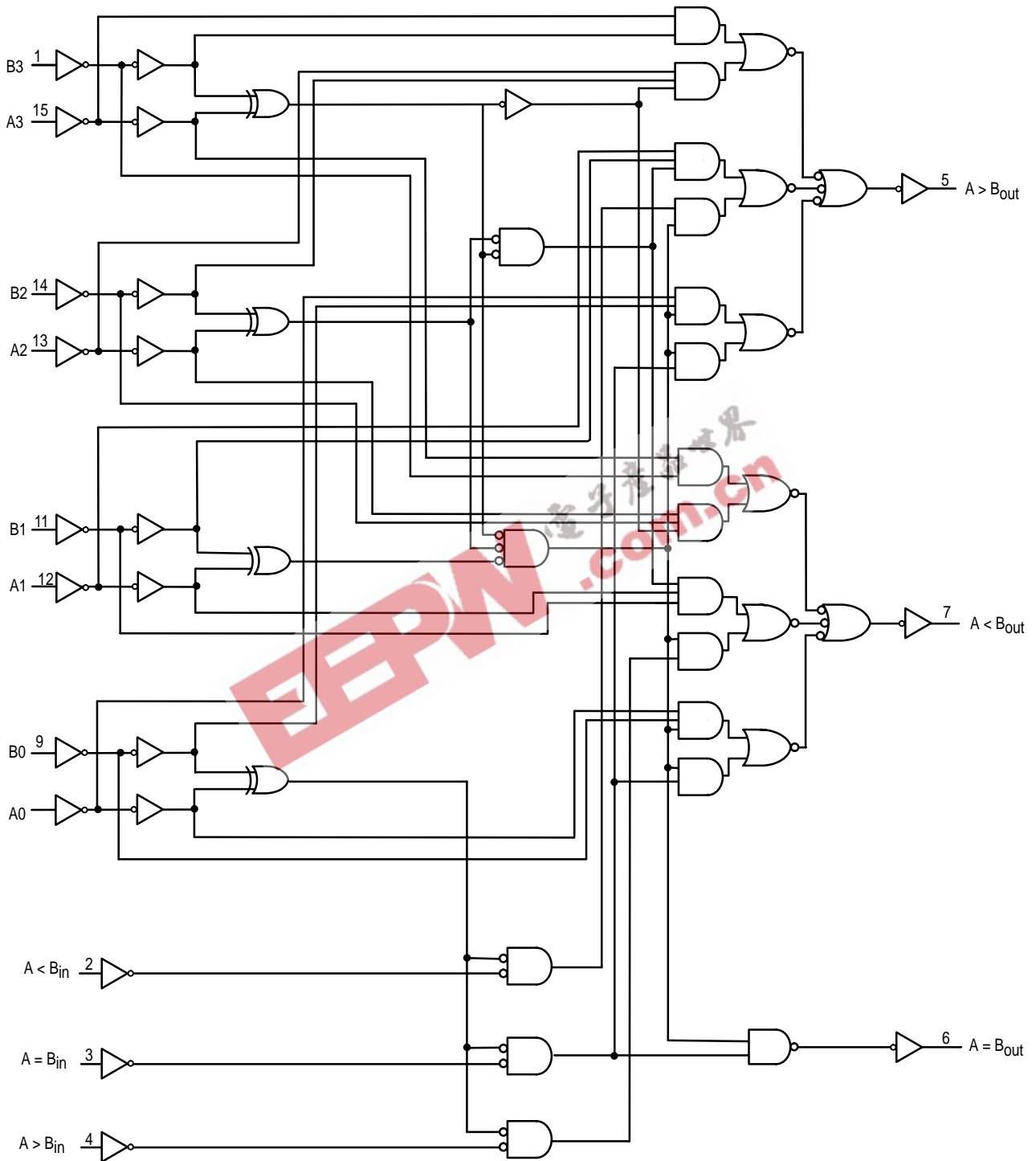
A–Less–Than–B Output. This output is at a high voltage level when Nibble A is less than Nibble B, regardless of data present at the cascading inputs. This output is also high when Nibble A equals Nibble B and the A < B_{in} input is high (A > B_{in} and A = B_{in} are at a low voltage level).

FUNCTION TABLE

Data Inputs				Cascading Inputs			Output		
A3, B3	A2, B2	A1, B1	A0, B0	A > B _{in}	A = B _{in}	A < B _{in}	A > B _{out}	A = B _{out}	A < B _{out}
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	L	H
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	L	H
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	H	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	H	X	L	H	L

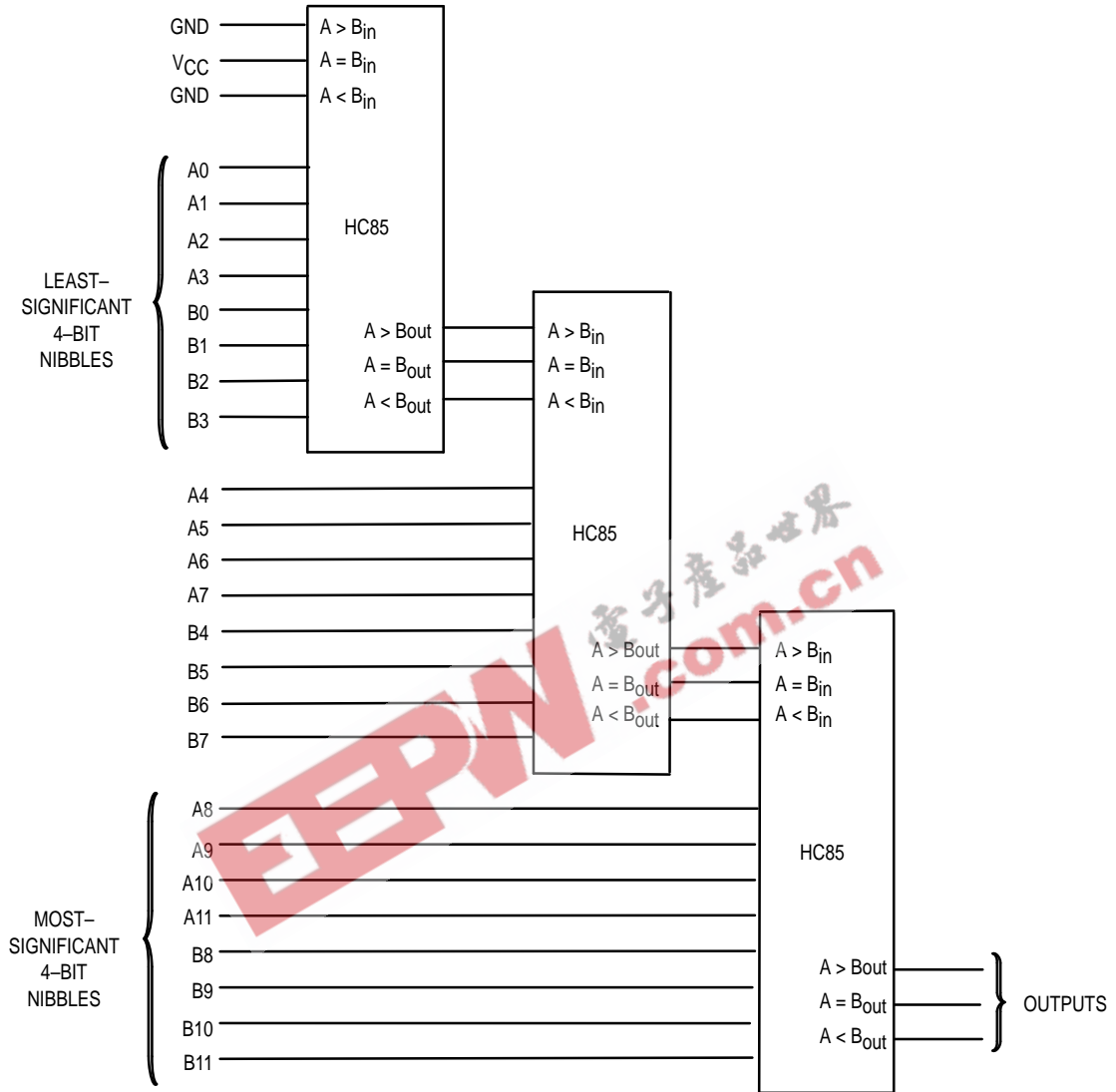
X = Don't Care

EXPANDED LOGIC PROGRAM



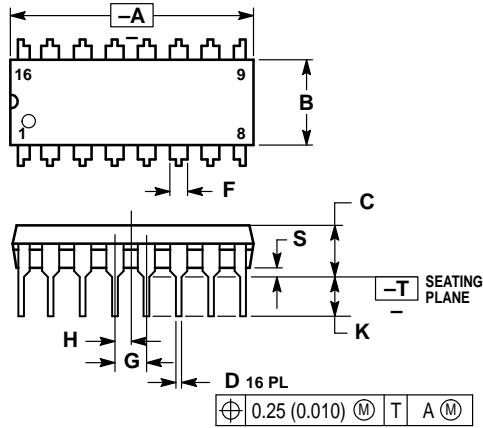
MC74HC85

TYPICAL APPLICATION
CASCADING COMPARATORS



OUTLINE DIMENSIONS

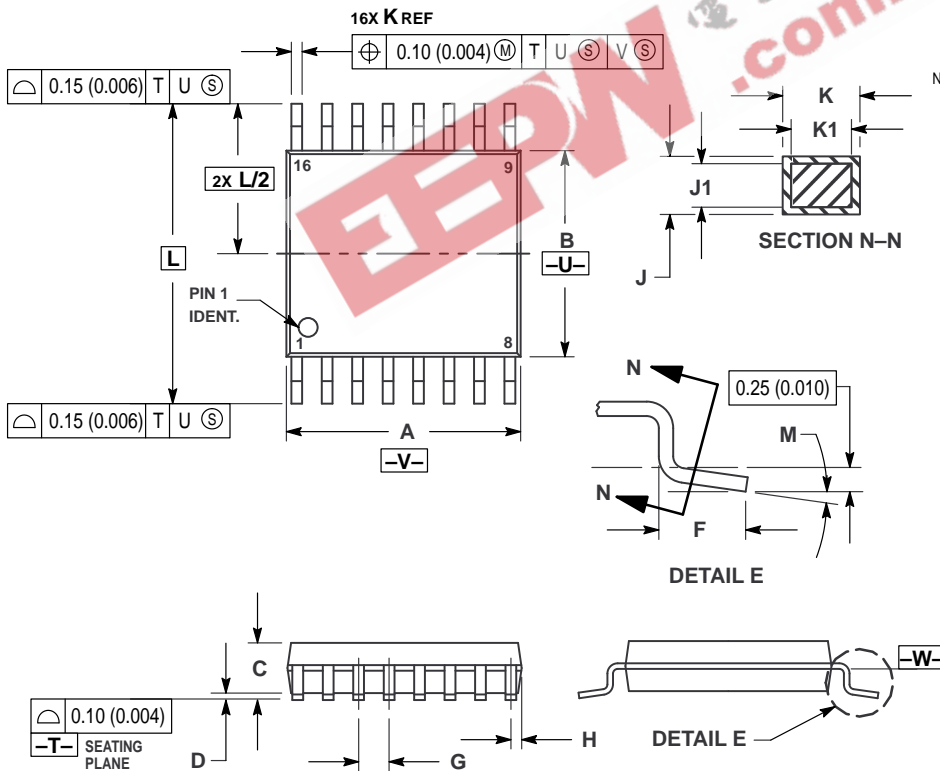
N SUFFIX
PLASTIC PACKAGE
CASE 648-08
ISSUE R



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948F-01
ISSUE O




- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

MC74HC85

EEPW 电子产品世界 .com.cn

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

How to reach us:

USA/EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, Toshikatsu Otsuki,
6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-3521-8315

MFAX: RMFAX0@email.sps.mot.com -TOUCHTONE (602) 244-6609
INTERNET: <http://Design-NET.com>

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298



◇ CODELINE

MC74HC85/D

