# **Hex Schmitt Inverter**

The MC74VHCT14A is an advanced high speed CMOS Schmitt inverter fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

Pin configuration and function are the same as the MC74VHCT04A, but the inputs have hysteresis and, with its Schmitt trigger function, the VHCT14A can be used as a line receiver which will receive slow input signals.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The VHCT14A input structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. The output structures also provide protection when  $V_{CC}=0$  V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0~V, allowing the interface of 5.0~V systems to 3.0~V systems.

#### **Features**

- High Speed:  $t_{PD} = 5.5 \text{ ns}$  (Typ) at  $V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation:  $I_{CC} = 2.0 \mu A$  (Max) at  $T_A = 25^{\circ}C$
- TTL-Compatible Inputs:  $V_{IL} = 0.8 \text{ V}$ ;  $V_{IH} = 2.0 \text{ V}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise:  $V_{OLP} = 0.8 \text{ V (Max)}$
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: 60 FETs or 15 Equivalent Gates
- Pb-Free Packages are Available\*



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MARKING DIAGRAMS



SOIC-14 D SUFFIX CASE 751A



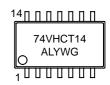


TSSOP-14 DT SUFFIX CASE 948G





SOEIAJ-14 M SUFFIX CASE 965



A = Assembly Location

WL, L = Wafer Lot
Y, YY = Year
WW, W = Work Week
G or ■ = Pb–Free Package
(Note: Microdot may be in either location)

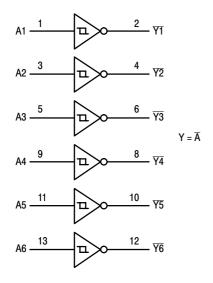
#### **FUNCTION TABLE**

Inputs	Outputs
A	Y
L	H

#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

<sup>\*</sup>For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



 $V_{CC}$ A6 <u>Y6</u> Α5 <u>Y5</u> A4 <u>Y4</u> 14 13 12 11 10 9 8 2 6 Α1 <u>Y1</u> A2 <u>Y2</u> А3 <u>Y3</u> GND

Pinout: 14-Lead Packages (Top View)

Figure 1. Logic Diagram

# **MAXIMUM RATINGS**

P	arameter	Symbol	Value	Unit
DC Supply Voltage	36.7	Vcc	-0.5 to +7.0	V
DC Input Voltage	CO	V <sub>IN</sub>	-0.5 to +7.0	V
DC Output Voltage	Output in HIGH or LOW State (Note 1)	V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> +0.5 V	V
V <sub>CC</sub> = 0 V		V <sub>OUT</sub>	-0.5 to 7.0	V
DC Input Diode Current		I <sub>IK</sub>	-20	mA
DC Output Diode Current		lok	±20	mA
DC Output Source/Sink Current		Io	±25	mA
DC Supply Current per Supply Pin		Icc	±50	mA
DC Ground Current per Ground Pin		I <sub>GND</sub>	±50	mA
Storage Temperature Range		T <sub>STG</sub>	-65 to +150	°C
Lead Temperature, 1 mm from Case for	10 Seconds	TL	260	°C
Junction Temperature under Bias		TJ	+150	°C
Thermal Resistance	SOIC TSSOP	θ <sub>JA</sub>	125 170	°C/W
Power Dissipation in Still Air	SOIC TSSOP	P <sub>D</sub>	500 450	mW
ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	V <sub>ESD</sub>	>2000 >200 2000	V
Latchup Performance	Above V <sub>CC</sub> and Below GND at 85°C (Note 5)	I <sub>Latchup</sub>	± 300	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- 1. Io absolute maximum rating must be observed.
- 2. Tested to EIA/JESD22-A114-A.
- 3. Tested to EIA/JESD22-A115-A.
- 4. Tested to JESD22-C101-A.
- Tested to EIA/JESD78.

# **RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.5	V
Input Voltage	VI	0	5.5	V
Output Voltage (Note 6)	Vo	0	V <sub>CC</sub>	V
V <sub>CC</sub> = 0 V	Vo	0	5.5	V
Operating Free–Air Temperature	T <sub>A</sub>	<b>–</b> 55	+125	°C

<sup>6.</sup> I<sub>O</sub> absolute maximum rating must be observed.

#### DC ELECTRICAL CHARACTERISTICS

			v <sub>cc</sub>	T <sub>A</sub> = 25°C		С	<b>T</b> <sub>A</sub> ≤	85°C	<b>T</b> <sub>A</sub> ≤ 1	125°C	
Parameter	Test Conditions	Symbol	v	Min	Тур	Max	Min	Max	Min	Max	Unit
Positive Threshold Voltage		V <sub>T+</sub>	4.5 5.5			1.9 2.1		1.9 2.1		1.9 2.1	V
Negative Threshold Voltage		V <sub>T-</sub>	4.5 5.5	0.5 0.6			0.5 0.6		0.5 0.6		V
Hysteresis Voltage		V <sub>H</sub>	4.5 5.5	0.40 0.40		1.40 1.50	0.40 0.40	1.40 1.50	0.40 0.40	1.40 1.50	V
Minimum High-Level Output Voltage $I_{OH} = -50 \mu A$	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50 \mu A$	V <sub>OH</sub>	4.5	4.4	4.5	5	4.4		4.4		V
	$I_{OH} = -8.0 \text{ mA}$		5.5	3.94	-	717	3.80		3.66		
Maximum Low-Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 50 \mu A$	V <sub>OL</sub>	4.5	1	0.0	0.1		0.1		0.1	V
	I <sub>OL</sub> = 8.0 mA		5. <b>5</b>	O.		0.36		0.44		0.52	
Maximum Input Leakage Current	V <sub>IN</sub> = 5.5 V or GND	I <sub>IN</sub>	0 to 5.5			±0.1		±1.0		±1.0	μΑ
Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	Icc	5.5			2.0		20		40	μΑ
Quiescent Supply Current	Input: $V_{IN} = 3.4 \text{ V}$	I <sub>CCT</sub>	5.5			1.35		1.50		1.65	mA
Output Leakage Current	V <sub>OUT</sub> = 5.5 V	loff	0.0			0.5		5.0		10	μΑ

# AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0 ns)

			T,	<sub>A</sub> = 25°	С	T <sub>A</sub> ≤	85°C	<b>T</b> <sub>A</sub> ≤ '	125°C	
Parameter	Test Conditions	Symbol	Min	Тур	Max	Min	Max	Min	Max	Unit
Maximum Propagation Delay, A to $\overline{Y}$	$V_{CC} = 5.0 \pm 0.5 \text{ V}$ $C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$	t <sub>PLH</sub> , t <sub>PHL</sub>		5.5 7.0	7.6 9.6	1.0 1.0	9.0 11.0	1.0 1.0	11.5 13.5	ns
Maximum Input Capacitance		C <sub>IN</sub>		2.0	10		10		10	pF
Power Dissipation Capacitance			Typical @ 25°C, V <sub>CC</sub> = 5.0 V							
(Note 7)		$C_{PD}$				11				pF

<sup>7.</sup> C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/6$  (per buffer). C<sub>PD</sub> is used to determine the no–load dynamic power consumption;  $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$ .

# **NOISE CHARACTERISTICS** (Input $t_r = t_f = 3.0 \text{ ns}$ , $C_L = 50 \text{ pF}$ , $V_{CC} = 5.0 \text{ V}$ )

	Т		$T_A = 25^{\circ}C$		
Characteristic	Symbol	Тур	Max	Unit	
Quiet Output Maximum Dynamic V <sub>OL</sub>	V <sub>OLP</sub>	0.8	1.0	V	
Quiet Output Minimum Dynamic V <sub>OL</sub>	V <sub>OLV</sub>	-0.8	-1.0	V	
Minimum High Level Dynamic Input Voltage	V <sub>IHD</sub>		2.0	V	
Maximum Low Level Dynamic Input Voltage	V <sub>ILD</sub>		0.8	V	

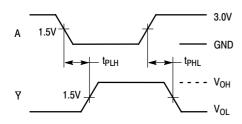
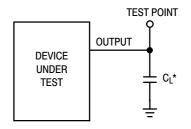


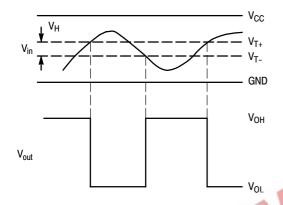
Figure 2. Switching Waveforms



\*Includes all probe and jig capacitance

Figure 3. Test Circuit

(a) A Schmitt-Trigger Squares Up Inputs With Slow Rise and Fall Times



(b) A Schmitt-Trigger Offers Maximum Noise Immunity

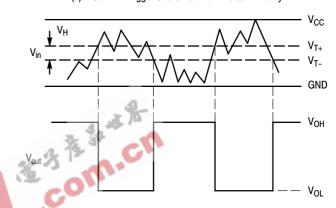


Figure 4. Typical Schmitt-Trigger Applications

# ORDERING INFORMATION

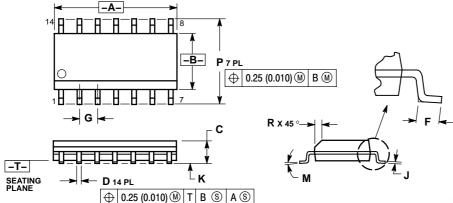
Device	Package	Shipping <sup>†</sup>
MC74VHCT14ADR2	SOIC-14	
MC74VHCT14ADR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
MC74VHCT14ADTR2	TSSOP-14*	·
MC74VHCT14ADTR2G	TSSOP-14*	
MC74VHCT14AM	SOEIAJ-14	
MC74VHCT14AMG	SOEIAJ-14 (Pb-Free)	50 Units / Rail
MC74VHCT14AMEL	SOEIAJ-14*	
MC74VHCT14AMELG	SOEIAJ-14 (Pb-Free)	2000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

<sup>\*</sup>These packages are inherently Pb-Free.

#### PACKAGE DIMENSIONS

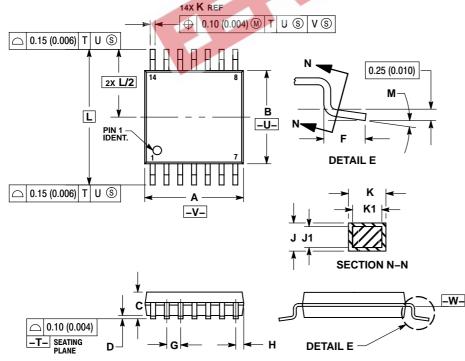
### SOIC-14 **D SUFFIX** CASE 751A-03 ISSUE G



- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) DEP SIDE
  - PER SIDE.
    5. DIMENSION D DOES NOT INCLUDE
  - DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	8.55	8.75	0.337	0.344
В	3.80	4.00	0.150	0.157
O	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	BSC	0.050	BSC
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7°	0°	7°
—P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

TSSOP-14 ASE 948G-01 ISSUE A CASE 948G-01



- NOTES:

  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

  2. CONTROLLING DIMENSION: MILLIMETER.

  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

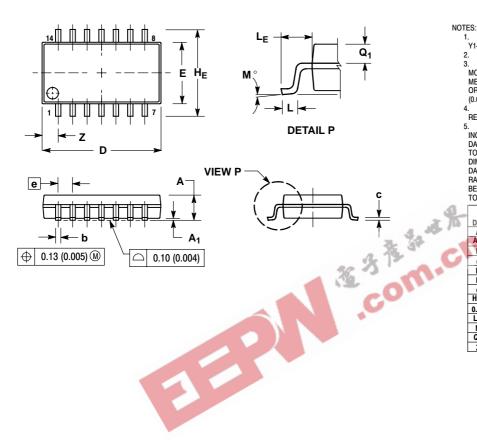
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE

  - 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  - 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY. 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIM	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	4.90	5.10	0.193	0.200
В	4.30	4.50	0.169	0.177
C	-	1.20	-	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65	BSC	0.026	BSC
Н	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40	BSC	0.252	BSC
М	0°	8 °	0 °	8 °

#### PACKAGE DIMENSIONS

SOEIAJ-14 CASE 965-01 ISSUE A



#### NOTES:

- 1. DIMEN. Y14.5M, 1982. DIMENSIONING AND TOLERANCING PER ANSI
- CONTROLLING DIMENSION: MILLIMETER. DIMENSIONS D AND E DO NOT INCLUDE
  MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15
- I. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

(0.006) PER SIDE.

THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH
DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 ( 0.018).

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
DIM	IVIIIVI	IVIAA	IVIIIV	WAX	
Α		2.05		0.081	
$A_1$	0.05	0.20	0.002	0.008	
b	0.35	0.50	0.014	0.020	
С	0.10	0.20	0.004	0.008	
D	9.90	10.50	0.390	0.413	
Е	5.10	5.45	0.201	0.215	
е	1.27	BSC	0.050	BSC	
HE	7.40	8.20	0.291	0.323	
0.50	0.50	0.85	0.020	0.033	
LE	1.10	1.50	0.043	0.059	
M	0 °	10 °	0°	10°	
Q <sub>1</sub>	0.70	0.90	0.028	0.035	
Z		1.42		0.056	

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