

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

**NONINVERTING
 QUAD THREE-STATE BUS TRANSCEIVER**

This quad three-state bus transceiver features both excellent MOS or MPU compatibility, due to its high impedance PNP transistor input, and high-speed operation made possible by the use of Schottky diode clamping. Both the -48 mA driver and -20 mA receiver outputs are short circuit protected and employ three-state enabling inputs.

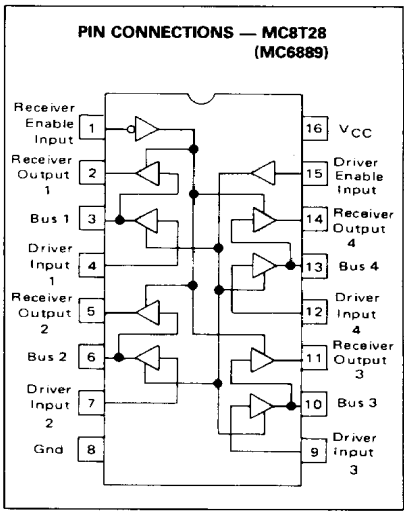
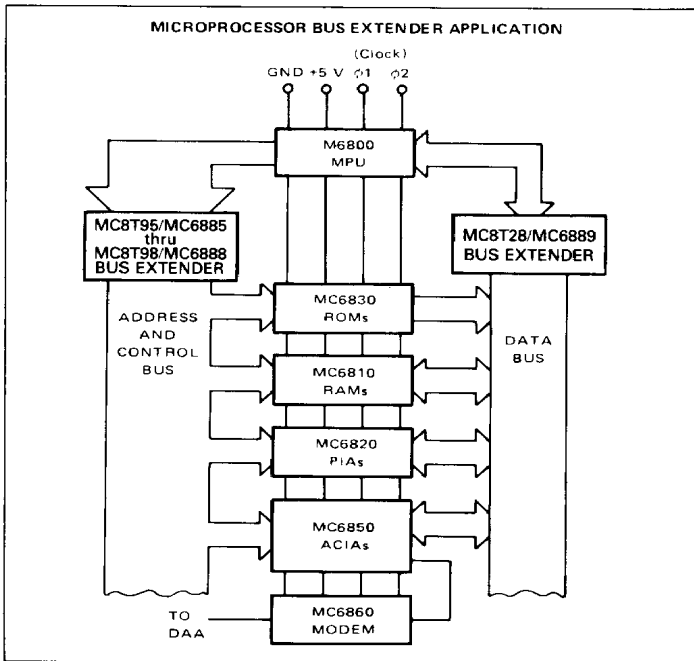
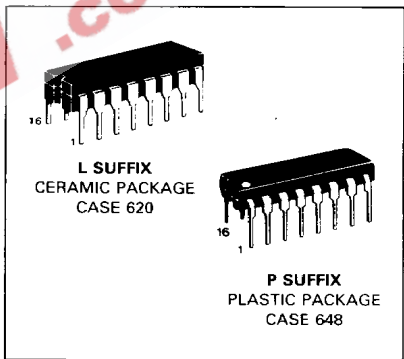
The device is useful as a bus extender in systems employing the M6800 family or other comparable MPU devices. The maximum input current of 200 μ A at any of the device input pins assures proper operation despite the limited drive capability of the MPU chip. The inputs are also protected with Schottky-barrier diode clamps to suppress excessive undershoot voltages.

Propagation delay times for the driver portion are 17 ns maximum while the receiver portion runs 17 ns. The MC8T28 is identical to the NE8T28 and it operates from a single +5 V supply.

- High Impedance Inputs
- Single Power Supply
- High Speed Schottky Technology
- Three-State Drivers and Receivers
- Compatible with M6800 Family Microprocessor
- Non-Inverting

MC8T28
 (MC6889)

**NONINVERTING
 BUS TRANSCEIVER**
 MONOLITHIC SCHOTTKY
 INTEGRATED CIRCUITS



ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC8T28L	MC6889L	0 to -75°C	Ceramic DIP
MC8T28P	MC6889P	0 to -75°C	Plastic DIP

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MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Junction Temperature	T_J		$^\circ\text{C}$
Ceramic Package		175	
Plastic Package		150	
Operating Ambient Temperature Range	T_A	0 to +75	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS (4.75 V $\leq V_{CC} \leq 5.25$ V and $0^\circ\text{C} \leq T_A \leq 75^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current – Low Logic State (Receiver Enable Input, $V_{IL}(\overline{RE}) = 0.4$ V) (Driver Enable Input, $V_{IL}(\overline{DE}) = 0.4$ V) (Driver Input, $V_{IL}(D) = 0.4$ V) (Bus (Receiver) Input, $V_{IL}(B) = 0.4$ V)	$I_{IL}(\overline{RE})$ $I_{IL}(\overline{DE})$ $I_{IL}(D)$ $I_{IL}(B)$	–	–	-200	μA
Input Disabled Current – Low Logic State (Driver Input, $V_{IL}(D) = 0.4$ V)	$I_{IL}(D)_{DIS}$	–	–	-25	μA
Input Current – High Logic State (Receiver Enable Input, $V_{IH}(\overline{RE}) = 5.25$ V) (Driver Enable Input, $V_{IH}(\overline{DE}) = 5.25$ V) (Driver Input, $V_{IH}(D) = 5.25$ V)	$I_{IH}(\overline{RE})$ $I_{IH}(\overline{DE})$ $I_{IH}(D)$	–	–	25	μA
Input Voltage – Low Logic State (Receiver Enable Input) (Driver Enable Input) (Driver Input) (Receiver Input)	$V_{IL}(\overline{RE})$ $V_{IL}(\overline{DE})$ $V_{IL}(D)$ $V_{IL}(B)$	–	–	0.85	V
Input Voltage – High Logic State (Receiver Enable Input) (Driver Enable Input) (Driver Input) (Receiver Input)	$V_{IH}(\overline{RE})$ $V_{IH}(\overline{DE})$ $V_{IH}(D)$ $V_{IH}(B)$	2.0	–	–	V
Output Voltage – Low Logic State (Bus (Driver) Output, $I_{OL}(B) = 48$ mA) (Receiver Output, $I_{OL}(R) = 20$ mA)	$V_{OL}(B)$ $V_{OL}(R)$	–	–	0.5	V
Output Voltage – High Logic State (Bus (Driver) Output, $I_{OH}(B) = -10$ mA) (Receiver Output, $I_{OH}(R) = -2.0$ mA) (Receiver Output, $I_{OH}(R) = -100\mu\text{A}$, $V_{CC} = 5.0$ V)	$V_{OH}(B)$ $V_{OH}(R)$	2.4 2.4 3.5	3.1 3.1 –	– – –	V
Output Disabled Leakage Current – High Logic State (Bus (Driver) Output, $V_{OH}(B) = 2.4$ V) (Receiver Output, $V_{OH}(R) = 2.4$ V)	$I_{OHL}(B)$ $I_{OHL}(R)$	–	–	100	μA
Output Disabled Leakage Current – Low Logic State (Bus Output, $V_{OL}(B) = 0.5$ V) (Receiver Output, $V_{OL}(R) = 0.5$ V)	$I_{OLL}(B)$ $I_{OLL}(R)$	–	–	-100	μA
Input Clamp Voltage (Driver Enable Input $I_{ID}(\overline{DE}) = -12$ mA) (Receiver Enable Input $I_{IC}(\overline{RE}) = +12$ mA) (Driver Input $I_{IC}(D) = -12$ mA)	$V_{IC}(\overline{DE})$ $V_{IC}(\overline{RE})$ $V_{IC}(D)$	–	–	-1.0	V
Output Short Circuit Current, $V_{CC} = 5.25$ V, Note 1 (Bus (Driver) Output) (Receiver Output)	$I_{OS}(B)$ $I_{OS}(R)$	-50 -30	–	-150 -75	mA
Power Supply Current ($V_{CC} = 5.25$ V)	I_{CC}	–	–	110	mA

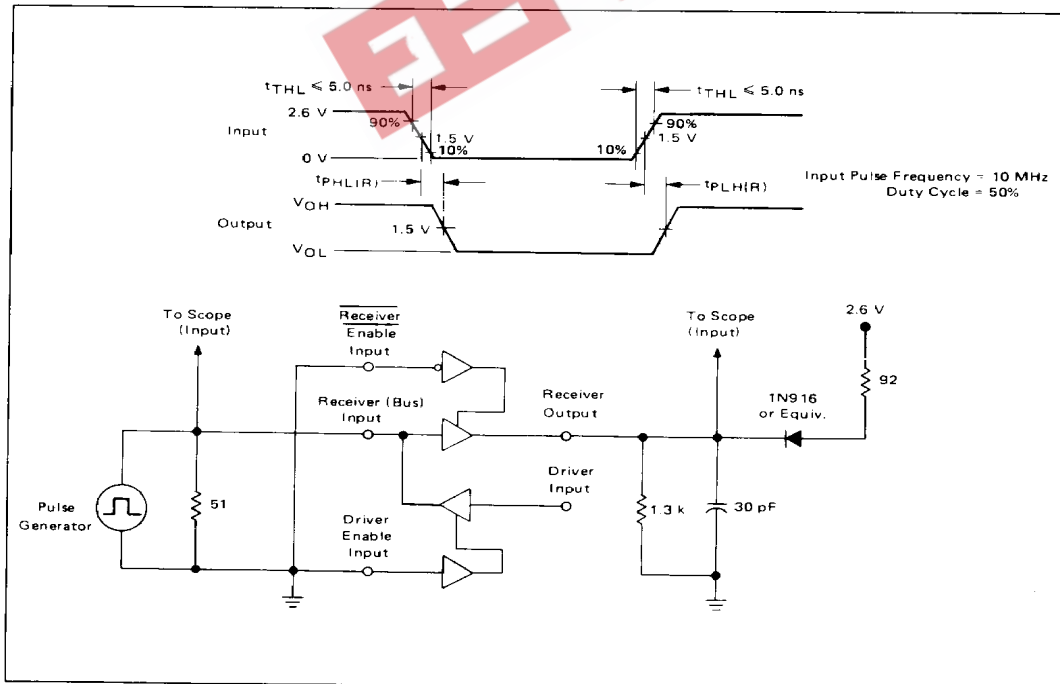
Note 1. Only one output may be short-circuited at a time.

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SWITCHING CHARACTERISTICS (Unless otherwise noted, $V_{CC} = 5.0\text{ V}$ and $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	Min	Max	Unit
Propagation Delay Time—Receiver ($C_L = 30\text{ pF}$)	$t_{PLH}(R)$	—	17	ns
	$t_{PHL}(R)$	—	17	ns
Propagation Delay Time—Driver ($C_L = 300\text{ pF}$)	$t_{PLH}(D)$	—	17	ns
	$t_{PHL}(D)$	—	17	ns
Propagation Delay Time—Enable ($C_L = 30\text{ pF}$)	$t_{PZL}(R)$	—	23	ns
	$t_{PLZ}(R)$	—	18	ns
	$t_{PZL}(D)$	—	28	ns
	$t_{PLZ}(D)$	—	23	ns

FIGURE 1 — TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY FROM BUS (RECEIVER) INPUT TO RECEIVER OUTPUT, $t_{PLH}(R)$ AND $t_{PHL}(R)$



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FIGURE 2 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER INPUT TO BUS (DRIVER) OUTPUT, $t_{PLH(D)}$ AND $t_{PHL(D)}$

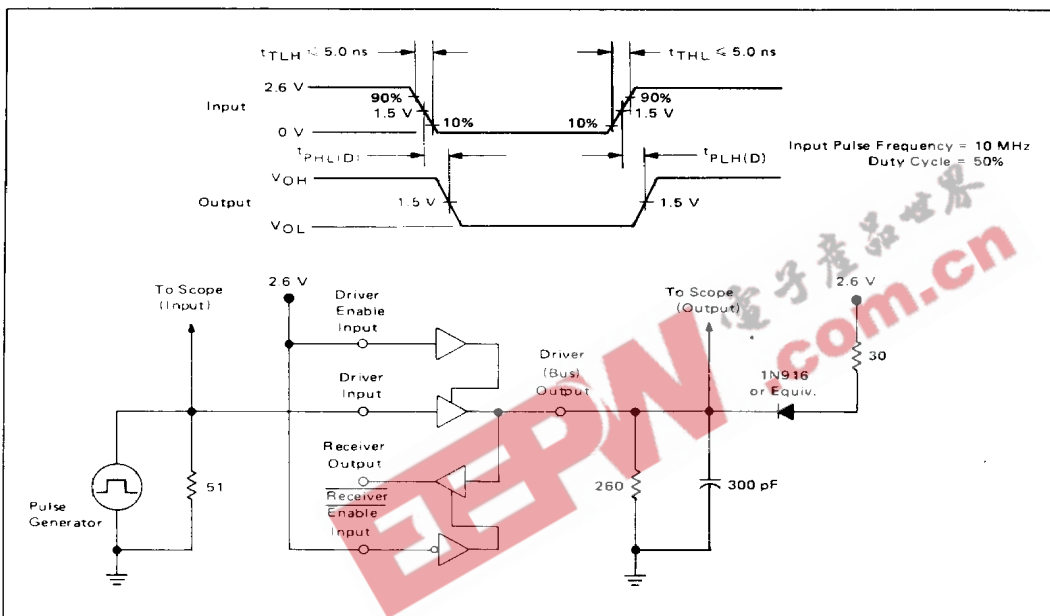
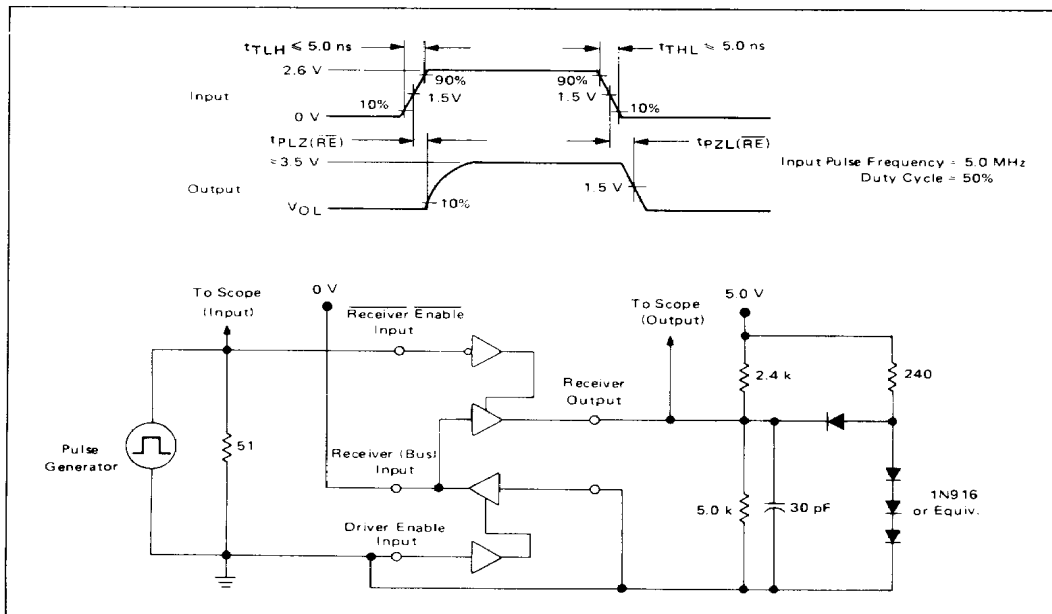


FIGURE 3 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER ENABLE INPUT TO RECEIVER OUTPUT, $t_{PLZ(RE)}$ AND $t_{PZL(RE)}$



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FIGURE 4 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIMES FROM DRIVER ENABLE INPUT TO DRIVER (BUS) OUTPUT, $t_{PLZ(DE)}$ AND $t_{PZL(DE)}$

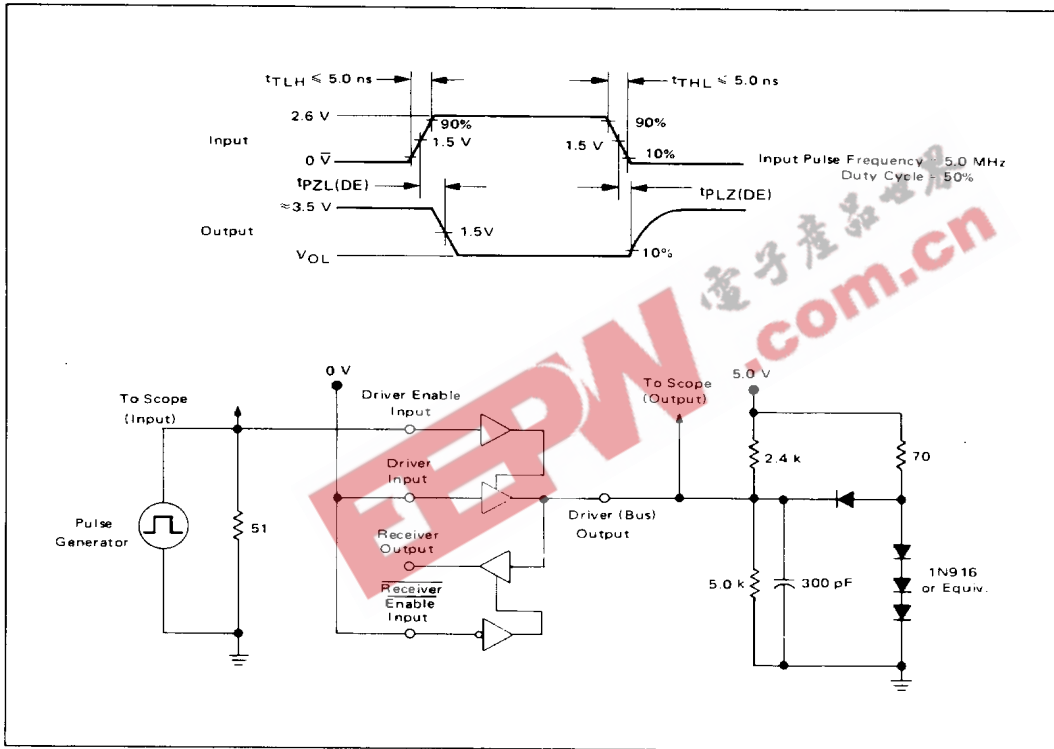


FIGURE 5 – BIDIRECTIONAL BUS APPLICATIONS

