MCR8DSM, MCR8DSN

Preferred Device

Sensitive Gate Silicon Controlled Rectifiers

Reverse Blocking Thyristors

Designed for high volume, low cost, industrial and consumer applications such as motor control; process control; temperature, light and speed control.

Features

- Small Size
- Passivated Die for Reliability and Uniformity
- Low Level Triggering and Holding Characteristics
- Available in Two Package Styles
  Surface Mount Lead Form − Case 369C
  Miniature Plastic Package − Straight Leads − Case 369
- Epoxy Meets UL 94 V−0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V
  Machine Model, C > 400 V
- Pb−Free Packages are Available

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off−State Voltage (Note 1) (T_J = −40 to 110°C, Sine Wave, 50 to 60 Hz, Gate Open) MCR8DSM MCR8DSN	V_{DRM}, V_{RRM}	600 800	V
On−State RMS Current (180° Conduction Angles; T_C = 90°C)	$I_{T(RMS)}$	8.0	A
Average On−State Current (180° Conduction Angles; T_C = 90°C)	$I_{T(AV)}$	5.1	A
Peak Non-Repetitive Surge Current (1/2 Cycle, Sine Wave 60 Hz, T_J = 110°C)	I_{TSM}	90	A
Circuit Fusing Consideration (t = 8.3 msec)	I^2t	34	A^2sec
Forward Peak Gate Power (Pulse Width ≤ 1.0 μsec, T_C = 90°C)	P_{GM}	5.0	W
Forward Average Gate Power (t = 8.3 msec, T_C = 90°C)	$P_{G(AV)}$	0.5	W
Forward Peak Gate Current (Pulse Width ≤ 1.0 μsec, T_C = 90°C)	I_{GM}	2.0	A
Operating Junction Temperature Range	T_J	−40 to 110	°C
Storage Temperature Range	T_{stg}	−40 to 150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

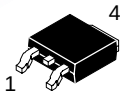
1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for negative gate voltage; positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the device are exceeded.

ON Semiconductor®

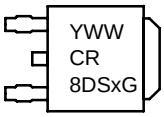
http://onsemi.com

SCRs
8 AMPERES RMS
600 − 800 VOLTS

MARKING DIAGRAM



DPAK
CASE 369C
STYLE 4



Y = Year
WW = Work Week
CR8DSx = Device Code
x= M or N
G = Pb−Free Package

PIN ASSIGNMENT	
1	Cathode
2	Anode
3	Gate
4	Anode

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance − Junction−to−Case − Junction−to−Ambient − Junction−to−Ambient (Note 2)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	2.2 88 80	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 10 Seconds	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristics		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Peak Repetitive Forward or Reverse Blocking Current (V_{AK} = Rated V_{DRM} or V_{RRM}; R_{GK} = 1.0 kΩ) (Note 3)	T_J = 25°C T_J = 110°C	I_{DRM} I_{RRM}	− −	− −	10 500	μA
ON CHARACTERISTICS						
Peak Reverse Gate Blocking Voltage (I_{GR} = 10 μA)		V_{GRM}	10	12.5	18	V
Peak Reverse Gate Blocking Current (V_{GR} = 10 V)		I_{RGM}	−	−	1.2	μA
Peak Forward On−State Voltage (Note 4) (I_{TM} = 16 A)		V_{TM}	−	1.4	1.8	V
Gate Trigger Current (Continuous dc) (Note 5) (V_D = 12 V, R_L = 100 Ω)	T_J = 25°C T_J = −40°C	I_{GT}	5.0 −	12 −	200 300	μA
Gate Trigger Voltage (Continuous dc) (Note 5) (V_D = 12 V, R_L = 100 Ω)	T_J = 25°C T_J = −40°C T_J = 110°C	V_{GT}	0.45 − 0.2	0.65 − −	1.0 1.5 −	V
Holding Current (V_D = 12 V, Initiating Current = 200 mA, Gate Open)	T_J = 25°C T_J = −40°C	I_H	0.5 −	1.0 −	6.0 10	mA
Latching Current (V_D = 12 V, I_G = 2.0 mA)	T_J = 25°C T_J = −40°C	I_L	0.5 −	1.0 −	6.0 10	mA
Total Turn−On Time (Source Voltage = 12 V, R_S = 6.0 kΩ, I_T = 16 A(pk), R_{GK} = 1.0 kΩ) (V_D = Rated V_{DRM}, Rise Time = 20kns, Pulse Width = 10 μs)		tgt	−	2.0	5.0	μs
DYNAMIC CHARACTERISTICS						
Critical Rate of Rise of Off−State Voltage (V_D = 0.67 X Rated V_{DRM}, Exponential Waveform, R_{GK} = 1.0 kΩ, T_J = 110°C)		dv/dt	2.0	10	−	V/μs

2. Surface mounted on minimum recommended pad size.
3. Ratings apply for negative gate voltage or R_{GK} = 1.0 kΩ. Devices shall not have a positive gate voltage concurrently with a negative voltage on the anode. Devices should not be tested with a constant current source for forward and reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.
4. Pulse Test; Pulse Width ≤ 2.0 msec, Duty Cycle ≤ 2%.
5. R_{GK} current not included in measurements.

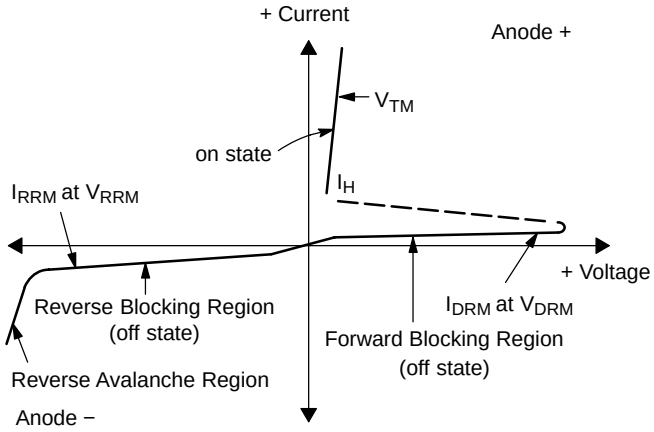
ORDERING INFORMATION

Device	Package	Shipping†
MCR8DSMT4	DPAK	2500 / Tape & Reel
MCR8DSMT4G	DPAK (Pb−Free)	
MCR8DSNT4	DPAK	
MCR8DSNT4G	DPAK (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Voltage Current Characteristic of SCR

Symbol	Parameter
V_{DRM}	Peak Repetitive Off−State Forward Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Off−State Reverse Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Peak On−State Voltage
I_H	Holding Current



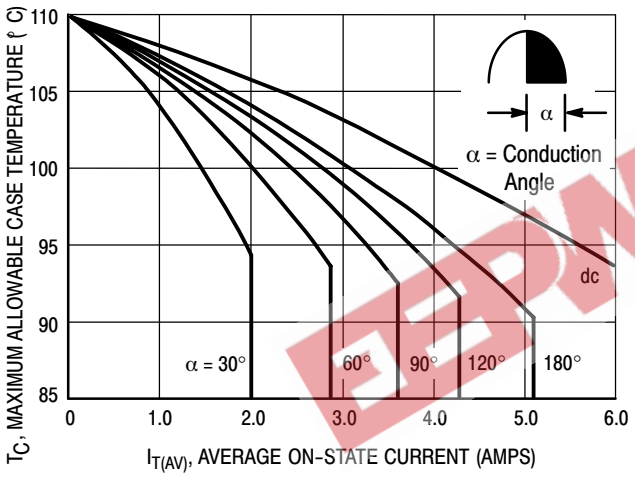


Figure 1. Average Current Derating

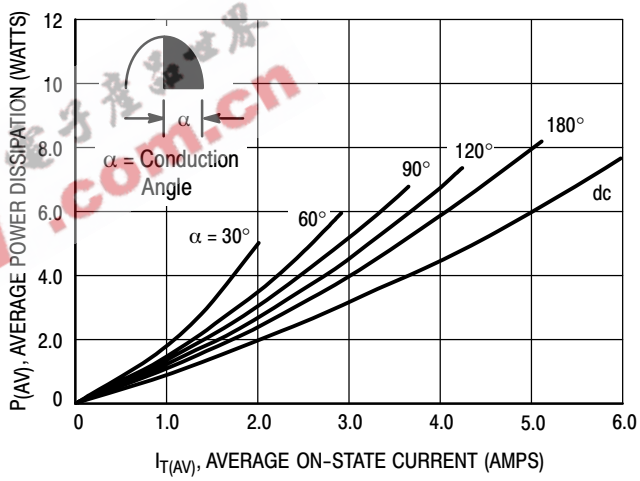


Figure 2. On−State Power Dissipation

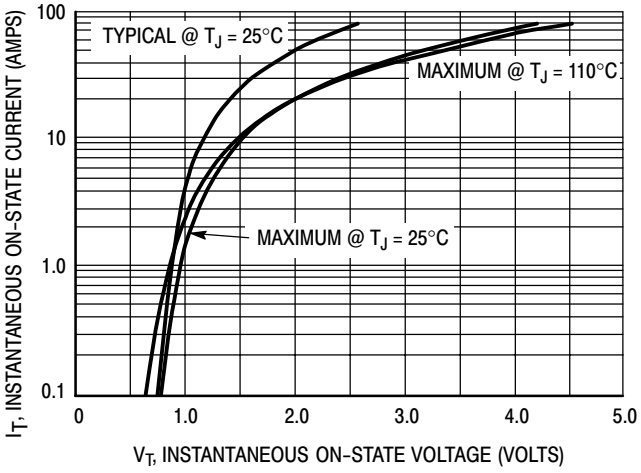


Figure 3. On−State Characteristics

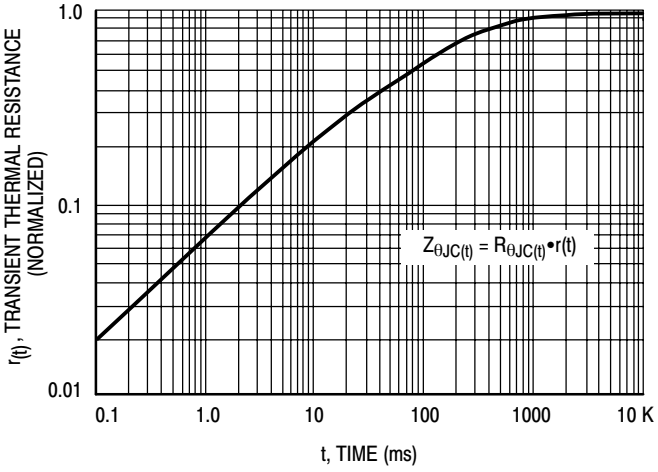


Figure 4. Transient Thermal Response

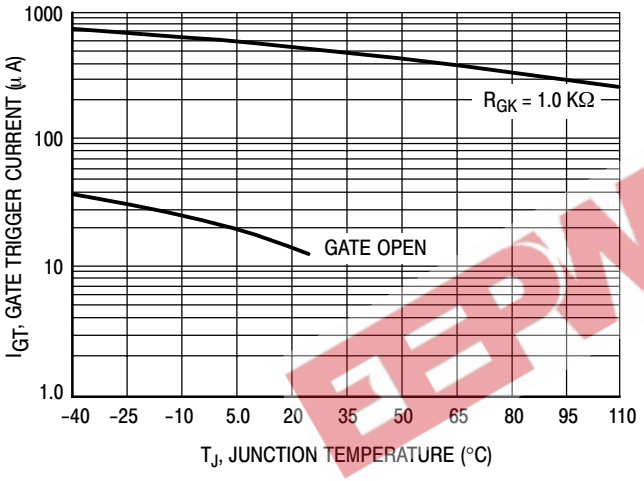


Figure 5. Typical Gate Trigger Current versus Junction Temperature

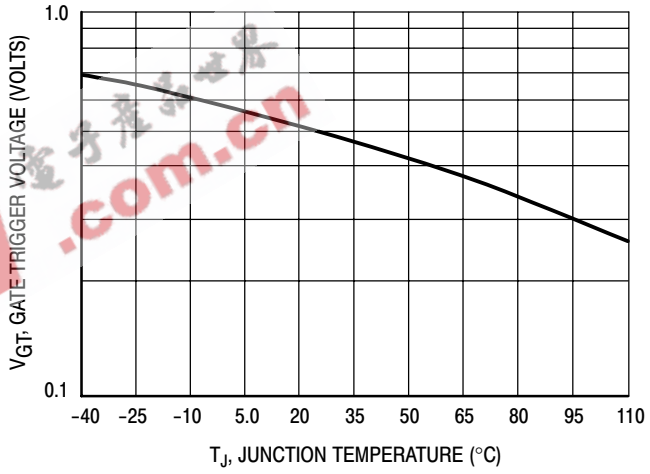


Figure 6. Typical Gate Trigger Voltage versus Junction Temperature

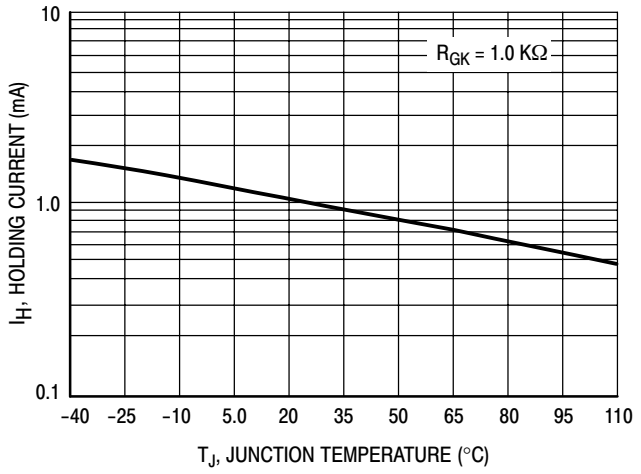


Figure 7. Typical Holding Current versus Junction Temperature

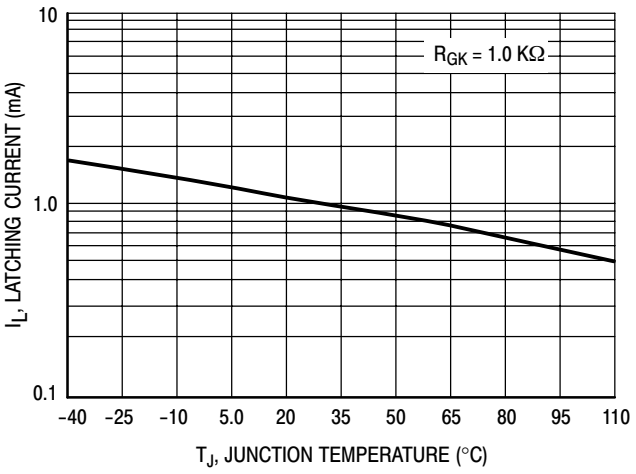


Figure 8. Typical Latching Current versus Junction Temperature

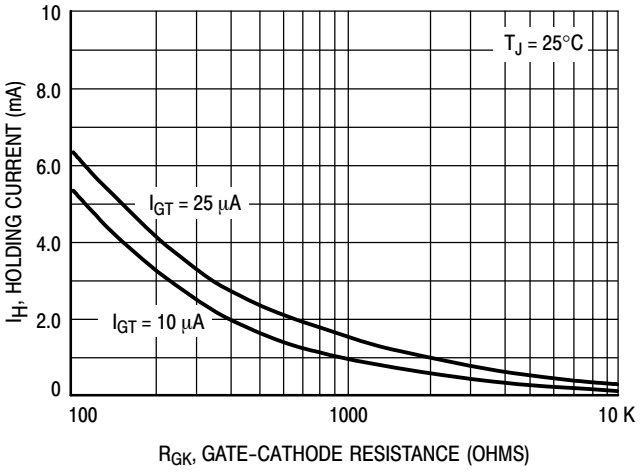


Figure 9. Holding Current versus Gate−Cathode Resistance

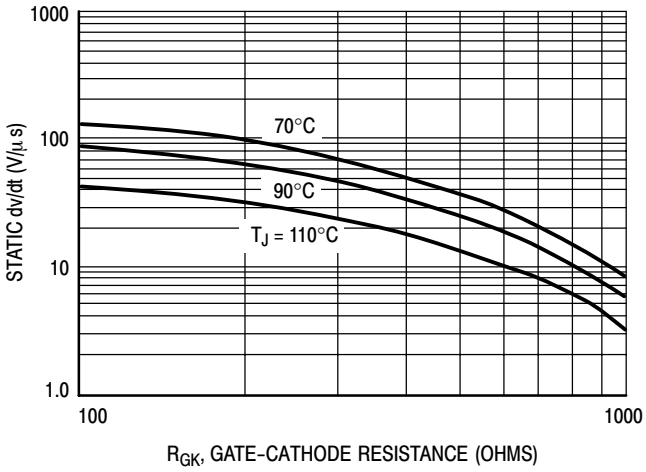


Figure 10. Exponential Static dv/dt versus Gate−Cathode Resistance and Junction Temperature

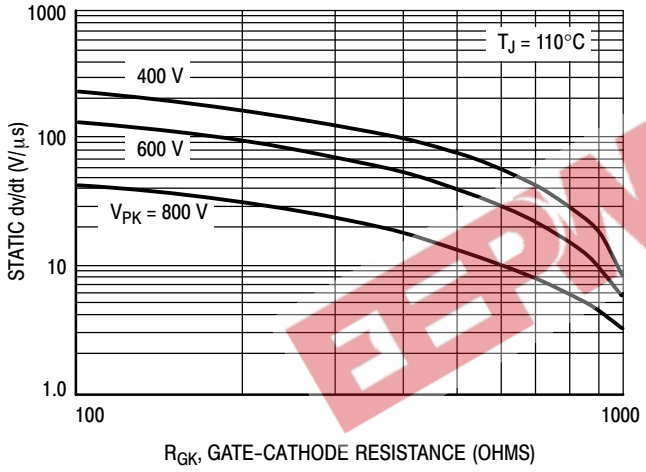


Figure 11. Exponential Static dv/dt versus Gate−Cathode Resistance and Peak Voltage

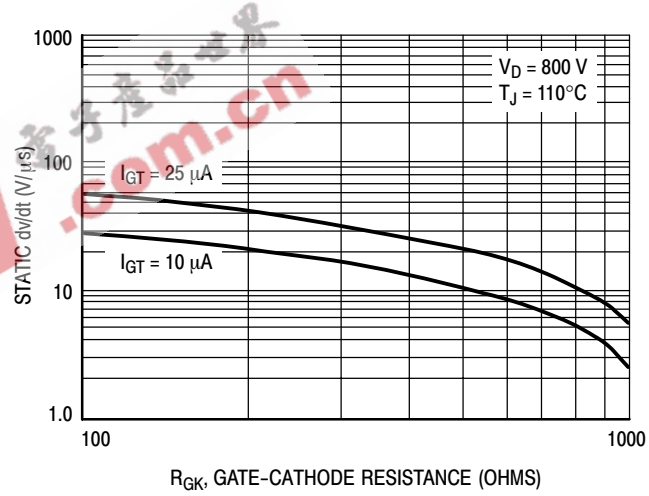
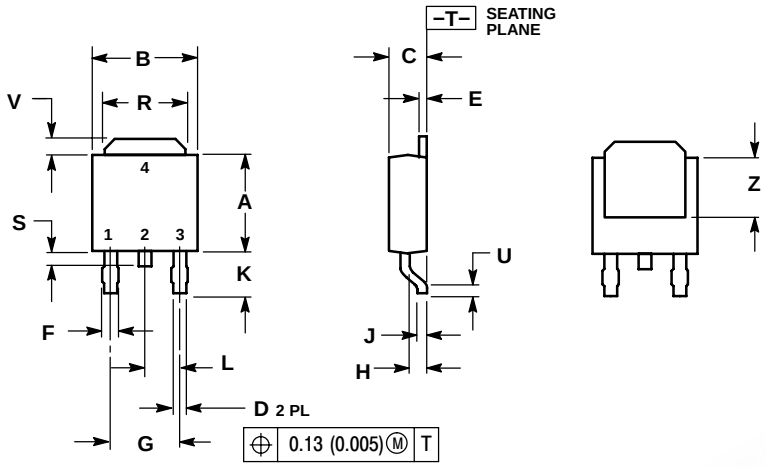


Figure 12. Exponential Static dv/dt versus Gate−Cathode Resistance and Gate Trigger Current Sensitivity

MCR8DSM, MCR8DSN

PACKAGE DIMENSIONS

DPAK
CASE 369C
ISSUE O

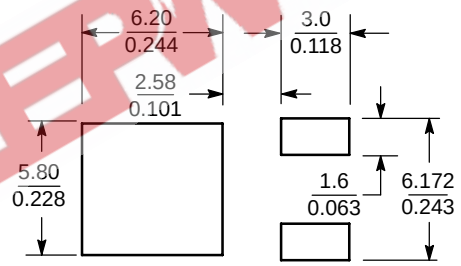


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

SOLDERING FOOTPRINT*



SCALE 3:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
Phone: 480−829−7710 or 800−344−3860 Toll Free USA/Canada
Fax: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
Phone: 81−3−5773−3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.