UNISONIC TECHNOLOGIES CO., LTD

MJE13003

NPN EPITAXIAL SILICON TRANSISTOR

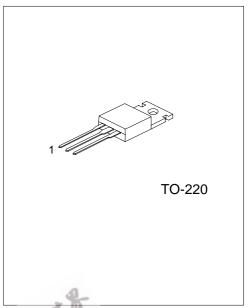
NPN SILICON POWER TRANSISTORS

DESCRIPTION

These devices are designed for high–voltage, high–speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220V SWITCHMODE.

■ FEATURES

- * Reverse Biased SOA with Inductive Load @ Tc=100°C
- * Inductive Switching Matrix $0.5 \sim 1.5$ Amp, 25 and 100° C Typical tc = 290ns @ 1A, 100° C.
- * 700V Blocking Capability



*Pb-free plating product number: MJE13003L

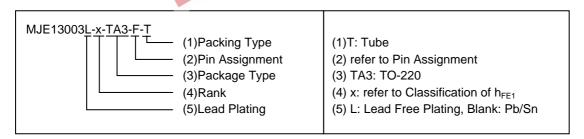
■ APPLICATIONS

- * Switching Regulator's, Inverters
- * Motor Controls
- * Solenoid/Relay drivers
- * Deflection circuits

■ ORDERING INFORMATION

Order	Package	Pin Assignment			Dooking		
Normal	Lead Free Plating	rackage	1	2	3	Packing	
MJE13003-x-TA3-F-T	MJE13003L-x-TA3-F-T	TO-220	В	C	Е	Tube	

Note: x: Rank, refer to Classification of hFE1.



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER			RATINGS	UNIT
Collector-Emitter Voltage			400	V
Collector-Emitter Voltage			700	V
Emitter Base Voltage			9	V
Collector Current	Continuous	I _C	1.5	А
Collector Current	Peak (1)	I _{CM}	3	A
Base Current	Continuous	I _B	0.75	А
base Current	Peak (1)	I _{BM}	1.5	Α
Emitter Current	Continuous	Ι _Ε	2.25	Α
Emiller Current	Peak (1)	I _{EM}	4.5	A
Total Power Dissipation @ Ta=25°C		0	1.4	W
Derate above 25 [°] C		P_{D}	11.2	mW/°C
Total Power Dissipation @ T _C =25°C		0	40	W
Derate above 25°C		P_{D}	320	mW/°C
Junction Temperature		TJ	150	$^{\circ}\mathbb{C}$
Storage Temperature		T _{STG}	-40 ~ +150	$^{\circ}\!\mathbb{C}$

Note Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Thermal Resistance, Junction to Ambient	R JA	89	°C/W
Thermal Resistance, Junction to Case	R JC	3.12	°C/W

⁽¹⁾ Pulse Test: Pulse Width=5ms, Duty Cycle 10%

■ ELECTRICAL CHARACTERISTICS (T_C=25°C, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS		TYP	MAX	UNIT
OFF CHARACTERISTICS (Note)		_	_	_		
Collector-Emitter Sustaining Voltage	V _{CEO(SUS)}	I _C =10 mA , I _B =0	400			V
Collector Cutoff Current		V _{CEO} =Rated Value, T _C =25°C			1	mΑ
Collector Cutoff Current	ICEO	V _{BE(OFF)} =1.5 V T _C =100°C			5	
Emitter Cutoff Current	I _{EBO}	$V_{EB}=9 \text{ V}, I_{C}=0$			1	mA
SECOND BREAKDOWN			_			
Second Breakdown Collector Current	ls/b		See Figure 5			
with bass forward biased	15/0		36	e rigui	e 5	
Clamped Inductive SOA with base	RBSOA		90	e Figur	2.6	
reverse biased	NBSOA		36	e i igui	- 0	
ON CHARACTERISTICS (Note)						
DC Current Gain	h _{FE1}	I _C =0.5A, V _{CE} =2V	8		40	
Do darrent dam	h _{FE2}	I _C =1A, V _{CE} =2V	5		25	
	V _{CE(SAT)}	I _C =0.5A, I _B =0.1A			0.5	1
Collector-Emitter Saturation Voltage		I _C =1A, I _B =0.25A			1	V
Collector-Emitter Saturation Voltage		I _C =1.5A, I _B =0.5A			3	
		I _C =1A, I _B =0.25A, T _C =100			1	
		I _C =0.5A, I _B =0.1A			1	
Base-Emitter Saturation Voltage	$V_{BE(SAT)}$	$I_{C}=1A$, $I_{B}=0.25A$	1.2			V
		I _C =1A, I _B =0.25A, T _C =100°C		1.1		
DYNAMIC CHARACTERISTICS						
Current-Gain-Bandwidth Product	f⊤	I _C =100mA, V _{CE} =10V, f=1MHz	4	10		MHz
Output Capacitance	Cob	V_{CB} =10V, I_E =0, f=0.1MHz		21		pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	t _D			0.05	0.1	μ s
Rise Time	t _R	$V_{CC}=125V$, $I_{C}=1A$, $I_{B1}=I_{B2}=0.2A$,		0.5	1	μ s
Storage Time	t _S	t_P =25 μ s, Duty Cycle 1%		2	4	μs
Fall Time	t _{FALL}			0.4	0.7	μ s

■ ELECTRICAL CHARACTERISTICS(Cont.)

		•				
PARAMETER	SYMBOL TEST CONDITIONS		MIN	TYP	MAX	UNIT
Inductive Load, Clamped (Table 1)						
Storage Time	t _{SV}	1 44 1/515 75 7 0001/ 1 0 04		1.7	4	μ s
Crossover Time	t _C	I _C =1A, Vclamp=300V, I _{B1} =0.2A, V _{BE(OFF)} =5Vdc, T _C =100°C		0.29	0.75	μ s
Fall Time	t _{FALL}	VBE(OFF)=3 VGC, TC=100 C		0.15		μ s

Note: Pulse Test : PW=300 μ s, Duty Cycle 2%

■ CLASSIFICATION OF h_{FE1}

RANK	А	В	С	D	E	F
RANGE	8 ~ 16	15 ~ 21	20 ~ 26	25 ~ 31	30 ~ 36	35 ~ 40

Table 1.Test Conditions for Dynamic Performance

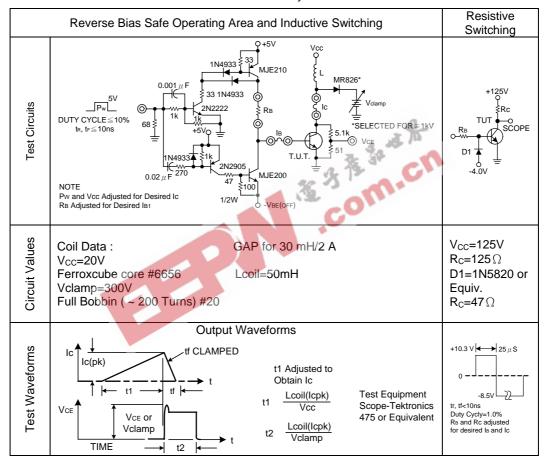


Figure 1. Inductive Switching Measurements

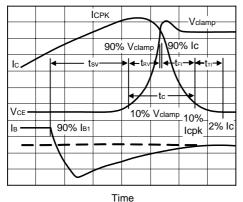


Table 2. Typical Inductive Switching Performance

Ic	Tc	tsv	t _{RV}	t _{Fl}	tπ	tc
AMP	℃	μS	μS	μs	μs	μs
0.5	25	1.3	0.23	0.30	0.35	0.30
	100	1.6	0.26	0.30	0.40	0.36
1	25	1.5	0.10	0.14	0.05	0.16
	100	1.7	0.13	0.26	0.06	0.29
1.5	25	1.8	0.07	0.10	0.05	0.16
	100	3	0.08	0.22	0.08	0.28

NOTE: All Data Recorded in the Inductive Switching Circuit in Table 1

■ SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads, which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{SV} = Voltage Storage Time, 90% I_{B1} to 10% Vclamp

 t_{RV} = Voltage Rise Time, 10 ~ 90% Vclamp

t_{FI}= Current Fall Time, 90 ~ 10% I_C

 t_{TI} = Current Tail, 10 ~ 2% I_{C}

 t_C = Crossover Time, 10% Vclamp to 10% I_C

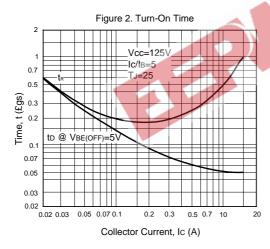
An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these Terms. For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222:

 $PSWT = 1/2 V_{CC}I_{C}(t_{C})f$

In general, t_{RV} + t_{Fl} t_C. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25° C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_C and t_{SV}) which are guaranteed at 100° C.

RESISTIVE SWITCHING PERFORMANCE



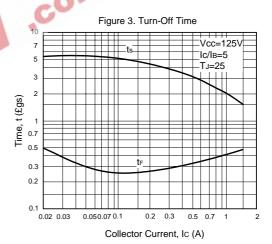


Figure 4. Thermal Response 0.7 0.5 (Normalized) Effective Transient Thermal esistance, R(t) (Normalized 0.3 0.2 0.2 .0.1 $Z_{\theta} JC(t)=r(t) R_{\theta} JC$ 0.1 R _θ JC=3.12°C/W Max 0.07 D Curves Apply for Power Resistance, 0.05 Pulse Train Shown tı l€ Read Time at t1 0.03 - t2 0.01TJ(pk)-TC=P(pk) $P \theta JC(t)$ Duty Cycle, D=t1/t2 0.02 Single Pulse 0.01 0.01 0.02 0.03 0.05 0.2 0.3 0.5 3 10 20 100 200 500 Time or Pulse Width, t (ms)

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

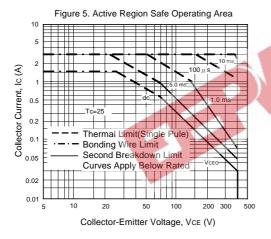
The data of Figure 5 is based on $T_C = 25^{\circ}C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 5 may be found at any case temperature by using the appropriate curve on Figure 7.

 $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 6 gives PBSOA characteristics.

The Safe Operating Area of figures 5 and 6 are specified ratings (for these devices under the test conditions shown.)



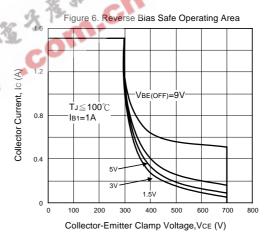


Figure 7. Forward Bias Power Derating

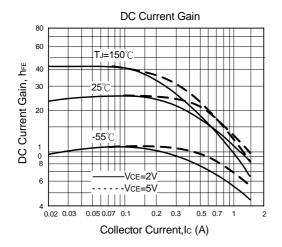
0.8 Second Breakdown
Derating

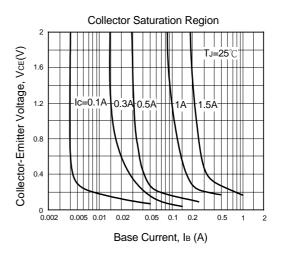
0.6 Thermal
Derating

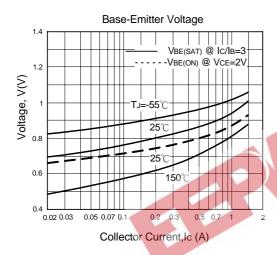
0.7 Derating

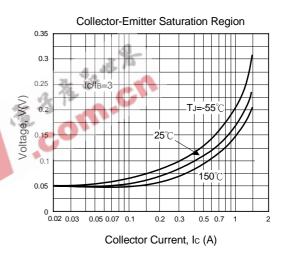
0.8 Case Temperature, Tc (°C)

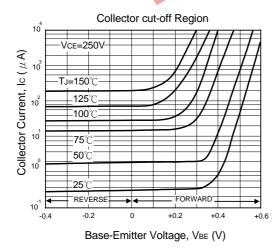
■ TYPICAL PERFORMANCE CHARACTERISTICS

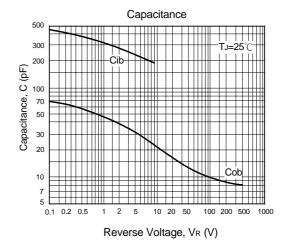














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