LANSDALE Semiconductor, Inc.

ML13150
Narrowband FM Coilless Detector IF Subsystem

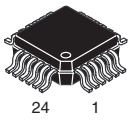
NARROWBAND FM COILLESS DETECTOR IF SUBSYSTEM FOR CELLULAR AND ANALOG APPLICATIONS

SEMICONDUCTOR TECHNICAL DATA

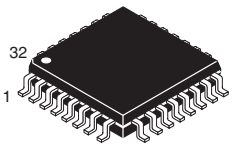
Legacy Device: *Motorola MC13150*

The ML13150 is a narrowband FM IF subsystem targeted at cellular and other analog applications. The ML13150 has an onboard Colpitts VCO that can be crystal controlled or phased lock for second LO in dual conversion receivers. The mixer is a double balanced configuration with excellent third order intercept. It is useful to beyond 200 MHz. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections., The quadrature detector is a unique design eliminating the conventional tunable quadrature coil.

Applications for the ML13150 include cellular, CT-1, 900 MHz cordless telephone, data links and other radio systems utilizing narrowband FM modulation.



ML13150-A9P
PLASTIC PACKAGE
(LQFP-24)



ML13150-B9P
PLASTIC PACKAGE
(LQFP-32)

CROSS REFERENCE/ORDERING INFORMATION

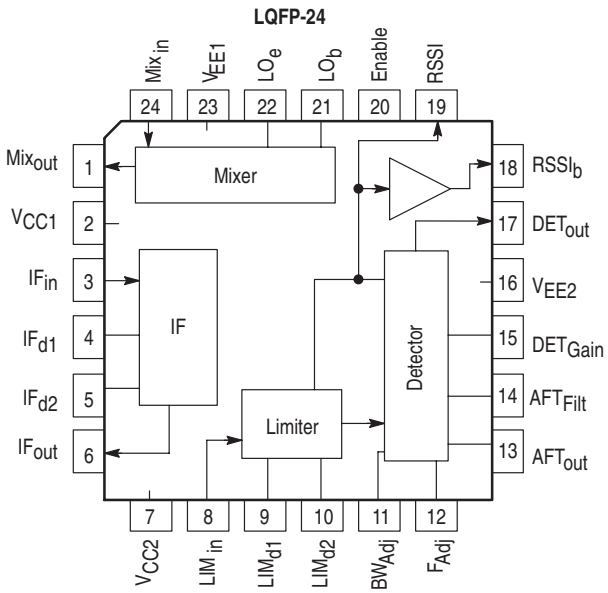
PACKAGE	MOTOROLA	LANSDALE
LQFP-24	MC13150FTA	ML13150-A9P
LQFP-32	MC13150FTB	ML13150-B9P

Note: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

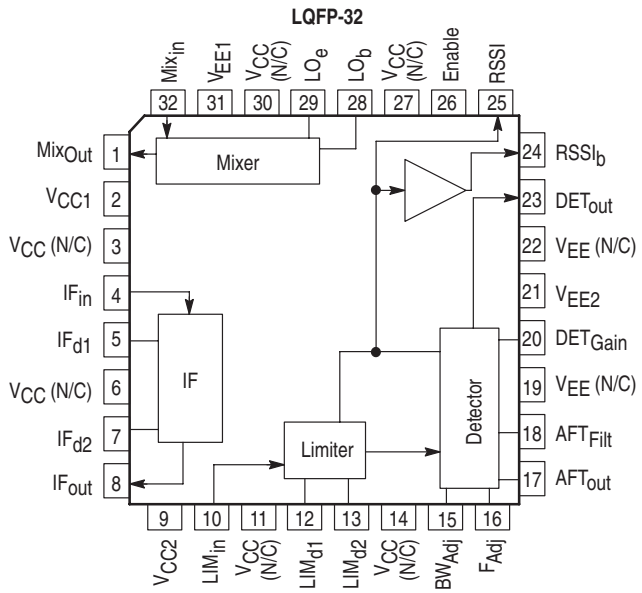
- Linear Coilless Detector
- Adjustable Demodulator Bandwidth
- 2.5 to 6.0 Vdc Operation
- Low Drain Current <2.0 mA
- Typical Sensitivity of 2.0 µV for 12 dB SINAD
- IIP3, Input Third Order Intercept Point of 0 dBm
- RSSI Range of Greater Than 100 dB
- Internal 1.4 kΩ Terminations for 455 kHz Filters
- Split IF for Improved filtering and Extended RSSI Range
- Operating Temperature Range - T_A = -40° to +85°C

PIN CONNECTIONS

LQFP-24



LQFP-32



MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	2, 9	V_{CC}(max)	6.5	Vdc
Junction Temperature	-	T_{Jmax}	+150	C
Storage Temperature Range	-	T_{stg}	-65 to +150	C

NOTE: 1. Devices should not be operated at or outside these values. The "Recommended Operating Limits" provide for actual device operation.
2. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage T_A = 25 C –40 C T_A 85 C (See Figure 22)	2, 9 21, 31	V_{CC} V_{EE}	2.5 to 6.0 0	Vdc
Input Frequency	32	f_{in}	10 to 500	MHz
Ambient Temperature Range	-	T_A	-40 to +85	C
Input Signal Level	32	V_{in}	0	dBm

DC ELECTRICAL CHARACTERISTICS (T_A = 25 C, V_{CC1} = V_{CC2} = 3.0 Vdc, No Input Signal.)

Characteristics	Condition	Pin	Symbol	Min	Typ	Max	Unit
Total Drain Current (See Figure 2)	V_S = 3.0 Vdc	2 + 9	I_{TOTAL}	-	1.7	3.0	mA
Supply Current, Power Down (See Figure 3)	-	2 + 9	-	-	40	-	nA

AC ELECTRICAL CHARACTERISTICS (T_A = 25 C, V_S = 3.0 Vdc, f_{RF} = 50 MHz, f_{LO} = 50.455 MHz, LO Level = –10 dBm, see Figure 1 Test Circuit*, unless otherwise specified.)

Characteristics	Condition	Pin	Symbol	Min	Typ	Max	Unit
12 dB SINAD Sensitivity (See Figure 15)	f_{mod} = 1.0 kHz; f_{dev} = ±5.0 kHz	32	-	-	–100	-	dBm
RSSI Dynamic Range (See Figure 7)	-	25	-	-	100	-	dB
Input 1.0 dB Compression Point Input 3rd Order Intercept Point (See Figure 18)	- -	- -	1.0 dB C. Pt. IIP3	- -	-11 -1.0	- -	dBm
Coilless Detector Bandwidth Adjust (See Figure 11)	Measured with No IF Filters	-	ΔBW adj	-	26	-	kHz/μA
MIXER							
Conversion Voltage Gain (See Figure 5)	P_{in} = -30 dBm; PLO = -10 dBm	32	-	-	10	-	dB
Mixer Input Impedance	Single-Ended	32	-	-	200	-	Ω
Mixer Output Impedance	-	1	-	-	1.5	-	kΩ
LOCAL OSCILLATOR							
LO Emitter Current (See Figure 26)	-	29	-	30	63	100	μA
IF & LIMITING AMPLIFIERS SECTION							
IF and Limiter RSSI Slope	Figure 7	25	-	-	0.4	-	μA/dB
IF Gain	Figure 8	4, 8	-	-	42	-	dB
IF Input & Output Impedance	-	4, 8	-	-	1.5	-	kΩ
Limiter Input Impedance	-	10	-	-	1.5	-	kΩ
Limiter Gain	-	-	-	-	96	-	dB

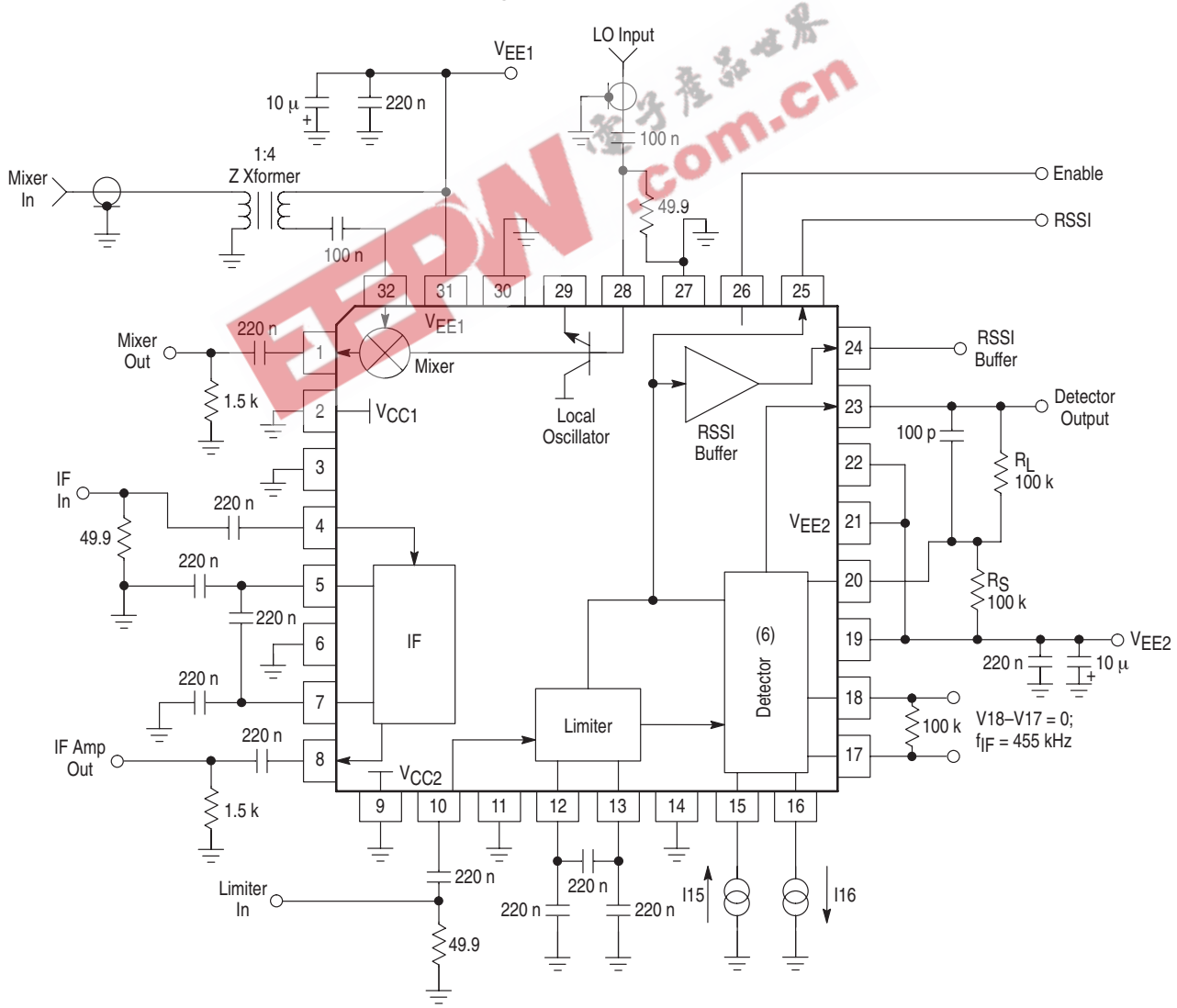
* Figure 1 Test Circuit uses positive (V_{CC}) Ground.

AC ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C, V_S = 3.0 Vdc, f_{RF} = 50 MHz, f_{LO} = 50.455 MHz, LO Level = -10 dBm, see Figure 1 Test Circuit*, unless otherwise specified.)

Characteristics	Condition	Pin	Symbol	Min	Typ	Max	Unit
DETECTOR							
Frequency Adjust Current	Figure 9, f_{IF} = 455 kHz	16	-	41	49	56	μA
Frequency Adjust Voltage	Figure 10, f_{IF} = 455 kHz	16	-	600	650	700	mVdc
Bandwidth Adjust Voltage	Figure 12, I_{15} = 1.0 μA	15	-	-	570	-	mVdc
Detector DC Output Voltage (See Figure 25)	-	23	-	-	1.36	-	Vdc
Recovered Audio Voltage	f_{dev} = ±3.0 kHz	23	-	85	122	175	mVrms

* Figure 1 Test Circuit uses positive (V_{CC}) Ground.

Figure 1. Test Circuit



This device contains 292 active transistors.

ML13150 CIRCUIT DESCRIPTION

GENERAL DESCRIPTION

The ML13150 is a very low power single conversion narrowband FM receiver incorporating a split IF. This device can be used as a single conversion or as the backend in analog narrowband FM systems such as 900 MHz cordless phones, and narrowband data links with data rates up to 9.6 k baud. It contains a mixer, oscillator, extended range received signal strength indicator (RSSI), RSSI buffer, IF amplifier, limiting IF, a unique coilless quadrature detector and a device enabler function (see Package Pin Outs/Block Diagram).

LOW CURRENT OPERATION

The ML13150 is designed for battery and portable applications. Supply current is typically 1.7 mAdc at 3.0 Vdc. Figure 2 shows the supply current versus supply voltage.

ENABLE

The enable function is provided for battery powered operation. The enabled pin is pulled down to enable the regulators. Figure 3 shows the supply current versus enable voltage, Venable (relative to VCC) needed to enable the device. Note that the device is fully enabled at VCC - 1.3 Vdc. Figure 4 shows the relationship of the enable current, Ienable, to enable voltage, Venable.

MIXER

The mixer is a double-balanced four quadrant multiplier and is designed to work up to 500 MHz. It has a single ended input. Figure 5 shows the mixer gain and saturated output response as a function of input signal drive and for –10 dBm LO drive level. This is measured in the application circuit shown in Figure 15 in which a single LC matching network is used. Since the single–ended input impedance of the mixer is 200 Ω, and alternate solution uses a 1:4 impedance transformer to match the mixer to 50 Ω input impedance. The linear voltage gain of the mixer alone is approximately 4.0 dB (plus an additional 6.0 dB for the transformer). Figure 6 shows the mixer gain versus the LO input level for various mixer input levels at 50 MHz RF input.

The buffered output of the mixer is internally loaded, resulting in an output impedance of 1.5kΩ.

LOCAL OSCILLATOR

The on–chip transistor operates with crystal and LC resonant elements up to 220 MHz. Series resonant, overtone crystals are used to achieve excellent local oscillator stability. 3rd overtone crystals are used through about 65 to 70 MHz. Operation for 70 MHz up to 200 MHz is feasible using the on–chip transistor with a 5th o 7th overtone crystal. To enhance operation using an overtone crystal, the internal transistor's bias is increased by adding an external resistor from Pin 29 (in 32 pin QF package) to VEE to keep the oscillator on continuously o it may be taken to the enable pin to shut is off when the receiver is disabled. –10 dBm of local oscillator drive is needed to adequately drive the mixer (Figure 6). The oscillator configurations specified above are described in the application section.

RSSI

The received signal strength indicator (RSSI) output is a current proportional to the log of the received signal amplitude. The RSSI current output is derived by summing the currents from the IF and limiting amplifier stages. An external resistor at Pin 25 (in 32 pin QFP package) sets the voltage range or swing of the RSSI output voltage. Linearity of the RSSI is optimized by using external ceramic bandpass filters which have an insertions loss of 4.0 dB. The RSSI circuit is designed to provide 100+ dB of dynamic range with temperature compensation (see Figures 7 and 23 which show the RSS response of the applications circuit).

RSSI BUFFER

The RSSI buffer has limitations in what loads it can drive. It can pull loads well towards the positive and negative supplies, but has problems pulling the load awa from the supplies. The load should be biased at half supply to overcome this situation.

Figure 2. Supply Current versus Supply Voltage

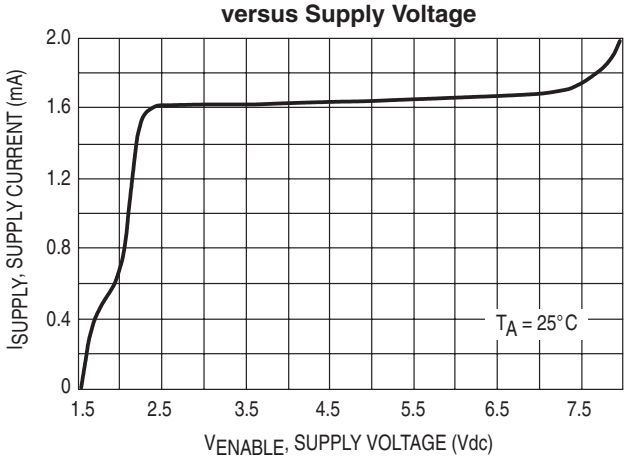


Figure 3. Supply Current versus Enable Voltage

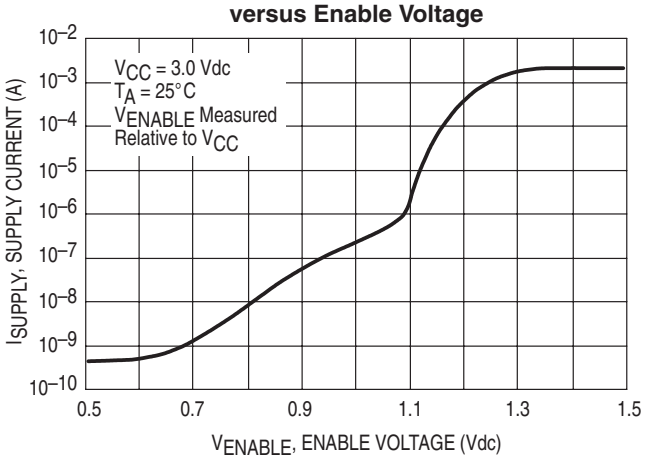


Figure 4. Enable Current versus Enable Voltage

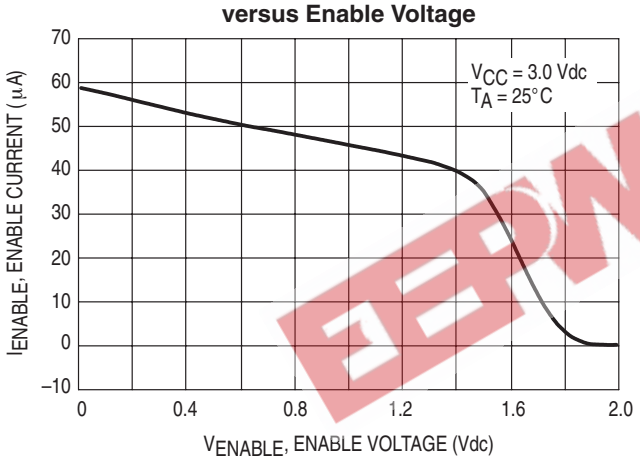


Figure 5. Mixer IF Output Level versus RF Input Level

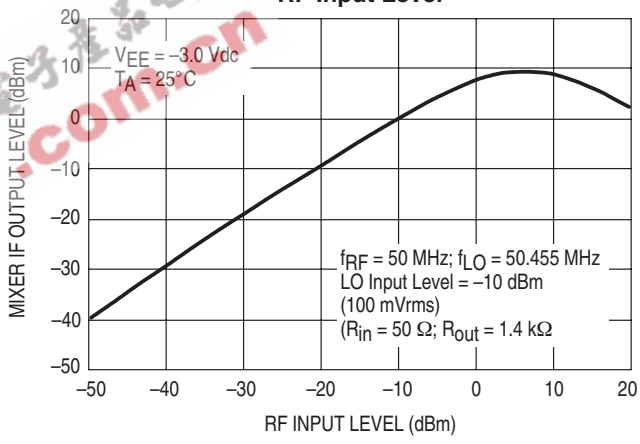


Figure 6. Mixer IF Output Level versus Local Oscillator Input Level

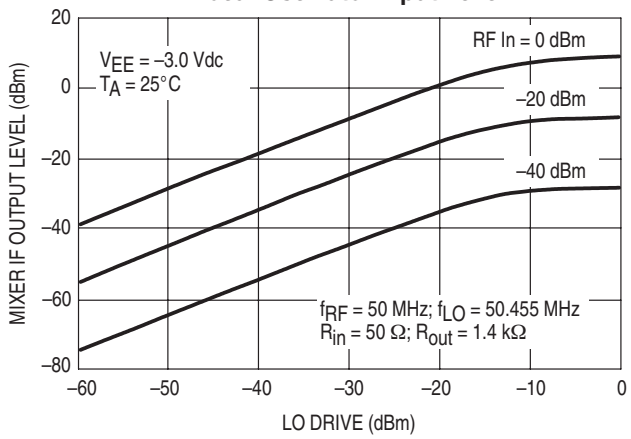
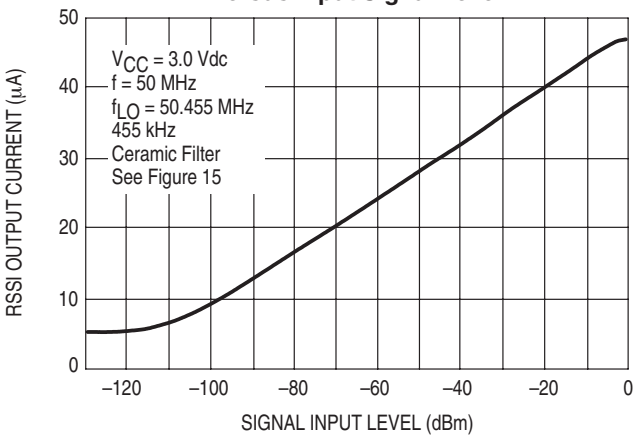


Figure 7. RSSI Output Current versus Input Signal Level



IF AMPLIFIER

The first IF amplifier section is composed of three differential stages. This section has internal dc feedback and external input decoupling for improved symmetry and stability. The total gain of the IF amplifier block is approximately 42 dB at 455 kHz. Figure 8 shows the gain of the IF amplifier as a function of the IF frequency.

The fixed internal input impedance is 1.5 kΩ; it is designed for applications where a 455 kHz ceramic filter is used and no external output matching is necessary since the filter requires a 1.5 kΩ source and load impedance.

Overall RSSI linearity is dependent on having total midban attenuation of 10 dB (4.0 insertion loss plus 6.0 dB impedance matching loss) for the filter. The output of the I amplifier is buffered and the impedance if 1.5kΩ.

LIMITER

The limiter section is similar to the IF amplifier section except that six stages are used. The fixed internal input impedance is 1.5 kΩ. The total gain of the limiting amplifier sections is approximately 96 dB. This IF limitin amplifier section internally drives the quadrature detector section.

Figure 8. IF Amplifier Gain versus IF Frequency

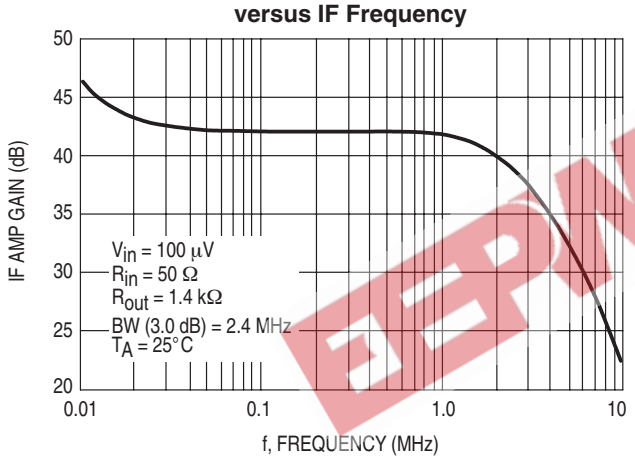


Figure 9. F_{adj} Current versus IF Frequency

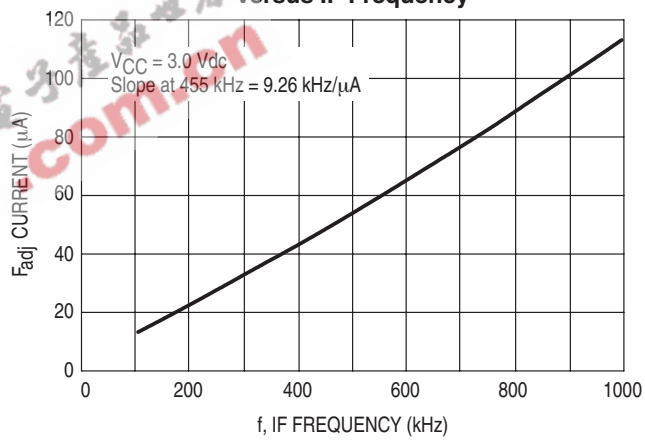


Figure 10. F_{adj} Voltage versus F_{adj} Current

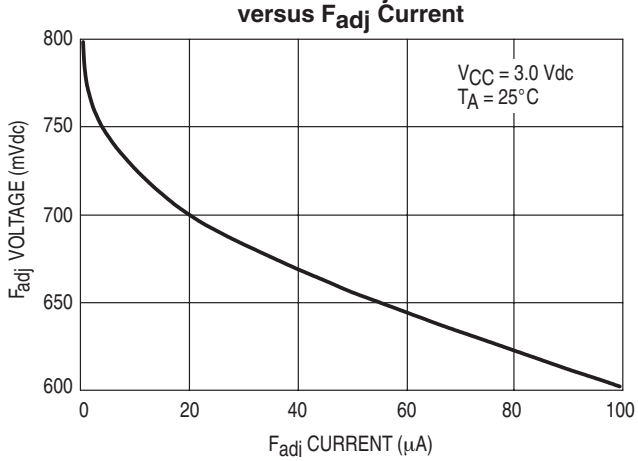
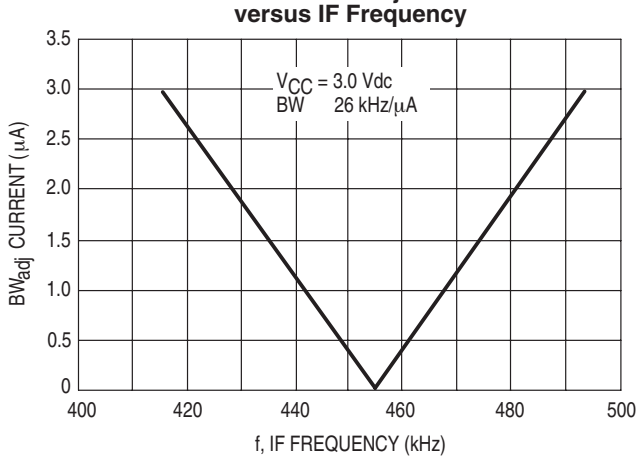


Figure 11. BW_{adj} Current versus IF Frequency



COILLESS DETECTOR

The quadrature detector is similar to a PLL. There is an internal oscillator running at the IF frequency and two detector outputs. One is used to deliver the audio signal and the other one is filtered and used to tune the oscillator.

The oscillator frequency is set by and external resistor at the F_{adj} pin. Figure 9 shows the control current required for a particular frequency; Figure 10 shows the pin voltage at that current. From this the value of RF is chosen. For example, 455 kHz would require a current of around 50 µA. The pin voltage (Pin 16 in the 32 pin QFP package) is around 655mV giving a resistor of 13.1 kΩ. Choosing 12 kΩ as the nearest standard value gives a current of approximately 55 µA. The 5.0 µA difference can be taken up by the tuning resistor, R_T.

The best nominal frequency for the AFTout pin (Pin 17) would be half supply. A supply voltage of 3.0 Vdc suggests a resistor value of (1.5 – 0.655) V/5.0 µA = 169 kΩ. Choosing 150 kΩ would give a tuning current of 3/150 kΩ = 20 µA. From Figure 9 this would give a tuning range of roughly 10 kHz/µA or ± 100 kHz which should be adequate.

The bandwidth can be adjusted with the help of Figure 11.

For example, 1.0 µA would give a band width of ± 13 kHz. The voltage across the bandwidth resistor, RB from Figure 1 is V_{CC} – 2.44 Vdc = 0.56 Vdc for V_{CC} = 3.0 Vdc, so R_B = 0.56V/1.0 µA = 560 kΩ. Actually the locking range will be ±13 kHz while the audio bandwidth wil be approximately ±8.4 kHz due to an internal filter capacitor. This is verified i Figure 13. For some applications it may be desireable that the audio bandwidth is increased; this is done by reducing R_B. Reducing R_B widens the detector bandwidth and improves the distortion at high input levels at the expense of 12 dB SINAD sensitivity. The low frequency 3.0dB point is set by the tuning circuit such that the product

$$RTCT = 0.68/f_{3dB}.$$

So, for example, 150 kΩ and 1.0 µF give a 3.0 dB point o 4.5 kHz. The recovered audio is set by RL to give roughly 50mV per kHz deviation per 100 k of resistance. The dc level can be shifted by R_S from the nominal 0.68 V by the following equation:

$$\text{Detector DC Output} = ((R_L + R_S)/R_S)\ 0.68\ \text{Vdc}$$

Thus $R_S = R_L$ sets the output at 2 x 0.68 = 1.36 V; R_L = $2R_S$ sets the output at 3 x .068 = 2.0V.

Figure 12. BW_{adj} Current versus BW_{adj} Voltage

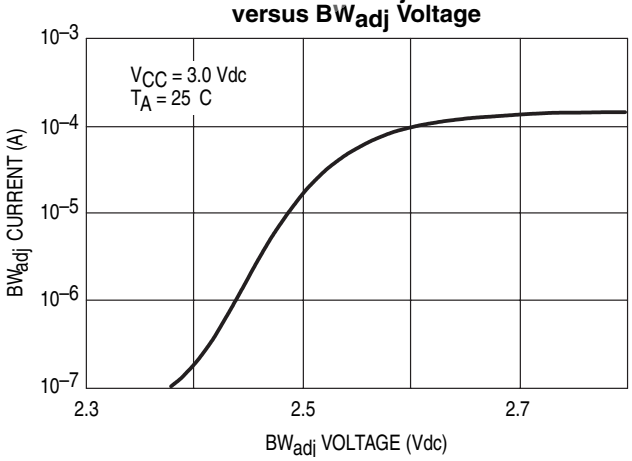
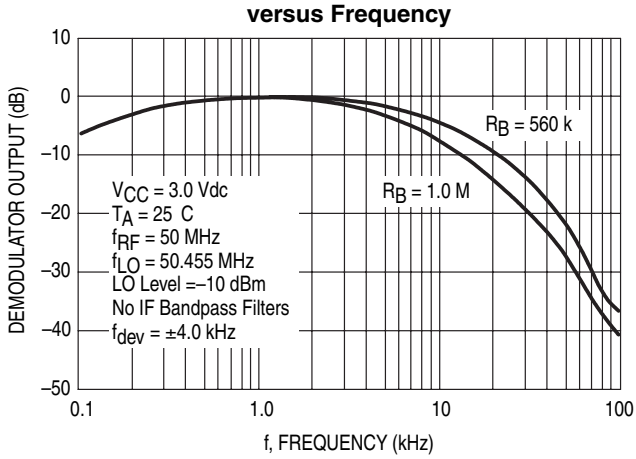


Figure 13. Demodulator Output versus Frequency



Legacy Applications Information

EVALUATION PC BOARD

The evaluation PCB is very versatile and is intended to be used across the entire useful frequency range of this device. The center section of the board provides an area for attaching all SMT components to the circuit side and radial leaded components to the component ground side (see Figures 29 and 30). Additionally, the peripheral area surrounding the RF core provides pads to add supporting and interface circuitry as a particular application requires. There is an area dedicated for a LNA preamp. This evaluation board will be discussed and referenced in this section.

COMPONENT SELECTION

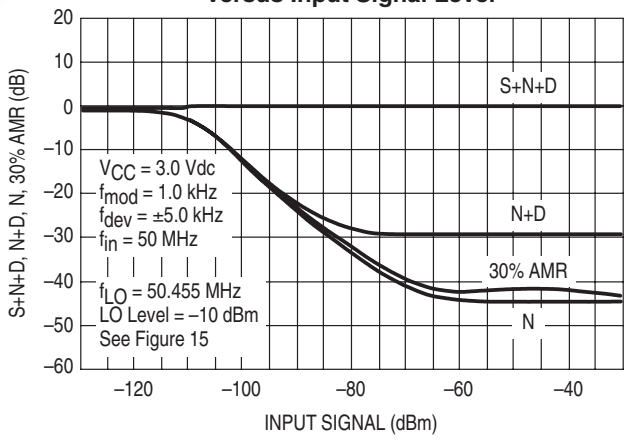
The evaluation PC board is designed to accommodate specific components, while also being versatile enough to use components from various manufacturers and coil types. The applications circuit schematic (Figure 15) specifies particular components that were used to achieve the results shown in the typical curves but equivalent components should give similar results. Component placement views are shown in Figures 27 and 28 for the application circuit in Figure 15 and for the 83.616 MHz crystal oscillator circuit in Figure 16.

INPUT MATCHING COMPONENTS

The input matching circuit shown in the application circuit schematic (Figure 15) is a series L, shunt C single L section which is used to match the mixer input to 50 Ω. An alternative input network may use 1:4 surface mount transformers o BALUNs. The 12 dB SINAD sensitivity using the 1:4 imped ance transformer is typically –100 dBm for f_{mod} = 1.0 kHz and f_{dev} = ±5.0 kHz at f_{in} = 50 MHz and f_{LO} = 50.455 MHz (see Figure 14).

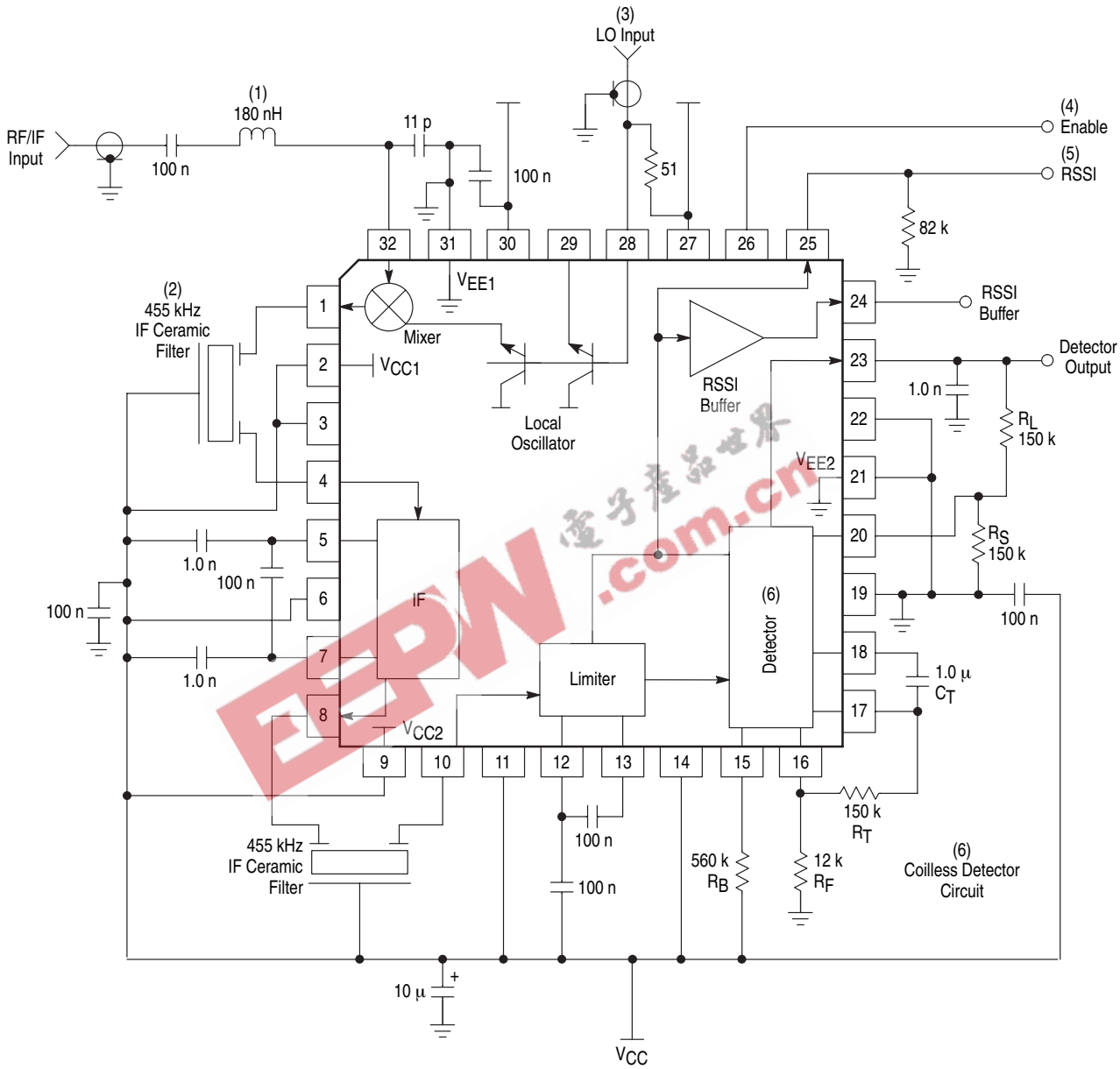
It is desirable to use a SAW filter before the mixer to provide additional selectivity an adjacent channel rejection and improved sensitivity. SAW filters sourced from Toko (Part #SWS083GBWA) and Murata (Part # SAF83.16MA51X) ar excellent choices to easily interface with the MC13150 mixe They are packaged in a 12 pin low profile surface mount ceramic package. The center frequency is 83.161 MHz and the 3.0 dB bandwidth is 30 kHz.

Figure 14. S+N+D, N+D, N, 30% AMR versus Input Signal Level



Legacy Applications Information

Figure 15. Application Circuit



NOTES: 1. Alternate solution is 1:4 impedance transformer (sources include Mini Circuits, Coilcraft and Toko).
2. 455 kHz ceramic filters (source Murata CFU455 series which are selected for various bandwidths).
3. For external LO source, a 51 Ω pullup resistor is used to bias the base of the on–board transistor as shown in Figure 15. Designer may provide local oscillator with 3rd, 5th, or 7th overtone crystal oscillator circuit. The PC board is laid out to accommodate external components needed for a Butler emitter coupled crystal oscillator (see Figure 16).
4. Enable IC by switching the pin to V_{EE}.
5. The resistor is chosen to set the range of RSSI voltage output swing.
6. Details regarding the external components to setup the coilless detector are provided in the application section.

Legacy Applications Information

LOCAL OSCILLATORS

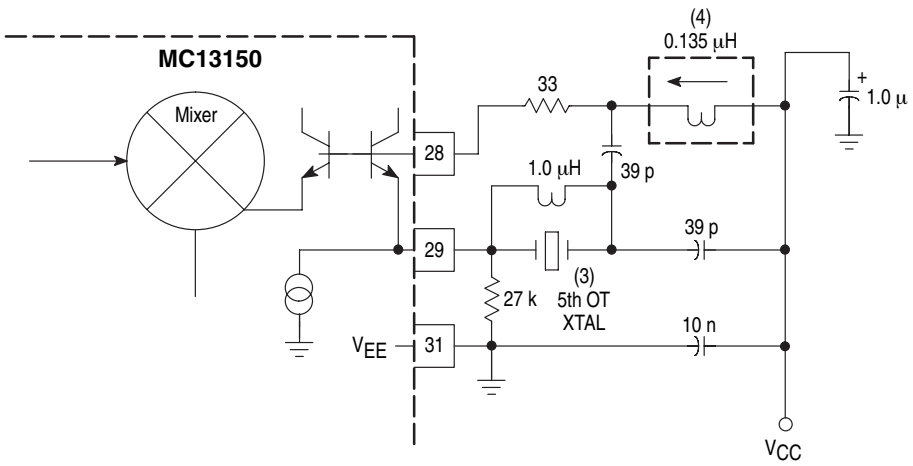
HF & VHF APPLICATIONS

In the application schematic, an external sourced local oscillator is utilized in which the base is biased via a 51 Ω resistor to V_{CC}. However, the on–chip grounded collector transistor may be used for HF and VHF local oscillators with higher order overtone crystals. Figure 16 shows a 5th overtone oscillator at 83.616 MHz. The circuit uses a Butler overtone oscillator configuration. The amplifier is an emitter follower. The crystal is driven from the emitter and is coupled to the high impedance base through a capacitive tap network. Operation at the desired overtone frequency is ensured by the parallel resonant circuit formed by the variable inductor and the tap capacitors and parasitic capacitances of the on–chip transistor and PC board. The variable inductor specified in the schematic could be replaced with a high tolerance, high Q ceramic or air wound surface mount component if the other components have tight enough tolerance. A variable inductor provides an adjustment for gain and frequency of the resonant tank ensuring lock up and start–up of the crystal oscillator. The overtone crystal is chosen with ESR of typically 80 Ω and 120 Ω maximum; if the resistive loss in the crystal is too high the performance of oscillator may be impacted by lower gain margins.

A series LC network to ac ground (which is V_{CC}) is comprised of the inductance of the base lead of on–chip transisto and PC board traces and tap capacitors. Parasitic oscillations often occur in the 200 to 800 MHz range. A small resistor is placed in series with the base (Pin 28) to cancel the negative resistance associated with this undesired mode of oscillation. Since the base input impedance is so large, a small resistor in the range of 27 to 68 Ω has very little effect on the desired Butler mode of oscillation.

The crystal parallel capacitance, C_O, provides a feedback pat that is low enough in reactance at frequencies of 5th overtones or higher to cause trouble. C_O has little effect near reso nance because of the low impedance of the crystal motional arm (Rm-Lm-Cm). As the tunable inductor, which forms the resonant tank with the tap capacitors, is tuned off the crystal resonant frequency, it may be difficult to tell if the oscillation is under crystal control. Frequency jumps may occur as the inductor is tuned. In order to eliminate this behavior an induc tor, L_O, is placed in parallel with the crystal. L_O is chosen to resonant with the crystal parallel capacitance, C_O, at the desired operation frequency. This inductor provides a feedback path at frequencies well below resonance; however, the parallel tank network of the tap capacitors and tunable inductor prevent oscillation at these frequencies.

Figure 16. ML13150 Overtone Oscillator
f_{RF} = 83.16 MHz; f_{LO} = 83.616 MHz
5th Overtone Crystal Oscillator



RECEIVER DESIGN CONSIDERATIONS

The curves of signal levels at various portions of the application receiver with respect to RF input level are shown in Figure 17. This information helps determine the network topology and gain blocks required ahead of the ML13150 to achieve the desired sensitivity and dynamic range of the receiver system. The PCB is laid out to accommodate a low noise preamp followed by the 83.16 MHz SAW filter. In the application circuit (Figure 15), the input 1.0 dB compression point is –10 dBm and the input third order intercept (IP3) performance of the system is approximately 0 dBm (see Figure 18).

TYPICAL PERFORMANCE OVER TEMPERATURE

Figures 19–26 show the device performance over temperature.

Figure 17. Signal Levels versus RF Input Signal Level

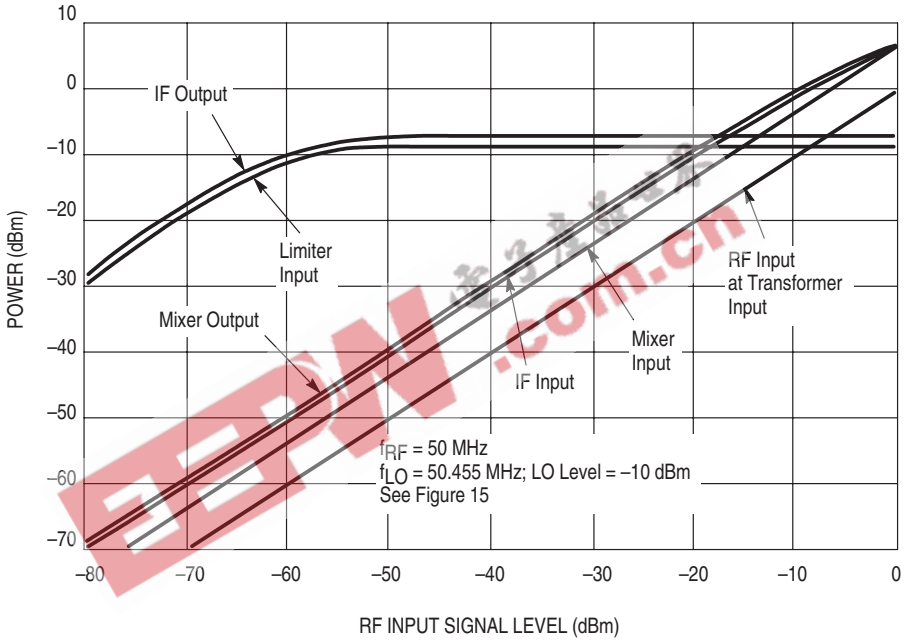
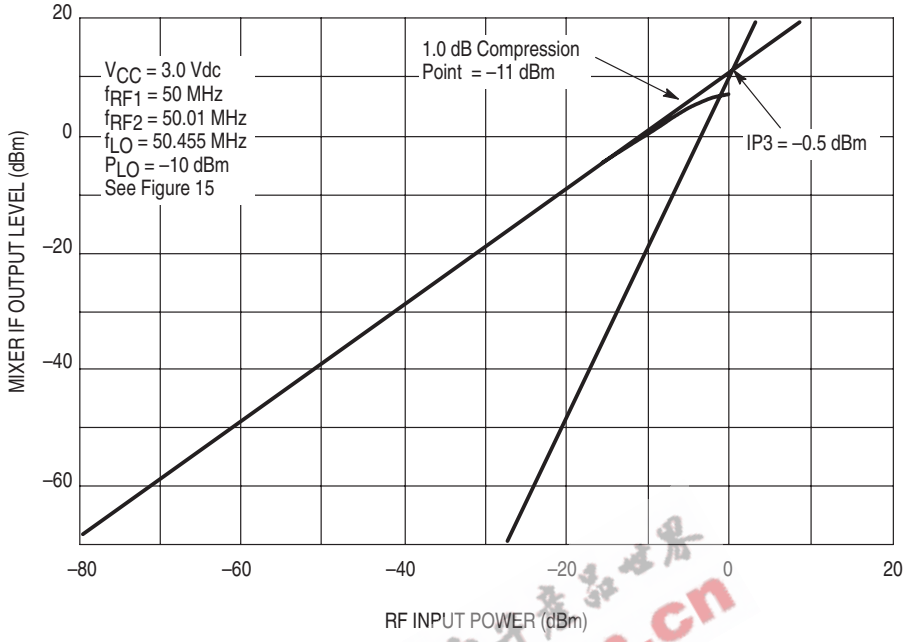


Figure 18. 1.0 dB Compression Point and Input Third Order Intercept Point versus Input Power



TYPICAL PERFORMANCE OVER TEMPERATURE

Figure 19. Supply Current, I_{VEE1} versus Signal Input Level

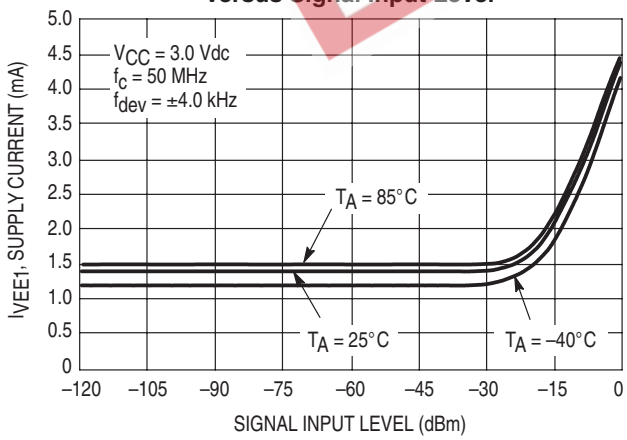
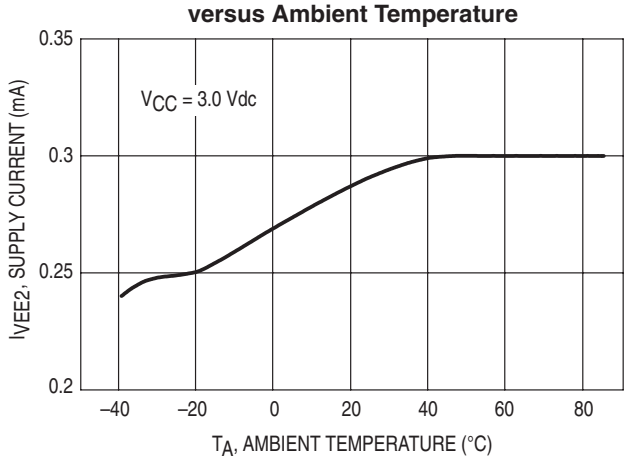


Figure 20. Supply Current, I_{VEE2} versus Ambient Temperature



TYPICAL PERFORMANCE OVER TEMPERATURE

Figure 21. Total Supply Current versus Ambient Temperature

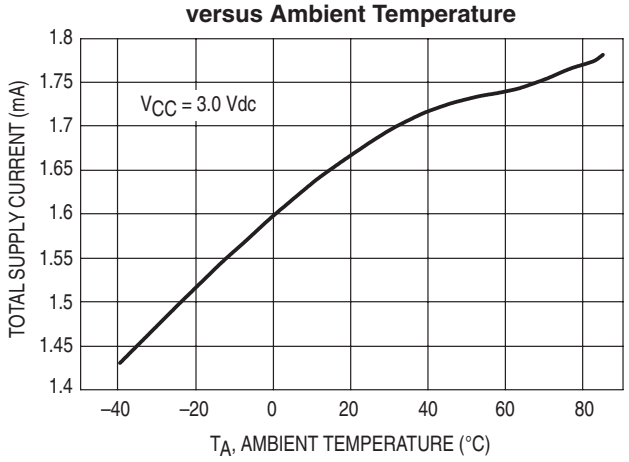


Figure 22. Minimum Supply Voltage versus Ambient Temperature

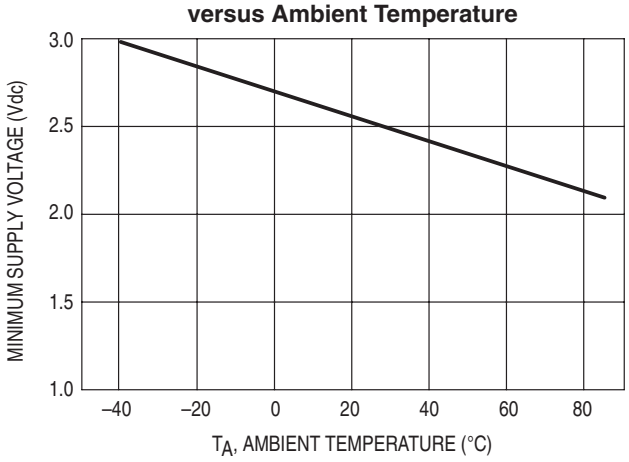


Figure 23. RSSI Current versus Ambient Temperature and Signal Level

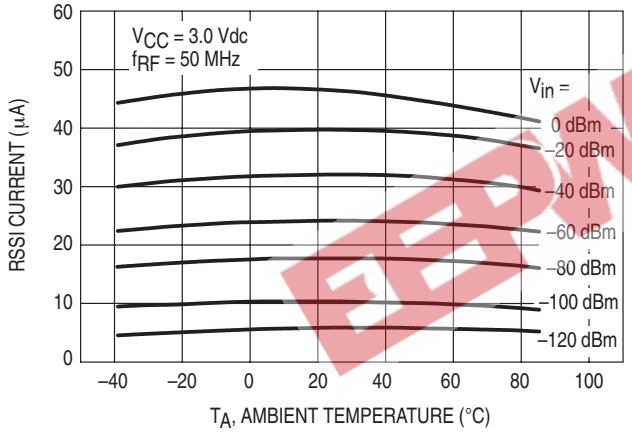


Figure 24. Recovered Audio versus Ambient Temperature

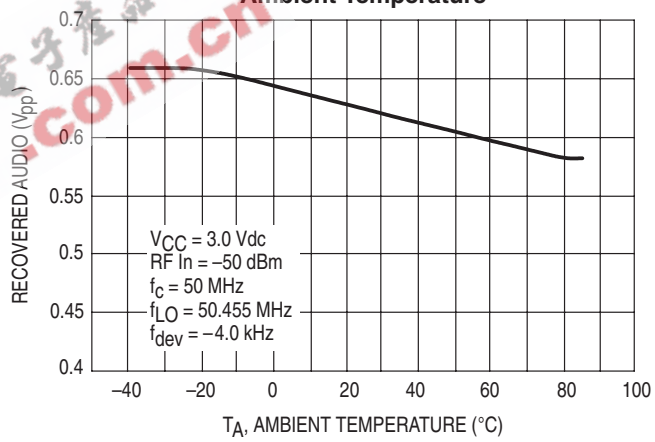


Figure 25. Demod DC Output Voltage versus Ambient Temperature

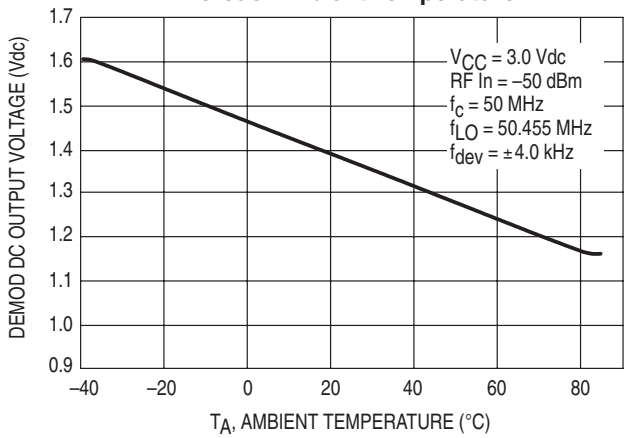
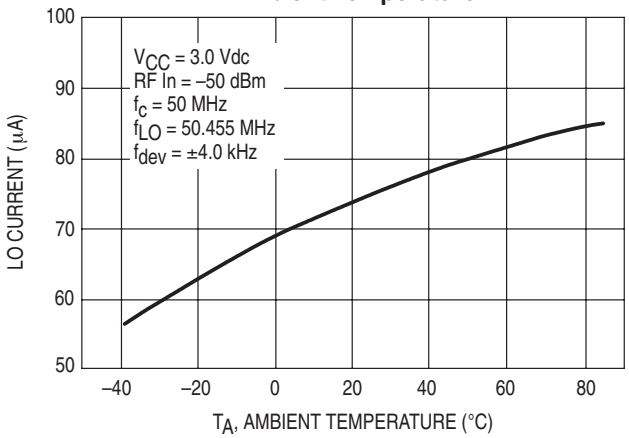
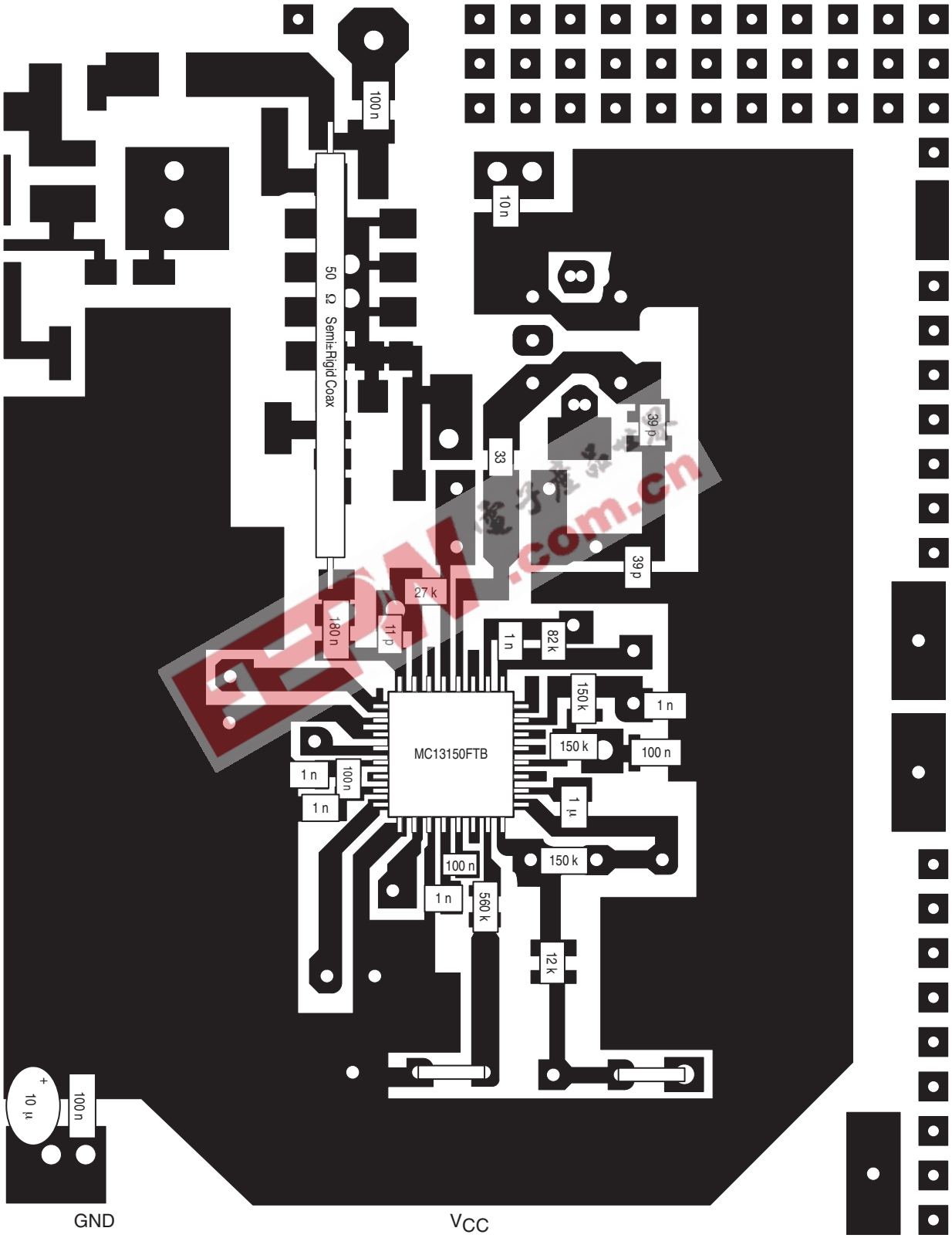


Figure 26. LO Current versus Ambient Temperature



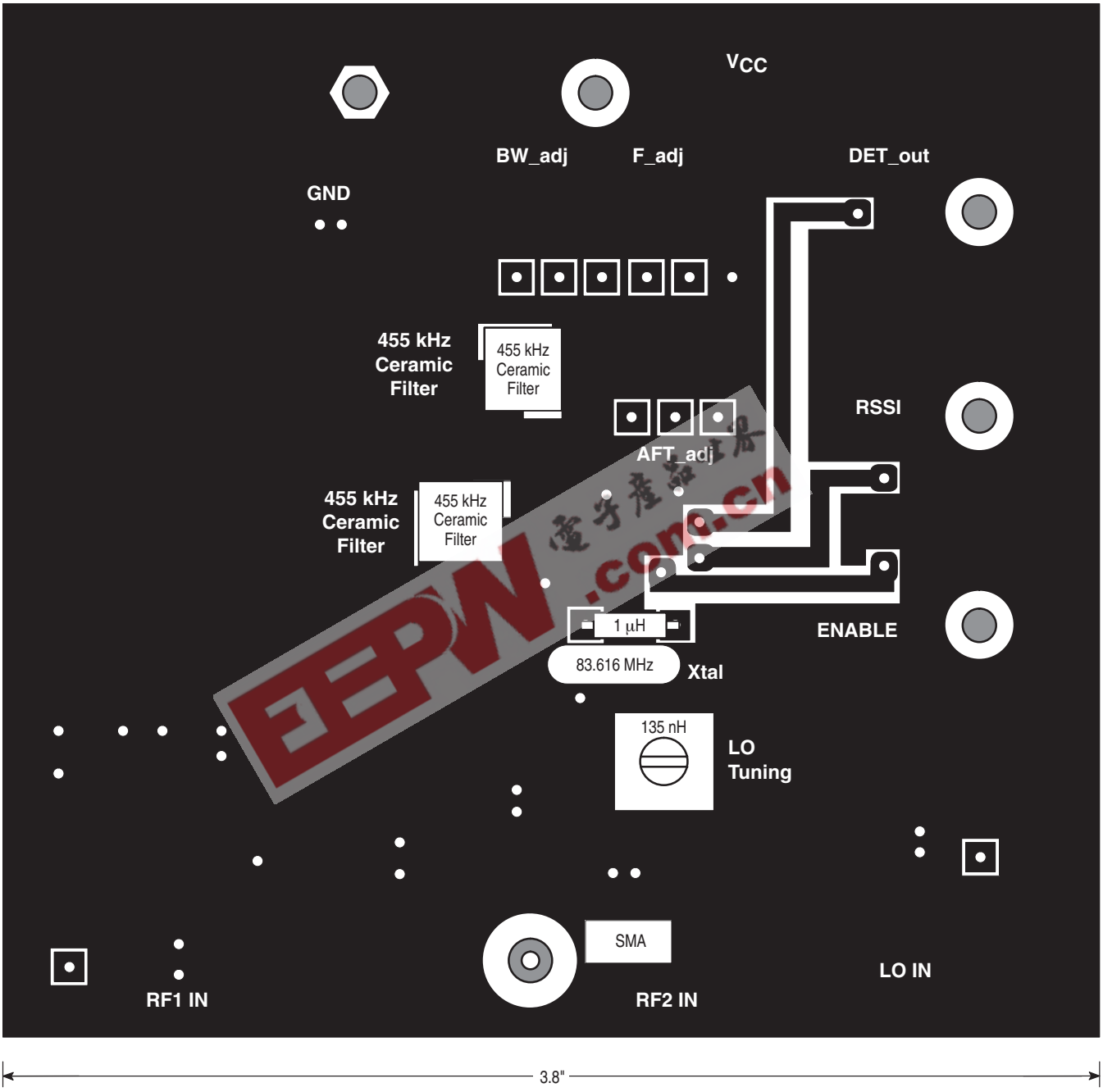
Legacy Applications Information

Figure 27. Component Placement View – Circuit Side



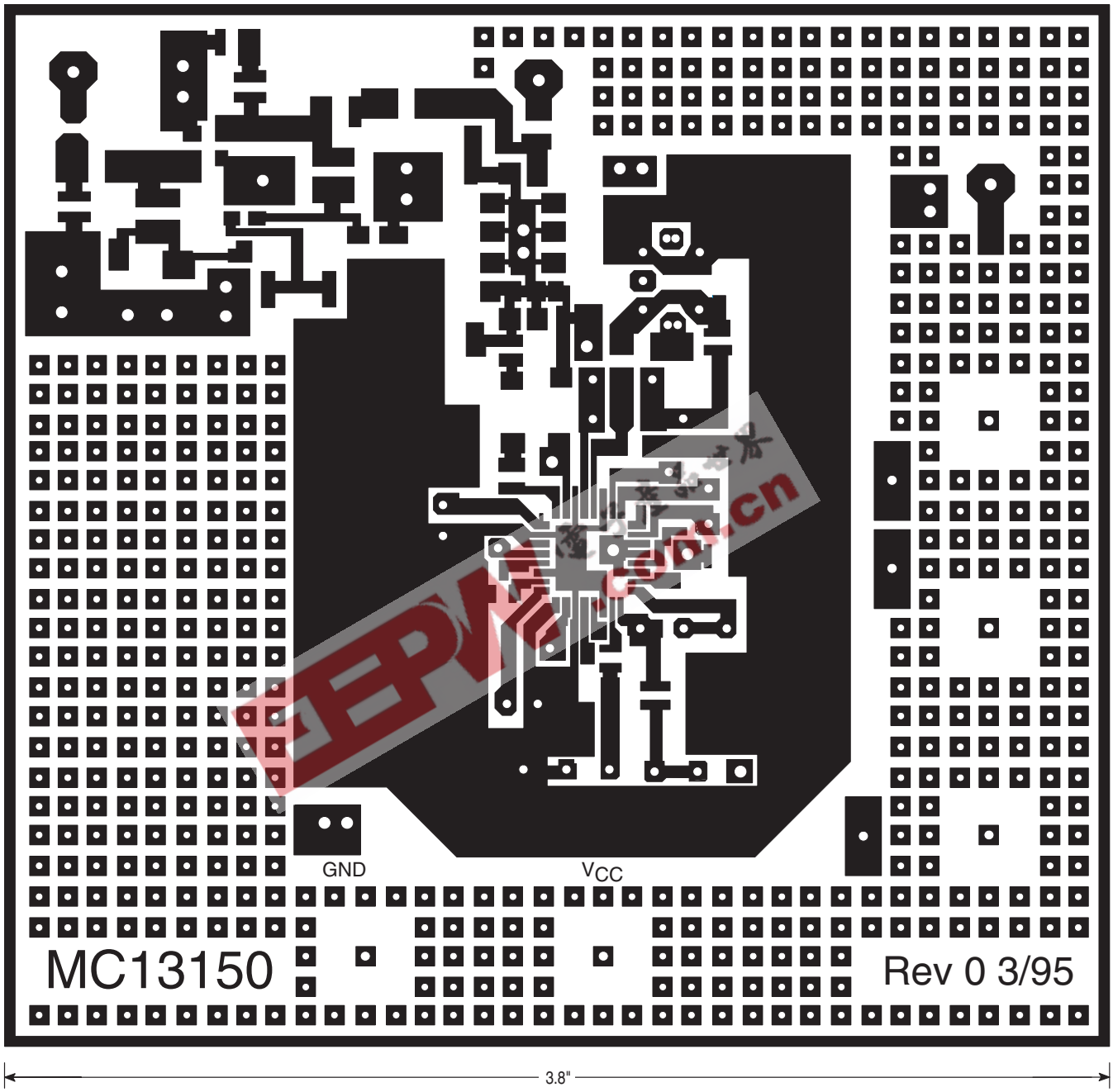
Legacy Applications Information

Figure 28. Component Placement View – Ground Side



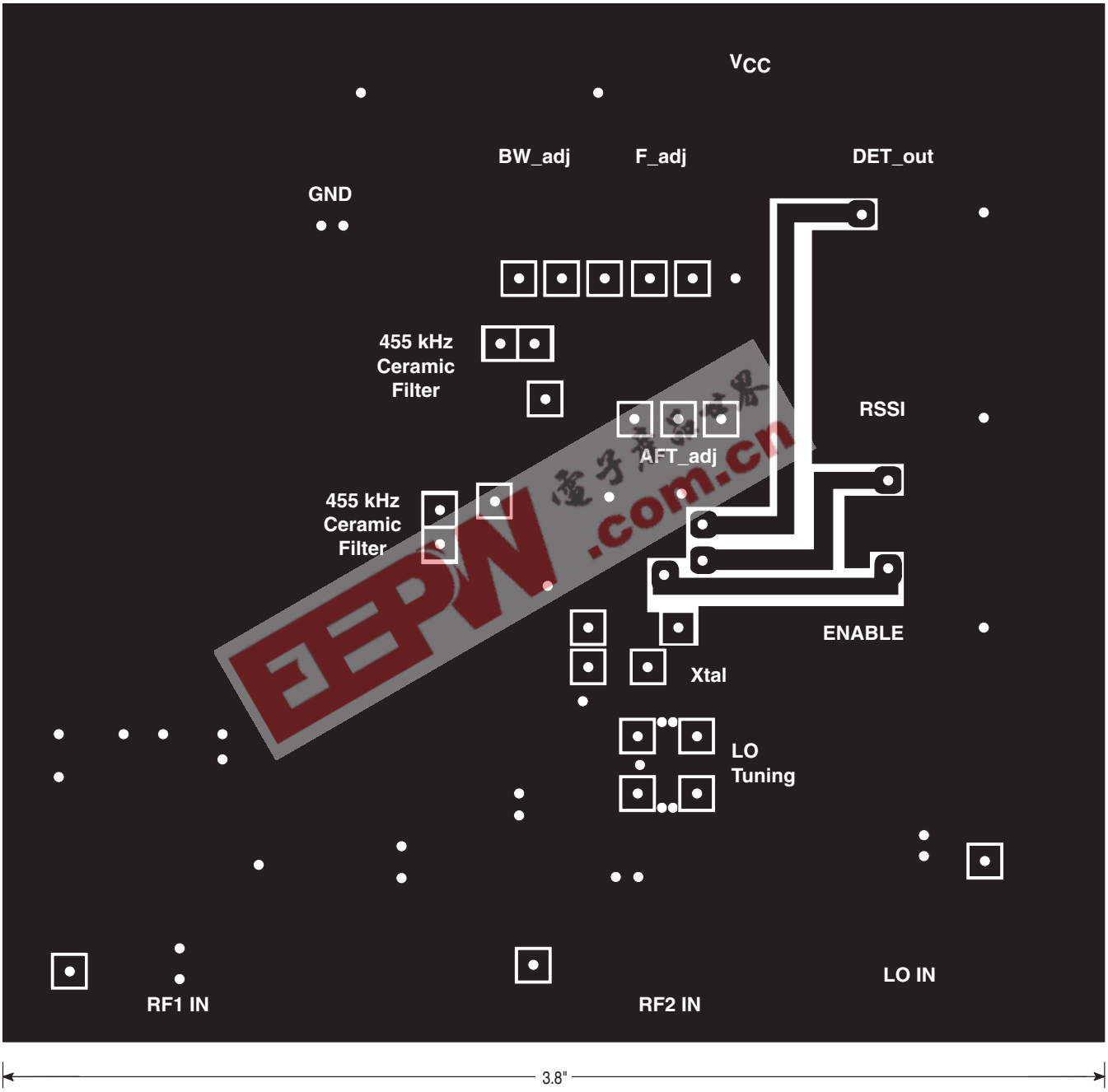
Legacy Applications Information

Figure 29. PCB Circuit Side View



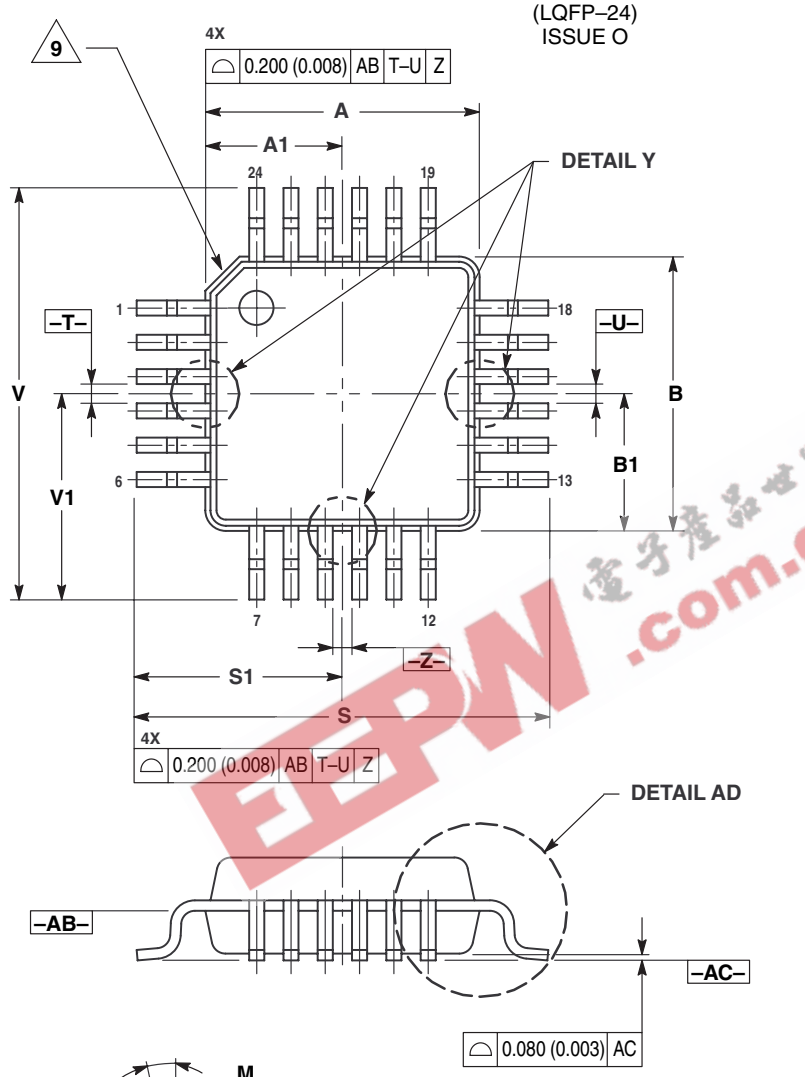
Legacy Applications Information

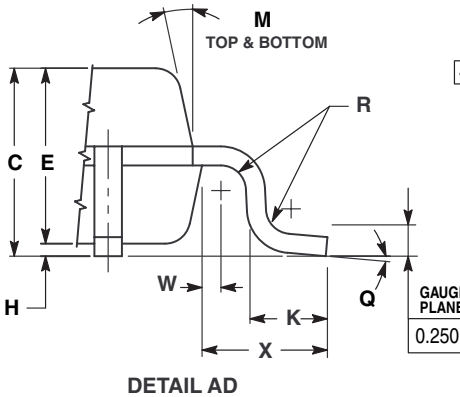
Figure 30. PCB Ground Side View

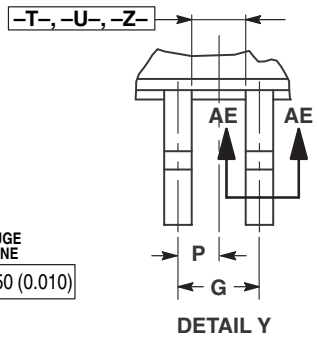


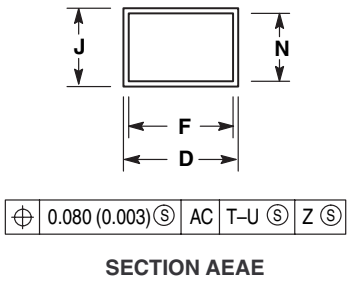
OUTLINE DIMENSIONS

ML13150-A9P
PLASTIC PACKAGE
CASE 977–01
(LQFP–24)
ISSUE O







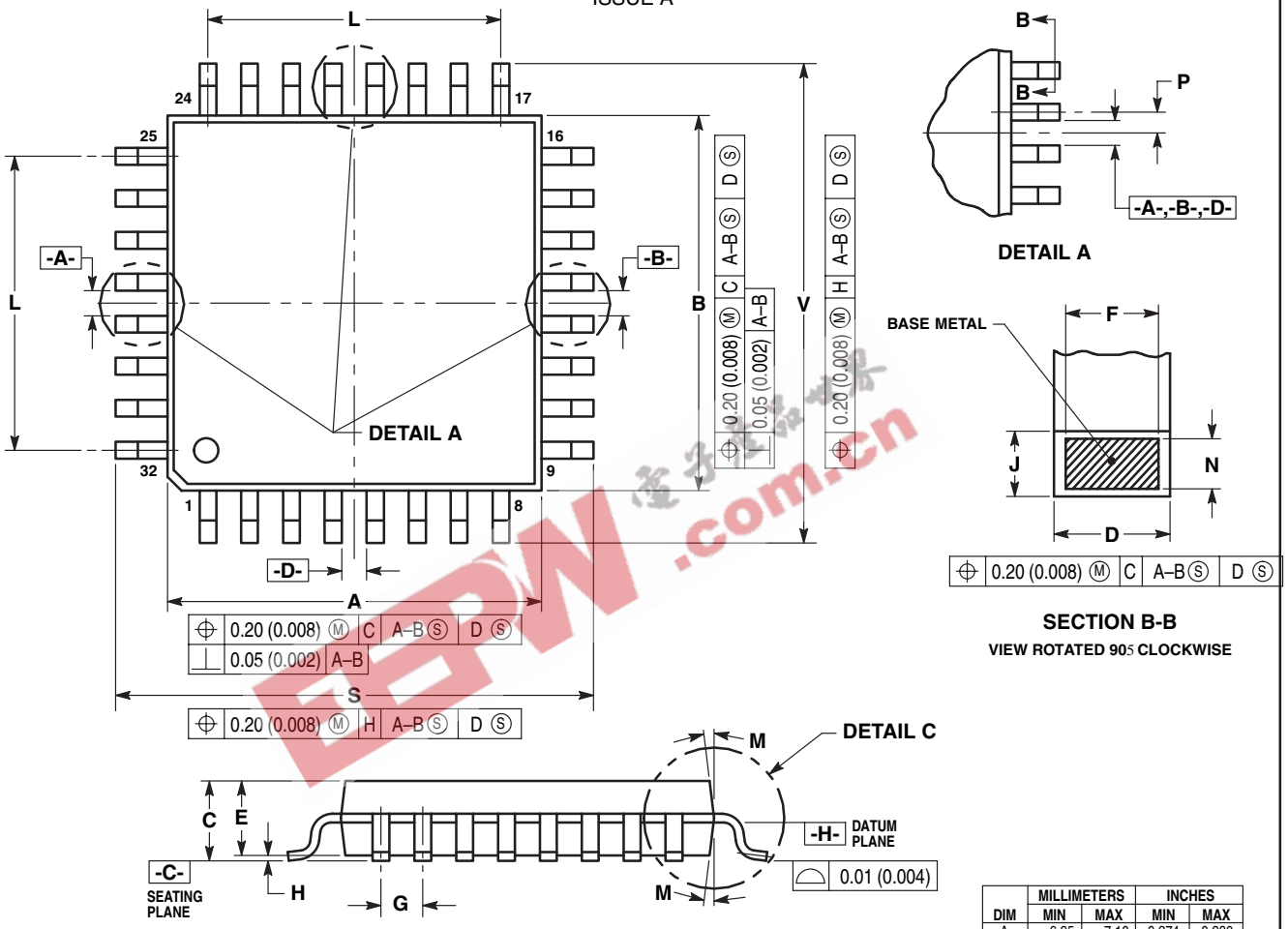


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT DATUM PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350 (0.014).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.000 BSC		0.157 BSC	
A1	2.000 BSC		0.079 BSC	
B	4.000 BSC		0.157 BSC	
B1	2.000 BSC		0.079 BSC	
C	1.400	1.600	0.055	0.063
D	0.170	0.270	0.007	0.011
E	1.350	1.450	0.053	0.057
F	0.170	0.230	0.007	0.009
G	0.500 BSC		0.020 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12 REF		12 REF	
N	0.090	0.160	0.004	0.006
P	0.250 BSC		0.010 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	6.000 BSC		0.236 BSC	
S1	3.000 BSC		0.118 BSC	
V	6.000 BSC		0.236 BSC	
V1	3.000 BSC		0.118 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

OUTLINE DIMENSIONS

ML13150-B9P
PLASTIC PACKAGE
CASE 873–01
(LQFP–32)
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.95	7.10	0.274	0.280
B	6.95	7.10	0.274	0.280
C	1.40	1.60	0.055	0.063
D	0.273	0.373	0.010	0.015
E	1.30	1.50	0.051	0.059
F	0.273	–	0.010	–
G	0.80 BSC		0.031 BSC	
H	–	0.20	–	0.008
J	0.119	0.197	0.005	0.008
K	0.33	0.57	0.013	0.022
L	5.6 REF		0.220 REF	
M	6°	8°	6°	8°
N	0.119	0.135	0.005	0.005
P	0.40 BSC		0.016 BSC	
Q	5°	10°	5°	10°
R	0.15	0.25	0.006	0.010
S	8.85	9.15	0.348	0.360
T	0.15	0.25	0.006	0.010
U	5°	11°	5°	11°
V	8.85	9.15	0.348	0.360
X	1.0 REF		0.039 REF	