HEWLETT® PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-1100

Features

- **High Dynamic Range Cascadable 50 Ω or 75 Ω Gain Block**
- **3 dB Bandwidth:** 50 MHz to 1.6 GHz
- **17.5 dBm Typical $P_{1 dB}$ at 0.5 GHz**
- **12 dB Typical 50 Ω Gain at 0.5 GHz**
- **3.5 dB Typical Noise Figure at 0.5 GHz**

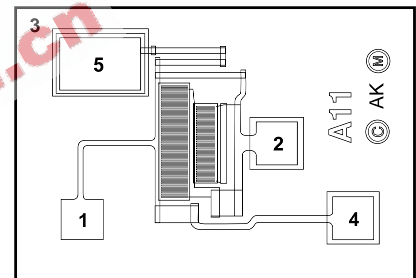
Description

The MSA-1100 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) chip. This MMIC is designed for high dynamic range in either 50 or 75 Ω systems by combining low noise figure with high IP_3. Typical applications include narrow and broadband linear amplifiers in industrial and military systems.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire.

Chip Outline[1]

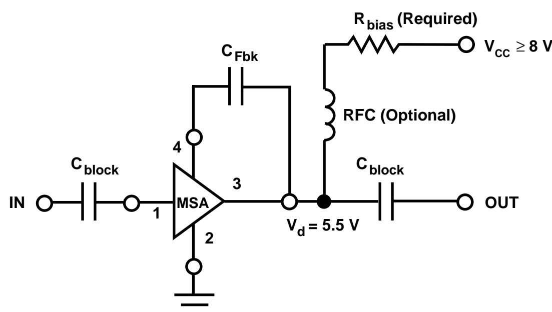


This chip is intended to be used with an external blocking capacitor completing the shunt feedback path (closed loop). Data sheet characterization is given for a 200 pF capacitor. Low frequency performance can be extended by using a larger valued capacitor.[1]

Note:

1. Refer to the APPLICATIONS section "Silicon MMIC Chip Use" for additional information.

Typical Biasing Configuration



MSA-1100 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	100 mA
Power Dissipation[2,3]	650 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,4]:
θ_{jc}[2] = 57°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{Mounting\ Surface}$ (T_{MS}) = 25°C.
3. Derate at 17.5 mW/°C for $T_{Mounting\ Surface}$ > 163°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions[2]: I_d = 60 mA, Z_o = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		12.5	
ΔG_P	Gain Flatness	f = 0.1 to 1.0 GHz	dB		±0.7	
$f_{3\ dB}$	3 dB Bandwidth[3]		GHz		1.6	
VSWR	Input VSWR	f = 0.1 to 1.0 GHz			1.7:1	
	Output VSWR	f = 0.1 to 1.0 GHz			1.9:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		3.5	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm		17.5	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		30.0	
t_D	Group Delay	f = 0.5 GHz	psec		125	
V_d	Device Voltage		V	4.5	5.5	6.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes:
1. The recommended operating current range for this device is 40 to 75 mA. Typical performance as a function of current is on the following page.
2. RF performance of the chip is determined by packaging and testing 10 devices per wafer.
3. Referenced from 0.05 GHz gain (G_P).

Part Number Ordering Information

Part Number	Devices Per Tray
MSA-1100-GP4	100

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MSA-1100 Typical Scattering Parameters[1,2] ($T_A = 25°C$, $I_d = 60$ mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		k
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	
0.001	.72	–26	19.3	9.23	168	–23.4	.067	46	.72	–27	.52
0.005	.19	–73	14.1	5.09	165	–16.7	.147	11	.19	–77	.96
0.010	.16	–69	13.9	4.97	168	–16.6	.148	9	.16	–79	.99
0.050	.04	–59	12.8	4.39	175	–16.0	.159	3	.04	–102	1.06
0.100	.05	–66	12.8	4.38	175	–16.0	.158	2	.05	–100	1.06
0.200	.07	–78	12.8	4.36	170	–15.9	.161	4	.08	–100	1.05
0.400	.14	–92	12.7	4.31	162	–15.6	.165	7	.14	–105	1.01
0.600	.19	–102	12.5	4.22	153	–15.3	.171	10	.21	–111	.96
0.800	.25	–110	12.3	4.11	144	–14.9	.180	13	.27	–116	.90
1.000	.31	–117	12.0	4.00	137	–14.4	.190	14	.33	–122	.83
1.500	.40	–132	10.9	3.52	117	–13.4	.214	15	.42	–136	.70
2.000	.47	–145	9.6	3.01	100	–12.6	.235	14	.46	–148	.64
2.500	.50	–150	8.3	2.60	89	–12.0	.251	16	.45	–152	.63
3.000	.52	–158	7.0	2.23	77	–11.6	.263	17	.42	–156	.66
3.500	.51	–164	5.7	1.92	68	–11.1	.278	19	.38	–155	.73
4.000	.50	–169	4.6	1.70	61	–10.5	.297	22	.34	–152	.79

Notes:

1. S-parameters are de-embedded from 200 mil BeO package measured data using the package model found in the DEVICE MODELS section.
2. S-parameter data assumes an external 200 pF capacitor. Low frequency performance can be extended using a larger valued capacitor.

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Typical Performance, $T_A = 25°C$

(Unless otherwise noted, performance is for a MSA-1100 used with an external 200 pF capacitor. See bonding diagram.)

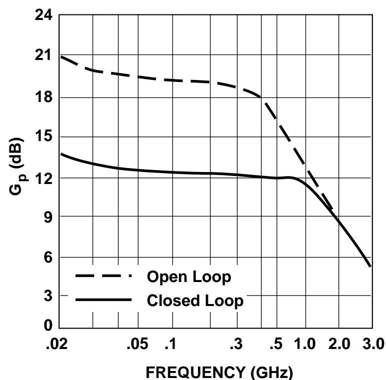


Figure 1. Typical Power Gain vs. Frequency, I_d = 60 mA.

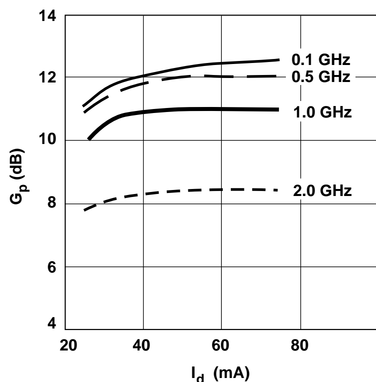


Figure 2. Power Gain vs. Current.

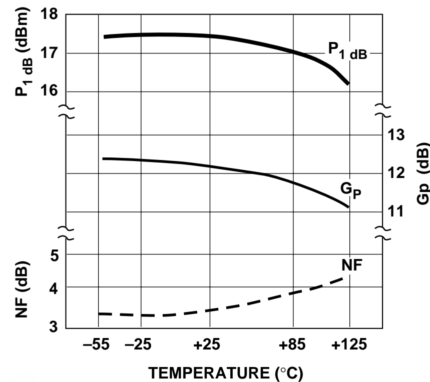


Figure 3. Output Power at 1 dB Gain Compression, Noise Figure and Power Gain vs. Case Temperature, f = 0.5 GHz, I_d = 60 mA.

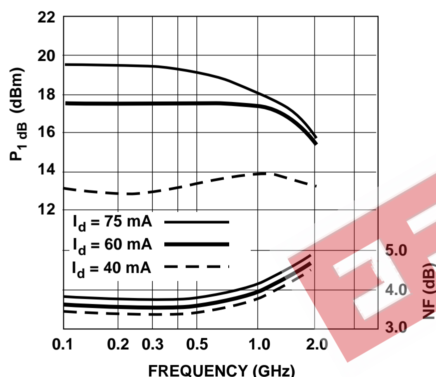
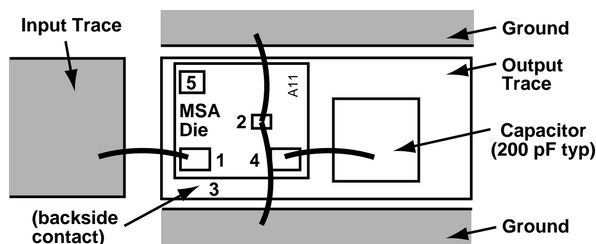


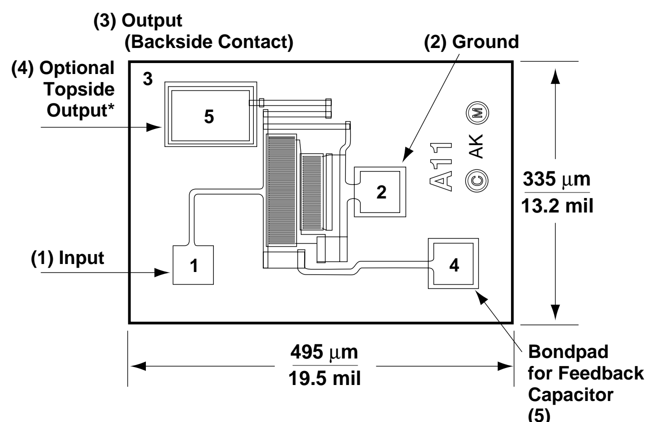
Figure 4. Output Power at 1 dB Gain Compression and Noise Figure vs. Frequency.

MSA-1100 Bonding Diagram



Numbers refer to pin contacts listed on the Chip Outline.

MSA-1100 Chip Dimensions



Unless otherwise specified, tolerances are ±13 µm/±0.5 mils.
Chip thickness is 114 µm/4.5 mil. Bond Pads are 41 µm/1.6 mil typical on each side.
*** Output contact is made by die attaching the backside of the die.**

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