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4Mb Ultra-Low Power Asynchronous CMOS SRAM w/ Dual Vcc and VccQ for Ultimate Power Reduction

256K×16 bit POWER SAVER TECHNOLOGY

Overview

The N04Q16yyC2B are ultra-low power memory devices containing a 4 Mbit Static Random Access Memory organized as 262,144 words by 16 bits. The device is designed and fabricated using NanoAmp's advanced CMOS technology to provide ultra-low active and standby power. The device operates with two chip enable ($\overline{CE1}$ and CE2) controls and output enable ($\overline{OE}$) to allow for easy memory expansion. Byte controls ($\overline{UB}$ and $\overline{LB}$) allow the upper and lower bytes to be accessed independently. The 4Mb SRAM is optimized for the ultimate in low power and is suited for various applications where ultra-low-power is critical such as medical applications, battery backup and power sensitive hand-held devices. The unique page mode operation saves active operating power and the dual power supply rails allow very low voltage operation while maintaining 3V I/O capability. The device can operate over a very wide temperature range of $0^{o}C$ to $+70^{o}C$ for the lowest power and is also available in the industrial range of $-40^{o}C$ to $+85^{o}C$. The devices are available in standard BGA and TSOP packages. The devices are also available as Known Good Die (KGD) for embedded package applications.

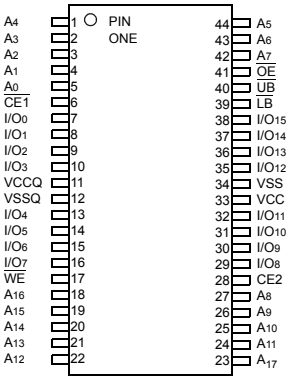
Features

- **Multiple Power Supply Ranges**
  1.1V - 1.3V
  1.65V - 1.95V
  2.3V - 2.7V
  2.7V - 3.6V
- **Dual Vcc / VccQ Power Supplies**
  1.2V Vcc with 3V VccQ
  1.8V Vcc with 3V VccQ
  2.5V Vcc with 3V VccQ
- **Very low standby current**
  50nA typical for 1.2V operation
- **Very low operating current**
  400µA typical for 1.2V operation at 1µs
- **Very low Page Mode operating current**
  80µA typical for 1.2V operation at 1µs
- **Simple memory control**
  Dual Chip Enables ($\overline{CE1}$ and CE2)
  Byte control for independent byte operation
  Output Enable ($\overline{OE}$) for memory expansion
- **Automatic power down to standby mode**
- **BGA, TSOP and KGD options**
- **RoHS Compliant**

Product Options

Part Number	I/O	Typical Standby Current	Vcc (V)	VccQ (V)	Speed (nS)	Typical Operating Current	Operating Temperature
N04Q1612C2Bx-15C	x16	50nA	1.2	1.2, 1.8, 3	150ns	0.4 mA @ 1MHz	$0^{o}C$ to $+70^{o}C$
N04Q1618C2Bx-15C	x16	50nA	1.8	1.8, 2.5, 3	150ns	0.4 mA @ 1MHz	
N04Q1618C2Bx-70C	x16	200nA			70ns	0.6 mA @ 1MHz	
N04Q1625C2Bx-15C	x16	800nA	2.5	2.5, 3	150ns	0.6 mA @ 1MHz	
N04Q1630C2Bx-70C	x16	800nA	3.0	3.0	70ns	2.2mA @ 1MHz	

Pin Configurations (4Mb)



TSOP II

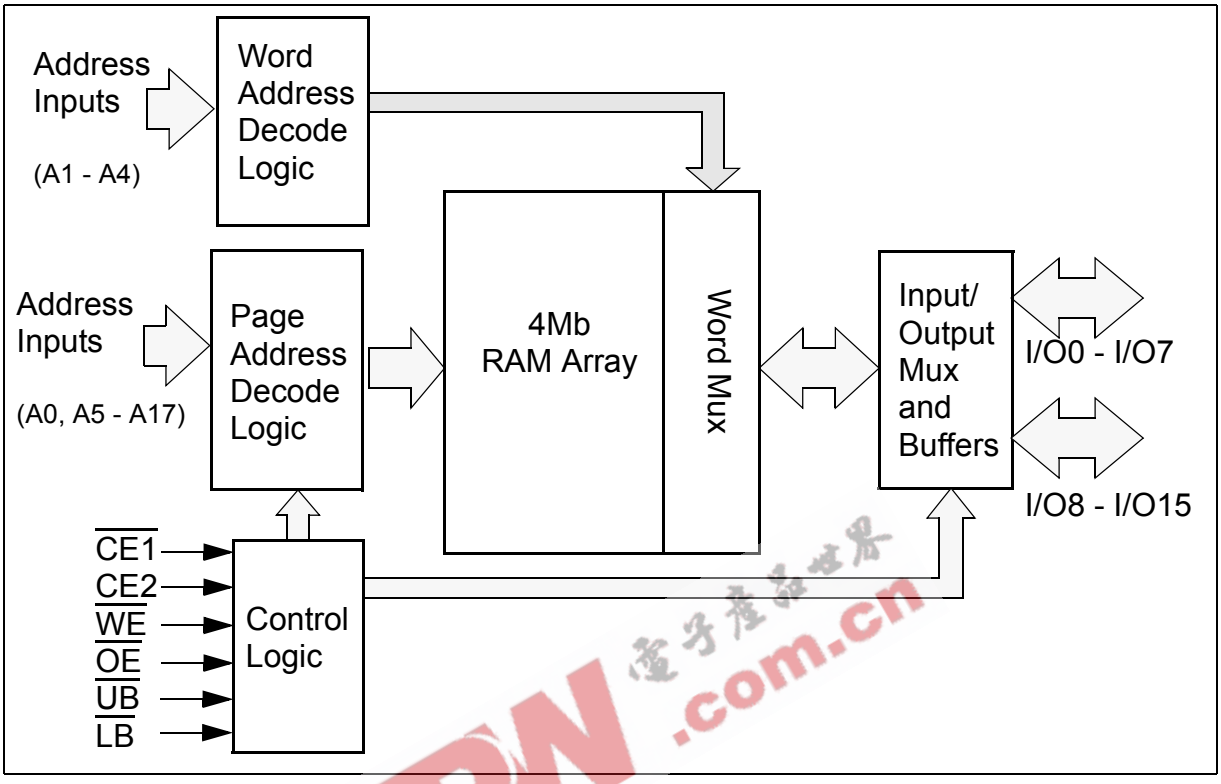
	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A_0	A_1	A_2	CE2
B	I/O_8	$\overline{UB}$	A_3	A_4	$\overline{CE1}$	I/O_0
C	I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2
D	V_{SSQ}	I/O_{11}	A_{17}	A_7	I/O_3	V_{CC}
E	V_{CCQ}	I/O_{12}	NC	A_{16}	I/O_4	V_{SS}
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6
G	I/O_{15}	NC	A_{12}	A_{13}	$\overline{WE}$	I/O_7
H	NC	A_8	A_9	A_{10}	A_{11}	NC

48 Pin BGA (top)

Pin Descriptions

Pin Name	Pin Function
A_0-A_{17}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CE1}$	Chip Enable 1 Input
CE2	Chip Enable 2 Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$	Lower Byte Enable Input
$\overline{UB}$	Upper Byte Enable Input
I/O_0-I/O_7	Lower Byte Data Input/Output
I/O_8-I/O_{15}	Upper Byte Data Input/Output
V_{CC}	Core Power
V_{CCQ}	Power for I/O
V_{SS}	Core Ground
V_{SSQ}	Ground for I/O
NC	Not Connected

Functional Block Diagram



Functional Description

$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	$\overline{UB}$[1]	$\overline{LB}$[1]	I/O_0 - I/O_{15}[1]	MODE	POWER
H	X	X	X	X	X	High Z	Standby[2]	Standby
X	L	X	X	X	X	High Z	Standby[2]	Standby
L	H	X	X	H	H	High Z	Standby	Standby
L	H	L	X[3]	L[1]	L[1]	Data In	Write[3]	Active
L	H	H	L	L[1]	L[1]	Data Out	Read	Active
L	H	H	H	L[1]	L[1]	High Z	Active	Active

1. When $\overline{UB}$ and $\overline{LB}$ are in select mode (low), I/O_0 - I/O_{15} are affected as shown. When $\overline{LB}$ only is in the select mode only I/O_0 - I/O_7 are affected as shown. When $\overline{UB}$ is in the select mode only I/O_8 - I/O_{15} are affected as shown.
2. When the device is in standby mode, control inputs ($\overline{WE}$, $\overline{OE}$, $\overline{UB}$, and $\overline{LB}$), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.
3. When $\overline{WE}$ is invoked, the $\overline{OE}$ input is internally disabled and has no effect on the circuit.

Capacitance[1]

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		8	pF
I/O Capacitance	$C_{I/O}$	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		8	pF

1. These parameters are verified in device characterization and are not 100% tested

Absolute Maximum Ratings[1]

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	–0.3 to V_{CC}+0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.3 to 4	V
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	–40 to 125	°C
Operating Temperature	T_A	-40 to +85	°C
Soldering Temperature and Time	T_{SOLDER}	260°C, 10sec	°C

1. Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Characteristics (Over Specified Temperature Range)

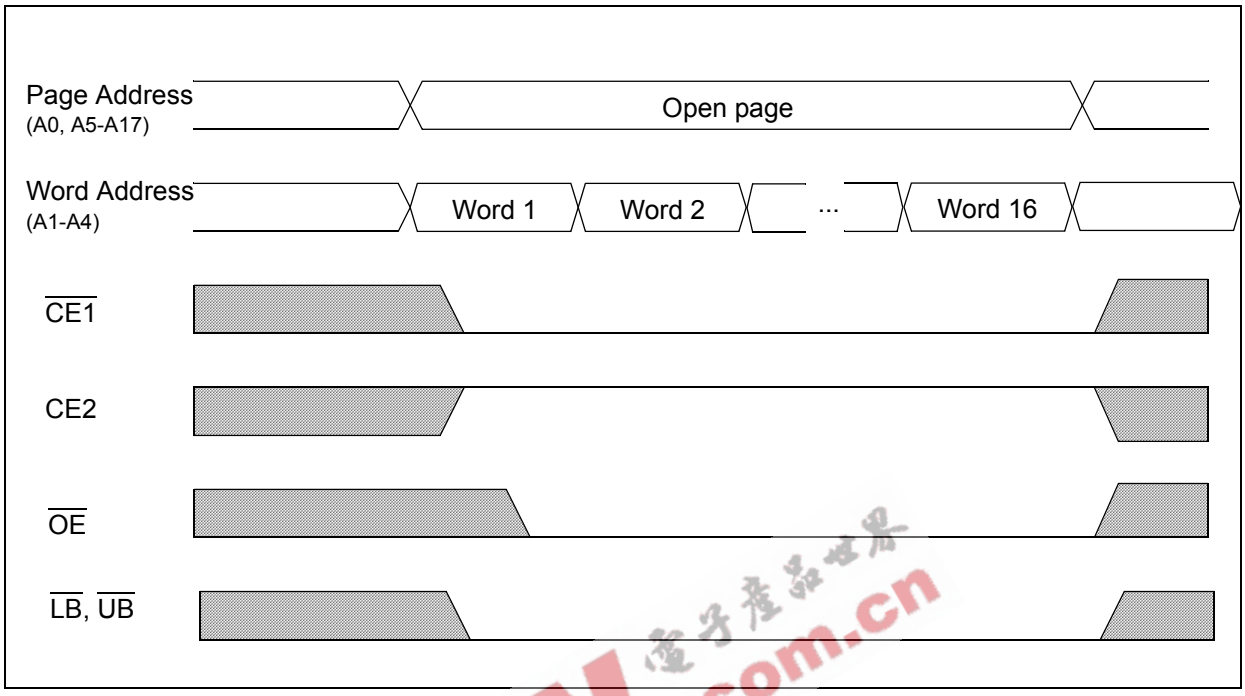
Item	Symbol	Device	Conditions	Min.	Typ	Max	Unit
Core Supply Voltage	V_{CC}	N04Q1612...	1.2V Core Device	1.1	1.2	1.3	V
		N04Q1618...	1.8V Core Device	1.65	1.8	1.95	
		N04Q1625...	2.5V Core Device	2.3	2.5	2.8	
		N04Q1630...	3V Core Device	2.7	3.0	3.6	
I/O Supply Voltage	V_{CCQ}	N04Q1612...	1.2V Core Device	1.1		3.3	V
		N04Q1618...	1.8V Core Device	1.65		3.3	
		N04Q1625...	2.5V Core Device	2.3		3.3	
		N04Q1630...	3V Core Device	2.7		3.6	
Input High Voltage	V_{IH}			0.8 x VCCQ		V_{CC}+0.3	V
Input Low Voltage	V_{IL}			–0.3		0.2 x VCCQ	
Output High Voltage	V_{OH}		I_{OH} = -100uA	V_{CC}–0.2			V
Output Low Voltage	V_{OL}		I_{OL} = 100uA			0.2	V
Input Leakage Current	I_{LI}		V_{IN} = 0 to V_{CC}			0.5	µA
Output Leakage Current	I_{LO}		$\overline{OE}$ = V_{IH} or Chip Disabled			0.5	µA

Power Consumption (T_A = 0°C - 70°C)

Device PN				Speed	Typ[1]	Max	
N04Q1612C2Bx-15C	Standby Current[2]	Isb	Chip Disabled V_{CC} = 1.3V, V_{IN} = V_{CC} or 0		50	500	nA
	Read/Write Current[3]	Icc	Chip Enabled, I_{OUT} = 0 V_{CC}=1.3V, V_{IN}=V_{IH} or V_{IL}	1us	0.4	0.5	mA
				150ns	2	3	
	Page Mode Current	Iccp	Chip Enabled, I_{OUT} = 0 V_{CC}=1.3V, V_{IN}=V_{IH} or V_{IL}	1us	80	100	µA
				150ns	300	450	
N04Q1618C2Bx-15C	Standby Current	Isb	Chip Disabled V_{CC} = 1.9V, V_{IN} = V_{CC} or 0V		50	500	nA
	Read/Write Current	Icc	Chip Enabled, I_{OUT} = 0 V_{CC}=1.9V, V_{IN}=V_{IH} or V_{IL}	1us	0.4	0.5	mA
				150ns	2	3	
	Page Mode Current	Iccp	Chip Enabled, I_{OUT} = 0 V_{CC}=1.9V, V_{IN}=V_{IH} or V_{IL}	1us	80	100	µA
				150ns	400	500	
N04Q1618C2Bx-70C	Standby Current	Isb	Chip Disabled V_{CC} = 1.9V, V_{IN} = V_{CC} or 0		0.2	1.5	µA
	Read/Write Current	Icc	Chip Enabled, I_{OUT} = 0 V_{CC}=1.9V, V_{IN}=V_{IH} or V_{IL}	1us	0.6	0.9	mA
				70ns	6	7	
	Page Mode Current	Iccp	Chip Enabled, I_{OUT} = 0 V_{CC}=1.9V, V_{IN}=V_{IH} or V_{IL}	1us	0.1	0.2	mA
				70ns	0.8	1	
N04Q1625C2Bx-15C	Standby Current	Isb	Chip Disabled V_{CC} = 2.8V, V_{IN} = V_{CC} or 0		0.8	1.0	µA
	Read/Write Current	Icc	Chip Enabled, I_{OUT} = 0 V_{CC}= 2.8V, V_{IN}=V_{IH} or V_{IL}	1us	0.6	1.0	mA
				150ns	3	4	
	Page Mode Current	Iccp	Chip Enabled, I_{OUT} = 0 V_{CC}= 2.8V, V_{IN}=V_{IH} or V_{IL}	1us	0.1	0.2	mA
				150ns	1.5	2	
N04Q1630C2Bx-70C	Standby Current	Isb	Chip Disabled V_{CC} = 3.6V, V_{IN} = V_{CC} or 0		0.8	4	µA
	Read/Write Current	Icc	Chip Enabled, I_{OUT} = 0 V_{CC}= 3.6V, V_{IN}=V_{IH} or V_{IL}	1us	2.2	3	mA
				70ns	8.5	10	
	Page Mode Current	Iccp	Chip Enabled, I_{OUT} = 0 V_{CC}= 3.6V, V_{IN}=V_{IH} or V_{IL}	1us	0.5	0.6	mA
				70ns	2	1.5	

1. Typical values are measured at Vcc=Vcc Typ., T_A=25°C and not 100% tested.
2. This device assumes a standby mode if the chip is disabled ($\overline{CE1}$ high or CE2 low). In order to achieve low standby current all inputs must be within 0.2 volts of either VCC or VSS. This applies to all ISB values.
3. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system. This applies to all Icc and Iccp values.

Power Savings with Page Mode Operation ($\overline{WE}$ = V_{IH})



Note: Page mode operation is a method of addressing the SRAM to save operating current. The internal organization of the SRAM is optimized to allow this unique operating mode to be used as a valuable power saving feature.

The only thing that needs to be done is to address the SRAM in a manner that the internal page is left open and 16-bit words of data are read from the open page. By treating addresses A1 - A4 as the least significant bits and addressing the 16 words within the open page, power is reduced to the page mode value which is considerably lower than standard operating currents for low power SRAMs.

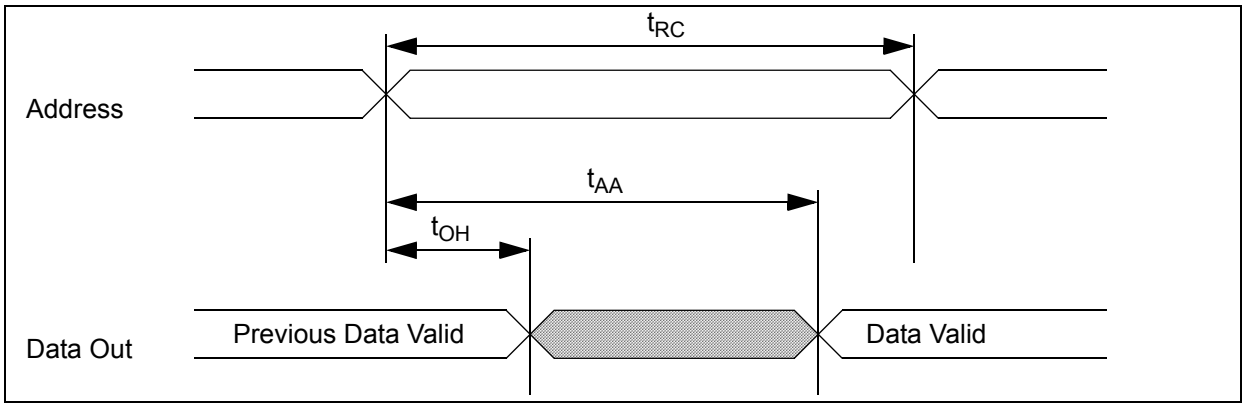
Timing Test Conditions

Item	
Input Pulse Level	$0.1V_{CC}$ to 0.9 V_{CC}
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	0.5 V_{CC}
Output Load	CL = 30pF
Operating Temperature	0 to +70°C

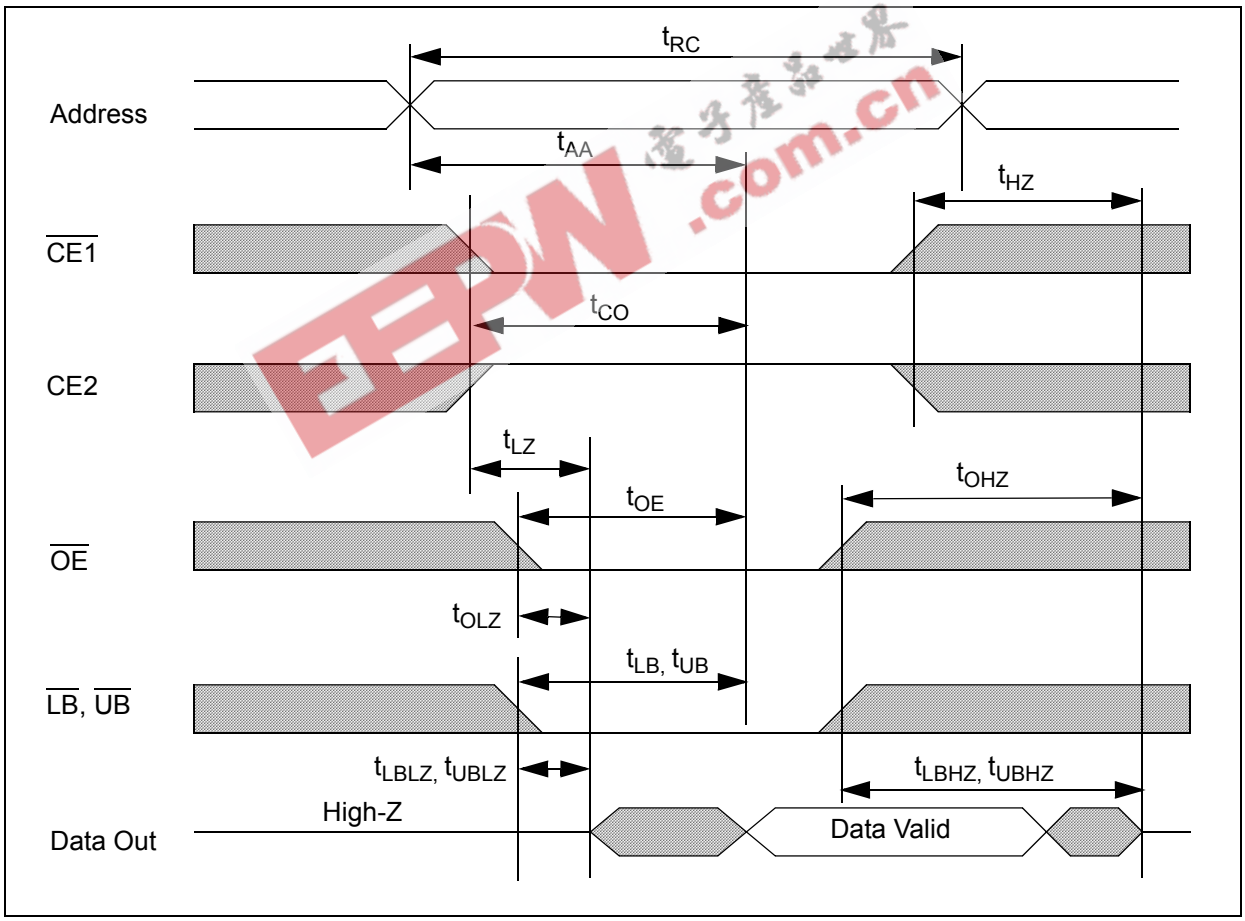
Timing

Item	Symbol	-70		-150		Units
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	70		150		ns
Address Access Time	t_{AA}		70		150	ns
Page Mode Address Access Time	t_{AAP}		35		75	ns
Chip Enable to Valid Output	t_{CO}		70		150	ns
Output Enable to Valid Output	t_{OE}		35		75	ns
Byte Select to Valid Output	t_{LB}, t_{UB}		70		150	ns
Chip Enable to Low-Z output	t_{LZ}	10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		ns
Byte Select to Low-Z Output	t_{LBZ}, t_{UBZ}	10		10		ns
Chip Disable to High-Z Output	t_{HZ}	0	20	0	20	ns
Output Disable to High-Z Output	t_{OHZ}	0	20	0	20	ns
Byte Select Disable to High-Z Output	t_{LBHZ}, t_{UBHZ}	0	20	0	20	ns
Output Hold from Address Change	t_{OH}	10		10		ns
Write Cycle Time	t_{WC}	70		150		ns
Chip Enable to End of Write	t_{CW}	50		120		ns
Address Valid to End of Write	t_{AW}	50		120		ns
Byte Select to End of Write	t_{LBW}, t_{UBW}	50		120		ns
Write Pulse Width	t_{WP}	40		100		ns
Address Setup Time	t_{AS}	0		0		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to High-Z Output	t_{WHZ}		20		20	ns
Data to Write Time Overlap	t_{DW}	40		100		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End Write to Low-Z Output	t_{OW}	5		5		ns

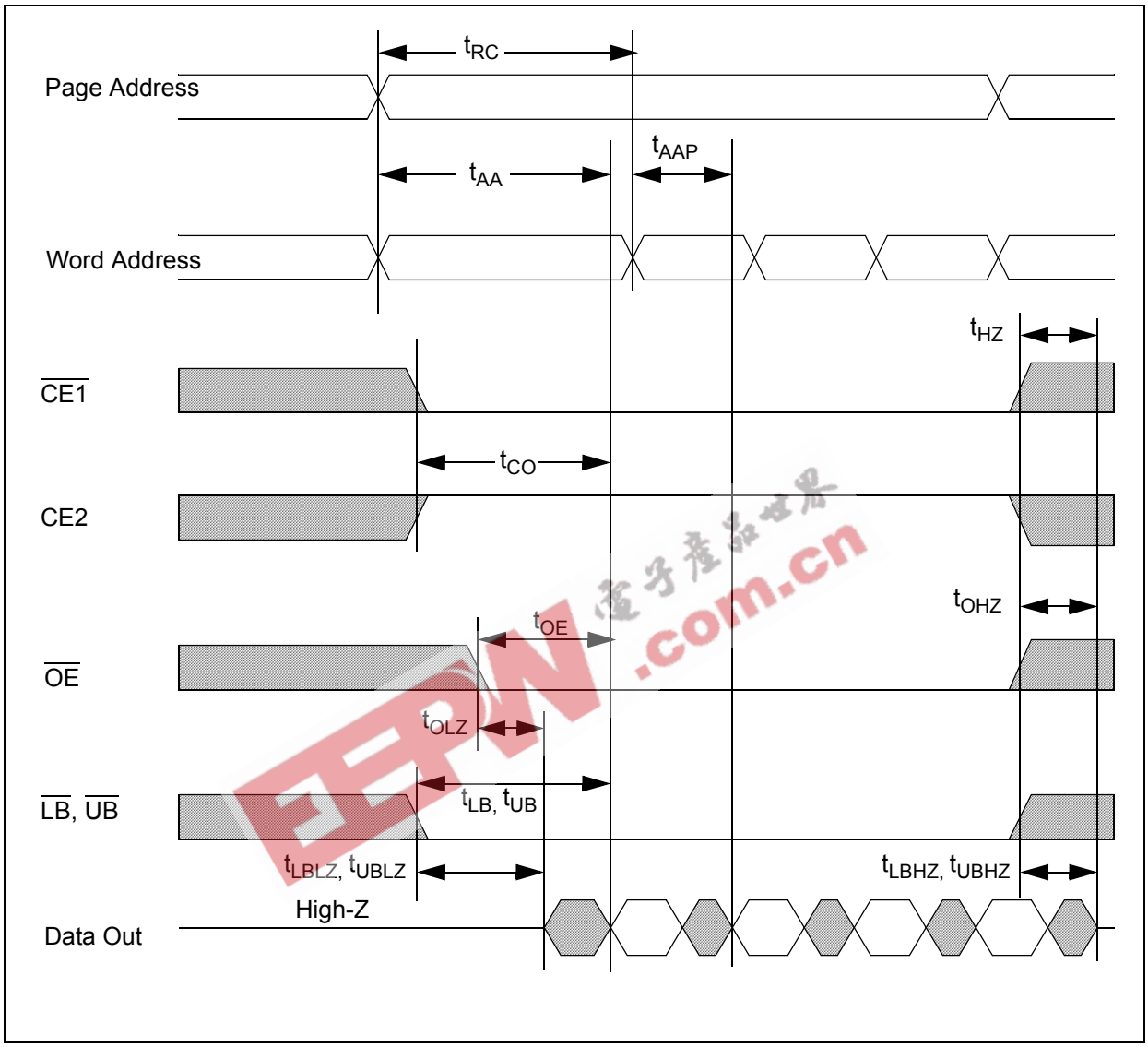
Timing of Read Cycle ($\overline{CE1}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = CE2 = V_{IH})



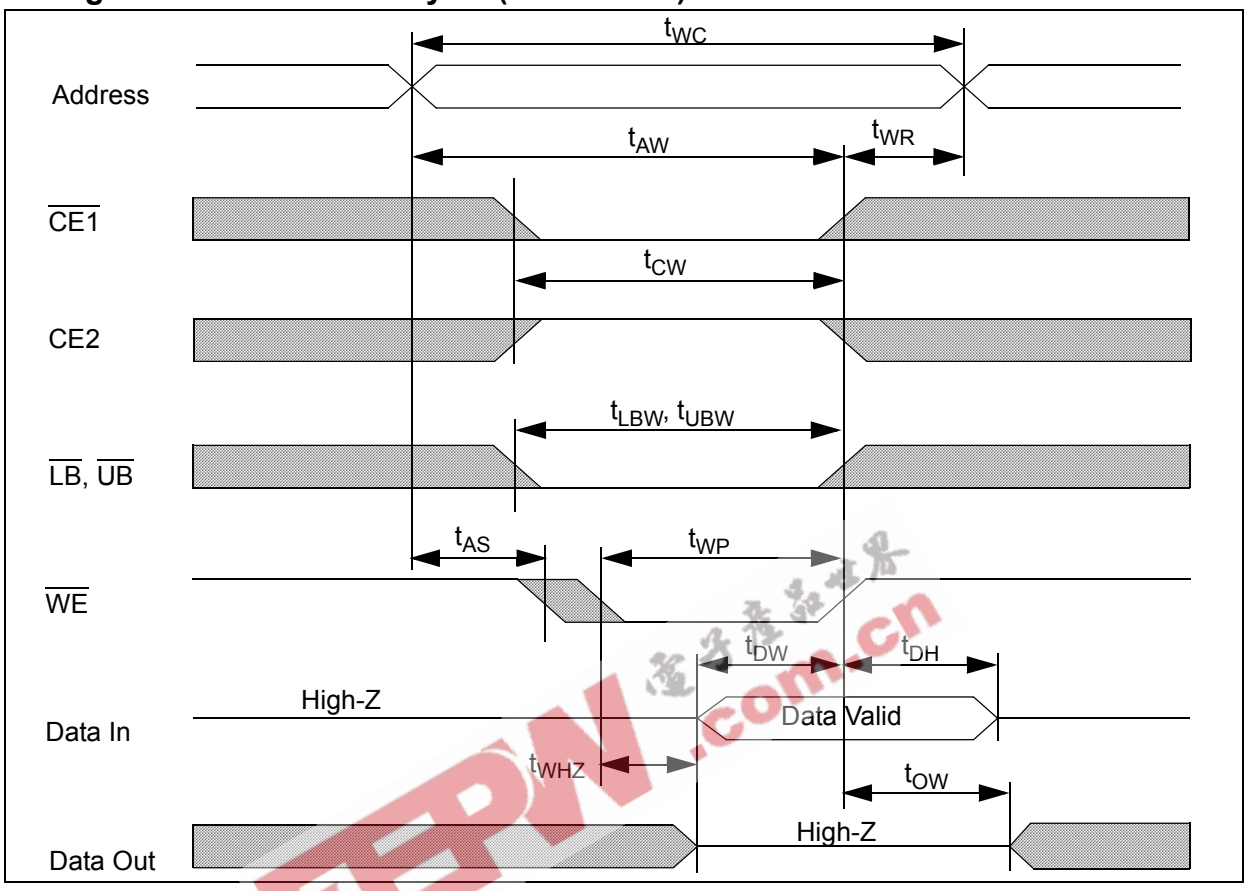
Timing Waveform of Read Cycle ($\overline{WE}$=V_{IH})



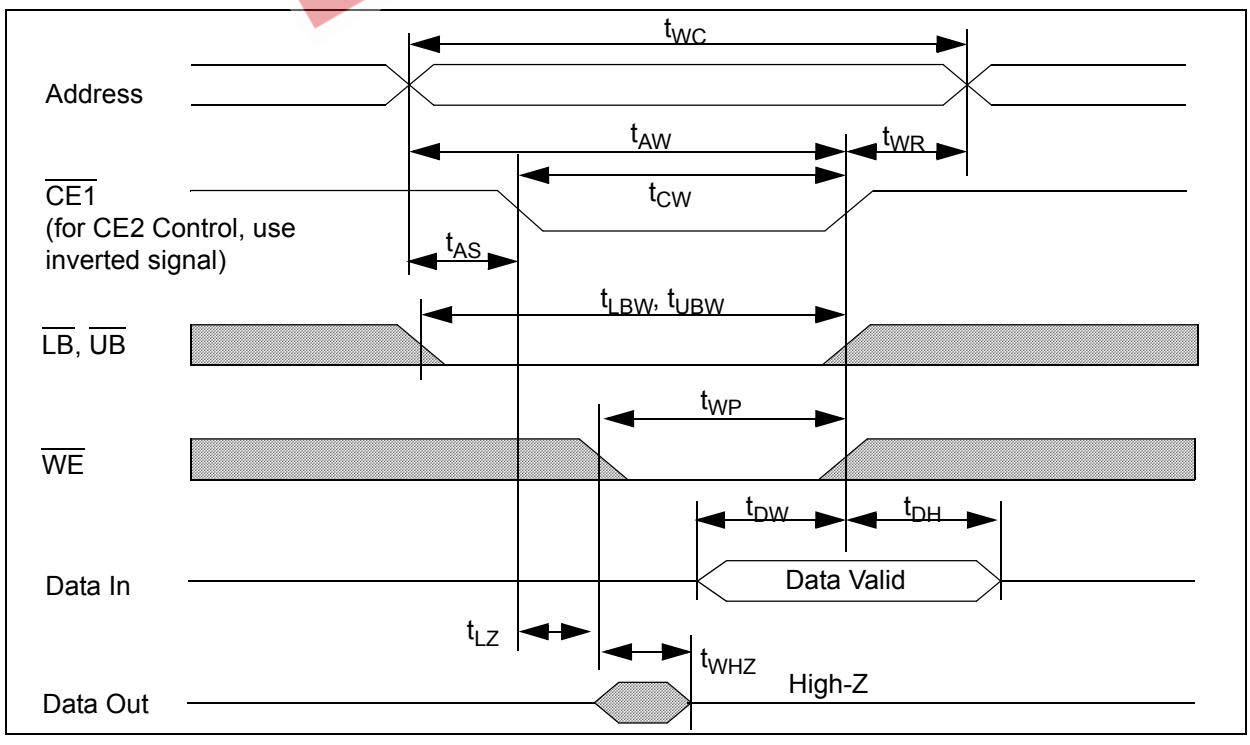
Timing Waveform of Page Mode Read Cycle ($\overline{WE}$ = V_{IH})



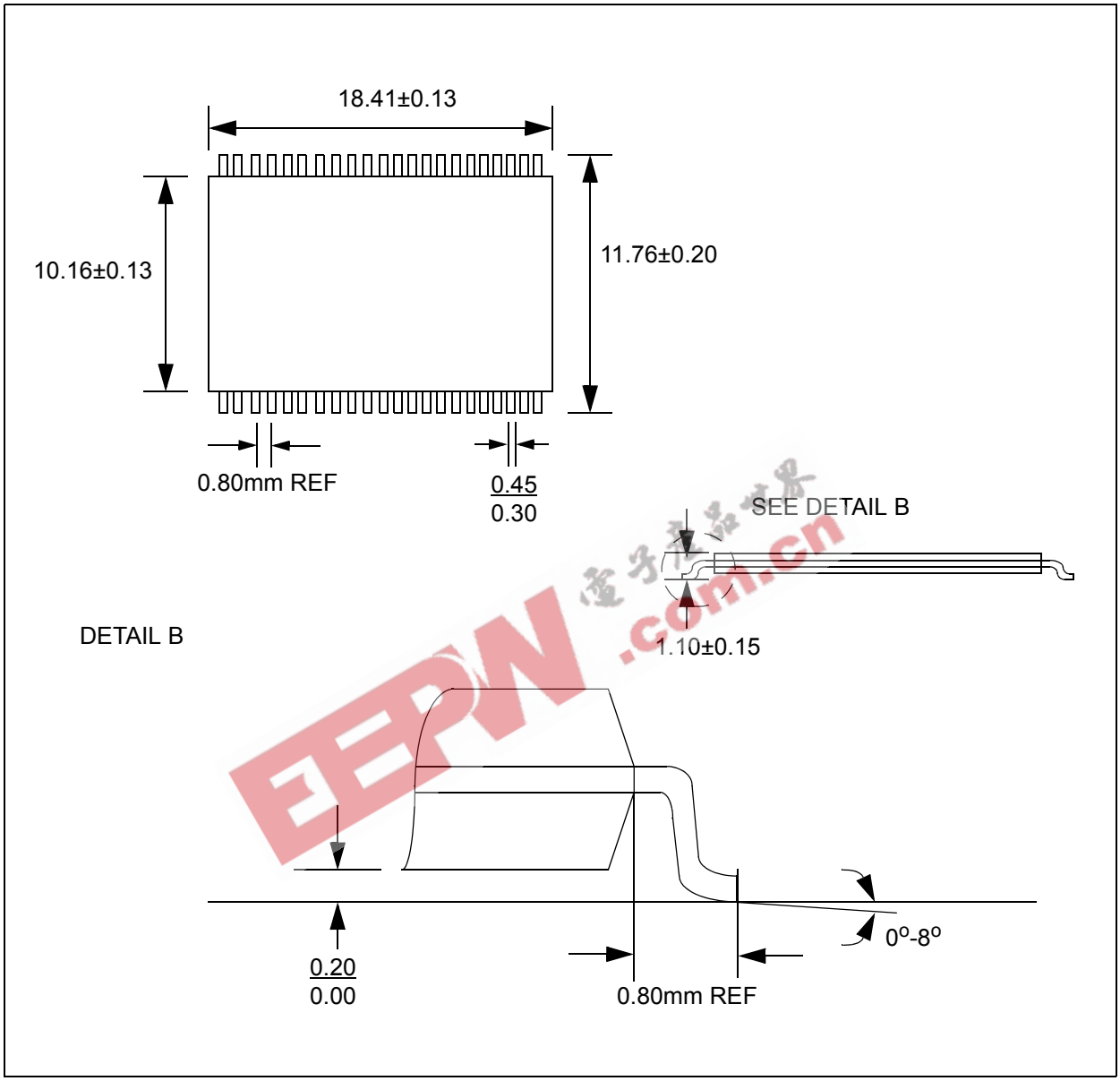
Timing Waveform of Write Cycle ($\overline{WE}$ control)



Timing Waveform of Write Cycle ($\overline{CE1}$ Control)

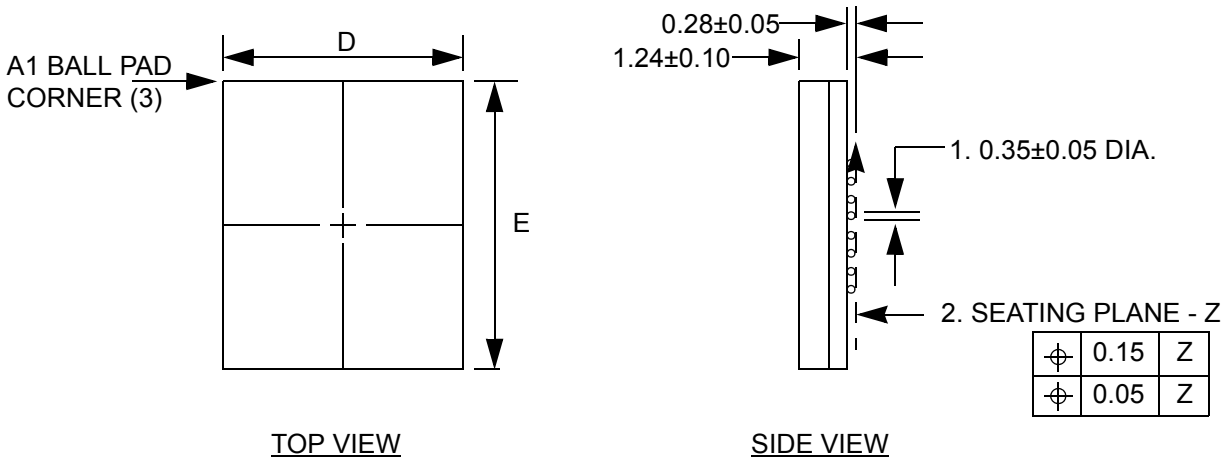


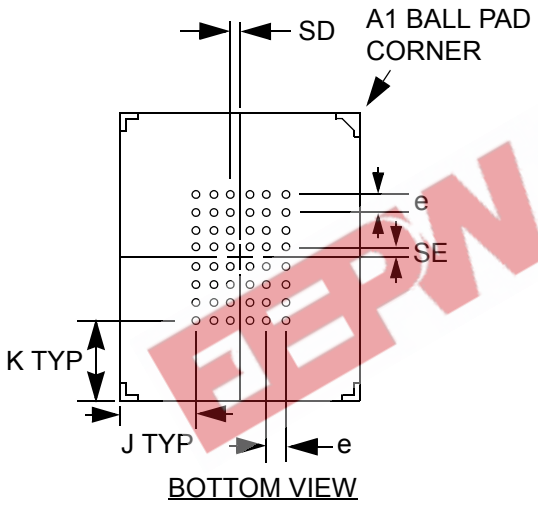
44-Lead TSOP II Package (T44)



Note:
1. All dimensions in inches (Millimeters)
2. Package dimensions exclude molding flash

Ball Grid Array Package





1. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER. PARALLEL TO PRIMARY Z.

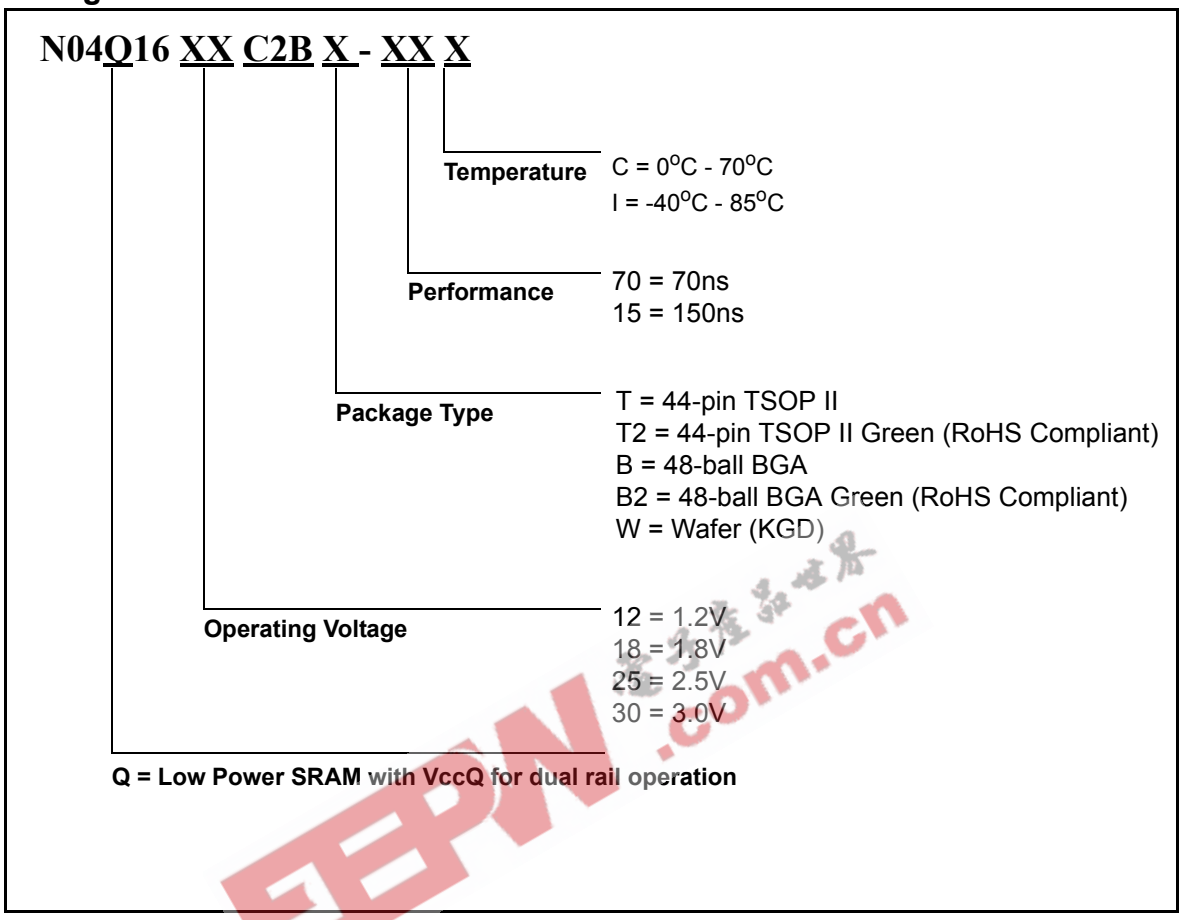
2. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

3. A1 BALL PAD CORNER I.D. TO BE MARKED BY INK.

Dimensions (mm)

D	E	e = 0.75				BALL MATRIX TYPE
		SD	SE	J	K	
6±0.10	8±0.10	0.375	0.375	1.125	1.375	FULL

Ordering Information



Revision History

Revision	Date	Change Description
A	October 2005	Initial Advanced Release
B	February 2006	Raised maximum Vcc to 3.6V for 3V device Added green packages Changed dual rail to 'Q' part designator