

## N- and P-Channel Enhancement-Mode Dual MOSFET

### Features

- ▶ 500V breakdown voltage
- ▶ Independent N- and P-channels
- ▶ Electrically isolated N- and P-channels
- ▶ Low input capacitance
- ▶ Fast switching speeds
- ▶ Free from secondary breakdowns
- ▶ Low input and output leakage

### Applications

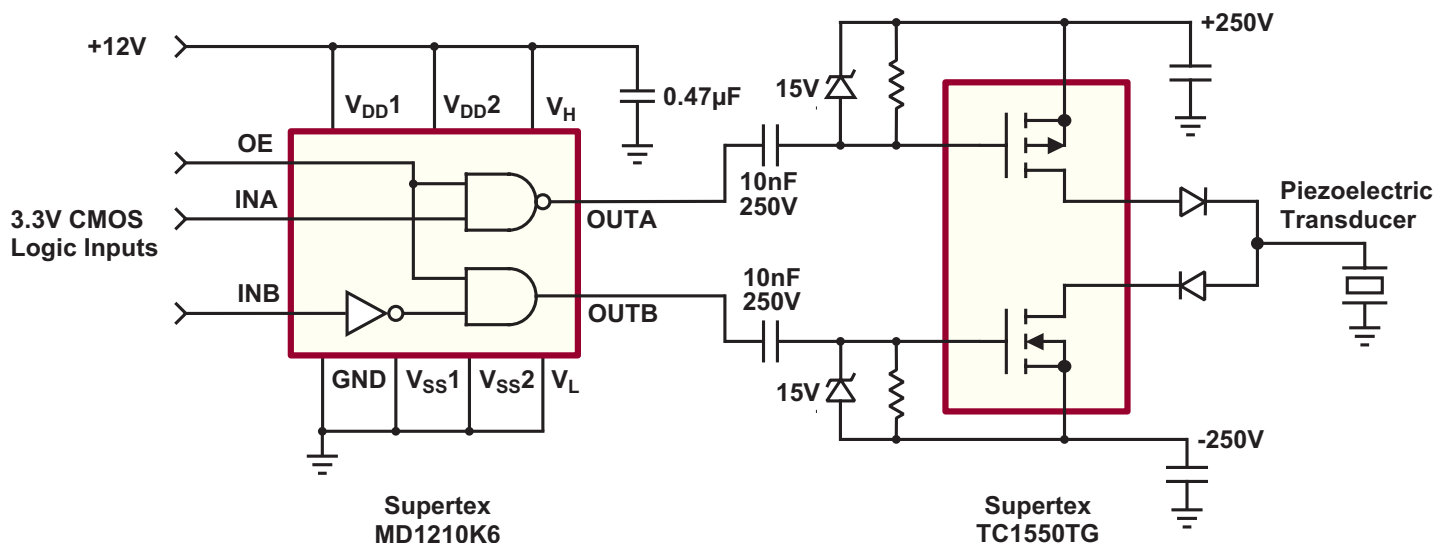
- ▶ High voltage pulsers
- ▶ Amplifiers
- ▶ Buffers
- ▶ Piezoelectric transducer drivers
- ▶ General purpose line drivers

### General Description

The Supertex TC1550TG-G consists of a high voltage N-channel and P-channel MOSFET in an SO-8 package. These are enhancement-mode (normally-off) transistors utilizing an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Typical Application Circuit



## Ordering Information

Device	BV <sub>DSS</sub> /BV <sub>DGS</sub>		R <sub>DS(ON)</sub> (Max)		Package Option
	N-Channel	P-Channel	N-Channel	P-Channel	8-Lead SO
TC1550	500V	-500V	60Ω	125Ω	TC1550TG-G

-G indicates package is RoHS compliant ('Green')



## Absolute Maximum Ratings

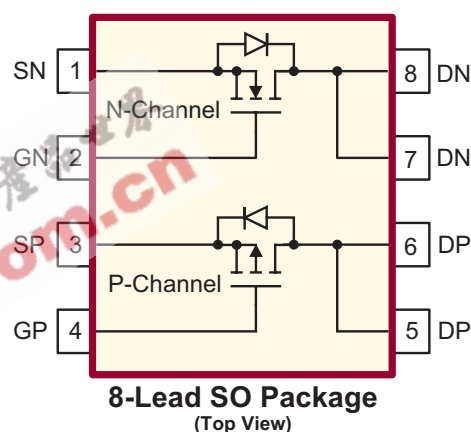
Parameter	Value
Drain-to-source voltage	BV <sub>DSS</sub>
Drain-to-gate voltage	BV <sub>DGS</sub>
Gate-to-source voltage	±20V
Operating and storage temperature	-55°C to + 150°C
Soldering temperature <sup>1</sup>	300°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Note:

1. Distance of 1.6mm from case for 10 seconds.

## Pin Configuration



## N-Channel Electrical Characteristics (T<sub>A</sub> = 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	500	-	-	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1mA
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	-	4.0	V	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 1mA
ΔV <sub>GS(th)</sub>	Change in V <sub>GS(th)</sub> with Temperature	-	-3.8	-5.0	mV/°C	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 1mA
I <sub>GSS</sub>	Gate Body Leakage Current	-	-	100	nA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	-	-	10	μA	V <sub>GS</sub> = 0V, V <sub>DS</sub> = Max Rating
		-	-	1.0	mA	V <sub>DS</sub> = 0.8 Max Rating, V <sub>GS</sub> = 0V, T <sub>A</sub> = 125°C
I <sub>D(ON)</sub>	On-State Drain Current	-	100	-	mA	V <sub>GS</sub> = 5.0V, V <sub>DS</sub> = 25V
		150	350	-		V <sub>GS</sub> = 10V, V <sub>DS</sub> = 25V
R <sub>DS(ON)</sub>	Static Drain-to-Source ON-State Resistance	-	45	-	Ω	V <sub>GS</sub> = 5.0V, I <sub>D</sub> = 50mA
		-	40	60		V <sub>GS</sub> = 10V, I <sub>D</sub> = 50mA
ΔR <sub>DS(ON)</sub>	Change in R <sub>DS(ON)</sub> with Temperature	-	1.0	1.7	%/°C	V <sub>GS</sub> = 10V, I <sub>D</sub> = 50mA
G <sub>FS</sub>	Forward Transconductance	50	100	-	mmho	V <sub>DS</sub> = 25V, I <sub>D</sub> = 50mA

## N-Channel Electrical Characteristics (cont.)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$C_{ISS}$	Input Capacitance	-	45	55	pF	$V_{GS} = 0V$ , $V_{DS} = 25V$ , $f = 1MHz$
$C_{OSS}$	Common Source Output Capacitance	-	8.0	10		
$C_{RSS}$	Reverse Transfer Capacitance	-	2.0	5.0		
$t_{d(ON)}$	Turn-ON Delay Time	-	-	10	ns	$V_{DD} = 25V$ , $I_D = 150mA$ , $R_{GEN} = 25\Omega$
$t_r$	Rise Time	-	-	15		
$t_{d(OFF)}$	Turn-Off Delay Time	-	-	10		
$t_f$	Fall Time	-	-	10		
$V_{SD}$	Diode Forward Voltage Drop	-	0.8	-	V	$V_{GS} = 0V$ , $I_{SD} = 500mA$
$t_{rr}$	Reverse Recovery Time	-	300	-	ns	$V_{GS} = 0V$ , $I_{SD} = 500mA$

P-Channel Electrical Characteristics ( $T_A = 25^\circ C$  unless otherwise specified)

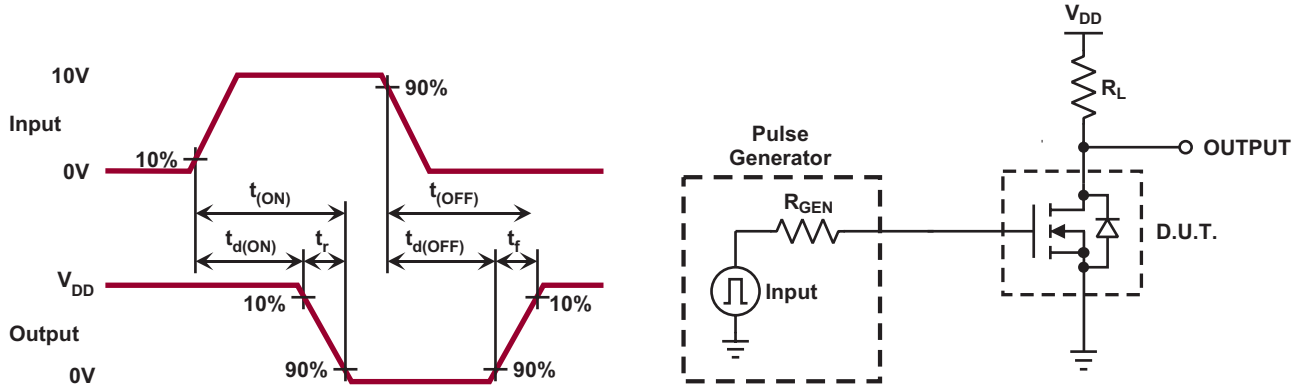
Symbol	Parameter	Min	Typ	Max	Units	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	-500	-	-	V	$V_{GS} = 0V$ , $I_D = -1mA$
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	-	-4.5	V	$V_{GS} = V_{DS}$ , $I_D = -1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature	-	3.5	6.0	mV/°C	$V_{GS} = V_{DS}$ , $I_D = -1mA$
$I_{GSS}$	Gate Body Leakage Current	-	-	100	nA	$V_{GS} = \pm 20V$ , $V_{DS} = 0V$
$I_{DSS}$	Zero Gate Voltage Drain Current	-	-	-10	$\mu A$	$V_{GS} = 0V$ , $V_{DS} = \text{Max Rating}$
		-	-	-1.0	mA	$V_{DS} = 0.8 \text{ Max Rating}$ , $V_{GS} = 0V$ , $T_A = 125^\circ C$
$I_{D(ON)}$	On-State Drain Current	-	-90	-	mA	$V_{GS} = -5.0V$ , $V_{DS} = -25V$
		-100	-240	-		$V_{GS} = -10V$ , $V_{DS} = -25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance	-	85	-	$\Omega$	$V_{GS} = -5.0V$ , $I_D = -5.0mA$
		-	80	125		$V_{GS} = -10V$ , $I_D = -10mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature	-	0.85	-	%/°C	$V_{GS} = -10V$ , $I_D = -10mA$
$G_{FS}$	Forward Transconductance	25	40	-	mmho	$V_{DS} = -25V$ , $I_D = -10mA$
$C_{ISS}$	Input Capacitance	-	40	70	pF	$V_{GS} = 0V$ , $V_{DS} = -25V$ , $f = 1MHz$
$C_{OSS}$	Common Source Output Capacitance	-	10	20		
$C_{RSS}$	Reverse Transfer Capacitance	-	3.0	10		
$t_{d(ON)}$	Turn-ON Delay Time	-	5.0	10	ns	$V_{DD} = -25V$ , $I_D = -100mA$ , $R_{GEN} = 25\Omega$
$t_r$	Rise Time	-	8.0	10		
$t_{d(OFF)}$	Turn-Off Delay Time	-	8.0	15		
$t_f$	Fall Time	-	5.0	16		
$V_{SD}$	Diode Forward Voltage Drop	-	-0.8	-1.5	V	$V_{GS} = 0V$ , $I_{SD} = -100mA$
$t_{rr}$	Reverse Recovery Time	-	200	-	ns	$V_{GS} = 0V$ , $I_{SD} = -100mA$

## Notes:

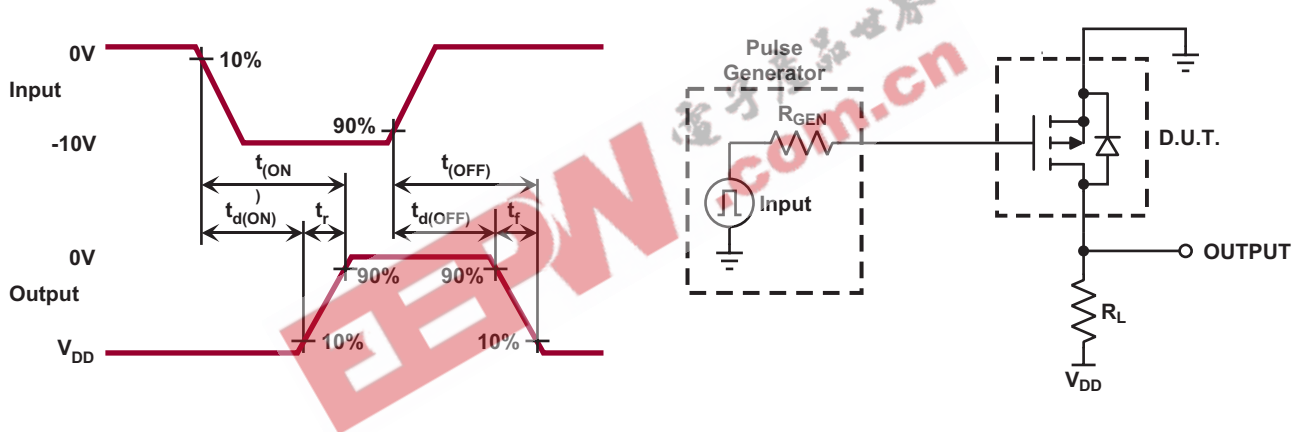
(1) All DC parameters 100% tested at 25°C unless otherwise stated. (Pulsed test: 300μs pulse at 2% duty cycle.)

(2) All AC parameters sample tested.

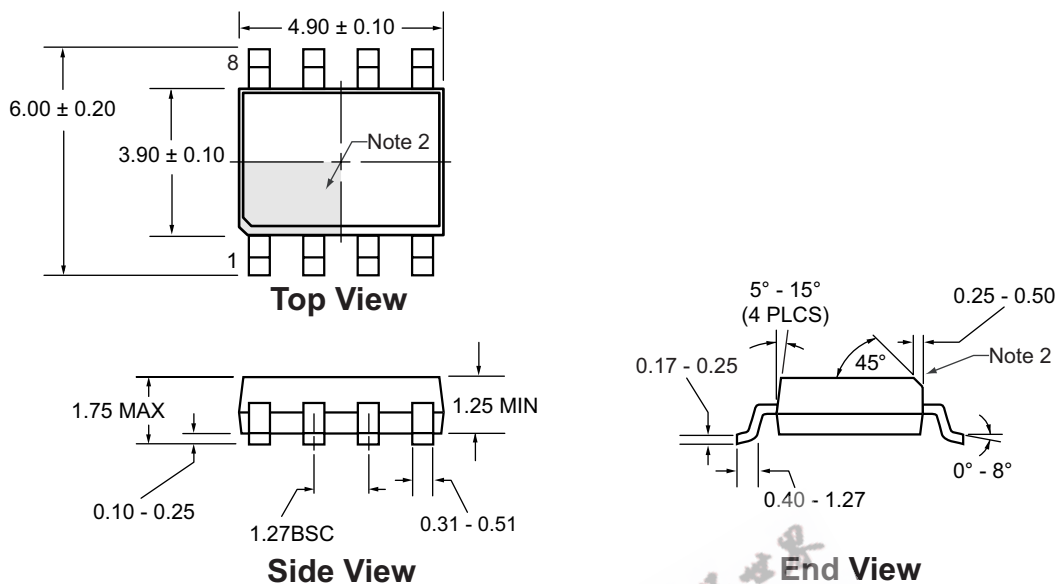
N-Channel Switching Waveforms and Test Circuit



P-Channel Switching Waveforms and Test Circuit



## 8-Lead SO (TG) Package Outline



## Notes:

1. All dimensions in millimeters. Angles in degrees.
2. If the corner is not chamfered, then a Pin 1 identifier must be located within the area indicated.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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