N-Channel Enhancement Mode Dual DMOS FET

calogic
CORPORATION

SD411

FEATURES

- **Normally "OFF" Configuration**
- **High Speed Switching. . . . . under 1 ns (typically)**
- **Ultra Low Capacitance . . . . . c_{iss} <3.5 pf (typically)**
- **Tight Matching Characteristics**
- **Pin Compatible to Industry Standard Dual JFETs with Addition of Substrate Bias Pin**

APPLICATIONS

- **Wideband Differential Amplifiers**
- **Cascode Amplifiers**
- **High Intercept Point Balanced Mixers**
- **Oscillators**
- **High Speed Analog Comparators**

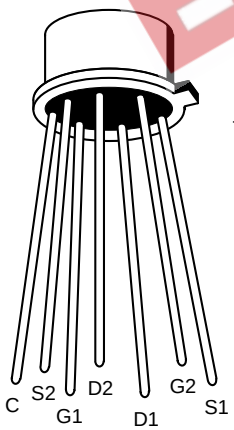
DESCRIPTION

The SD411 is constructed utilizing Calogic's high speed lateral DMOS techniques featuring tight matching characteristics between each FET. This device is an excellent choice for instrumentation, communication, RF and Video designs.

ORDERING INFOMATION

Part	Package	Temperature Range
SD411	TO-78 Hermetic Package	-55°C to +150°C
XSD411	Sorted Chips in Carriers	-55°C to +150°C

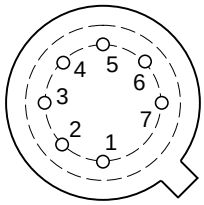
PIN CONFIGURATION



TO-78

CD2

1 SOURCE 1
2 DRAIN 1
3 GATE 1
4 CASE/BODY
5 SOURCE 2
6 DRAIN 2
7 GATE 2



BOTTOM VIEW

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

V_{DS}	Drain-Source Voltage	+20V	P_D	Device Dissipation (each side)	360 mW
V_{SD}	Source-Drain Voltage	+10V		Derating Factor	2.88 mW/°C
V_{DB}	Drain-Body voltage	+25V	P_D	Total Device Dissipation	500 mW
V_{SB}	Source-Body Voltage	+15V		Derating Factor	4 mW/°C
V_{GD}	Gate-Drain Voltage	+25V	T_j	Operating Junction Temperature Range	-55 to +125°C
V_{GS}	Gate-Source Voltage	+25V	T_S	Storage Temperature Range	-55 to +150°C
V_{GB}	Gate-Body Voltage	+25V	T_L	Lead Temperature (1/16' from mounting surface for 10 sec.)	+260°C
V_{G1G2}	Gate-to-Gate Voltage	+25V			
V_{D1D2}	Drain-to-Drain Voltage	+20V			
V_{S1S2}	Source-to-Source Voltage	+15V			
I_D	Continuous Drain Current	+50 mA			

ELECTRICAL CHARACTERISTICS(T_A = +25°C per side unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	TEST CONDITIONS
STATIC						
BV_{DS}	Drain Source Breakdown Voltage	20			V	I_D = 10 nA, V_{GS} = V_{BS} = -5V
BV_{SD}	Source-Drain Breakdown Voltage	10				I_S = 10 nA, V_{GD} = V_{BD} = -5V
BV_{DB}	Drain-Body Breakdown Voltage	25				I_D = 10 nA, V_{GB} = 0 Source Open
BV_{SB}	Source-Body Breakdown Voltage	15				I_S = 10µA, V_{GB} = 0 Drain Open
I_{DSX}	Drain-Source Leakage Current		0.7	10	nA	V_{DS} = 20V, V_{GS} = V_{BS} = -5V
I_{GBS}	Gate-Body Leakage Current			1.0	µA	V_{GS} = 25V, V_{DB} = V_{SB} = 0
$V_{GS(th)}$	Gate-Source Threshold Voltage	0.5	1.0	2.0	V	I_D = 1.0µA, V_{DS} = V_{GS}, V_{SB} = 0
$r_{DS(ON)}$	Drain-Source ON Resistance (1)			70	ohms	I_D = 1.0mA, V_{GS} = 5.0V, V_{SB} = 0
DYNAMIC						
g_{fs}	Common-Source Forward Transconductance(1)	10	12		mS	V_{DS} = 10V, I_D = 20mA, V_{SB} = 0 f = 1KHZ
C_{iss}	Common-Source Input Capacitance		3.5		pF	V_{DS} = 10V, V_{GS} = V_{BS} = 0 f = 1MHZ
C_{oss}	Common-Source Output Capacitance		1.2			
C_{rss}	Common Source Reverse Transfer Capacitance		0.3			
$C_{(gs + sb)}$	Source Node Capacitance		4.5			
MATCH						
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate Source Voltage		25		mV	V_{DS} = 10V, I_D = 5.0mA, V_{SB} = 0
$\frac{\Delta \lvert V_{GS1} - V_{DS2} \rvert}{\Delta T}$	Differential Drift		25		µV/ °C	T_A = -55°C to +125C°

NOTE 1: Pulse Test, 80sec, 1% Duty Cycle