

CMOS Single-Supply Rail-to-Rail Input/Output Operational Amplifier

OP150/OP250/OP450

FEATURES PIN CONFIGURATIONS Single-Supply Operation: 2.7 V to 6 V High Output Current: ±250 mA 5-Lead SOT23-5 8-Lead Narrow-Body SO Low Supply Current: 600 µA/Amp (S Suffix) (RT Suffix) Wide Bandwidth: 4 MHz Slew Rate: 6.5 V/µs No Phase Reversal NC [**Low Input Currents** _IN [**OP150** Unity Gain Stable +IN [⊐ ουτ OP150 PPLICATIONS Battery Powered Instrumentation Multi Media Audio 8 Lead Epoxy DIP 8-Lead Narrow-Body SO Medical (P Suffix) (S Suffix) Remo∕te \$en≴ors ASK Input or Output Amplifier Automotive OP250 OUT A 1 8 V+ Headphone Drive OUT 7 OUT B 6 -IN B **GENERAL DESCRIPTION** The OP150, OP250 and OP450 are single, dual and quad 14-Lead Epoxy DIP Lead SQ (P Suffix) CMOS single-supply, 4 MHz bandwidth amplifiers featuring Suffix) rail-to-rail inputs and outputs. All are guaranteed to operate from a 3 volt single supply as well as a +5 volt supply. OUT A 14 OUT D The OP150 family of amplifiers have very low input bias cur-OUT A rents. The outputs are capable of driving 250 mA loads and are 13 -IN A 2 -IN D □ –IN D **OP450** stable with capacitive loads as high as 500 pF. +IN A 3 12 +IN D +IN A □ ☐ +IN D V+ 4 11 V-V+ [□ v– Applications for these amplifiers include portable medical **OP450** +IN B □ ☐ +IN C +IN B 5 equipment, safety and security, and interface for transducers 10 +IN C □ -IN C –IN B □ with high output impedances. 9 -IN C OUT C OUT B [8 OUT C Supply current is only 600 µA per amplifier. The ability to swing rail-to-rail at both the input and output enables designers to build multistage filters in single-supply sys-14-Lead tems and maintain high signal-to-noise ratios. **TSSOP** (RU Suffix) The OP150/OP250/OP450 are specified over the extended industrial (-40°C to +125°C) temperature range. The OP150 single amplifiers are available in 8-pin SO surface mount and the 5-pin SOT23-5 packages. The OP250 dual is available in 8pin plastic DIPs and SO surface mount packages. The OP450 **OP450** quad is available in 14-pin DIPs, TSSOP and narrow 14-pin SO

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packages. Consult factory for TSSOP availability.

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OP150/OP250/OP450-SPECIFICATIONS

 $\hline \textbf{ELECTRICAL CHARACTERISTICS} \quad (@V_S = +3.0 \text{ V}, V_{CM} = 0.05 \text{ V}, V_0 = 1.4 \text{ V}, T_A = +25 ^{\circ}\text{C}, unless otherwise noted})$

Parameter	Symbol	Conditions	Min	Тур	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage OP150	V_{OS}				5	mV
000 - 11 1 000000000000000		$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$			_	mV
Offset Voltage OP250/OP450	V_{OS}	400C < T < 1050C			5	mV
Input Bias Current	I_{B}	$-40^{\circ}\text{C} \le T_{A} \le +125^{\circ}\text{C}$		10	60	mV pA
input bias Current	1B	$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$		10	00	pA pA
Input Offset Current	I_{OS}	10 C = 1A = +120 C		25		pA pA
	-03	$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$				pA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	$V_{\rm CM} = 0 \text{ V} \text{ to } 3 \text{ V}$	60			dB
		$-40^{\circ}C \le T_{A} \le +125^{\circ}C$				dB
Large Signal Voltage Gain	A_{VO}	$R_L = 10 \text{ k}\Omega, V_O = 0.3 \text{ V to } 2.7 \text{ V}$		40		V/mV
I have Signal Voltage Cair	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$		10		V/mV
Large Signal Voltage Gain Large Signal Voltage Gain	AVO	$R_L = 2 \text{ k}\Omega, V_O = 0.3 \text{ V to } 2.7 \text{ V}$ $R_L = 1 \text{ k}\Omega, V_O = 0.3 \text{ V to } 2.7 \text{ V}$		16 10		V/mV V/mV
Offset Voltage Drift	A_{V} ΔV ΔV ΔV	$N_{L} = 1 \text{ K22}, V_{O} = 0.3 \text{ V to } 2.7 \text{ V}$		10		μV/°C
Blas Current Drift	$\Delta I_{\rm B}/\Delta T$		7			pA/°C
Offset Current Drift	Al _{os} /AT					pA/°C
OLUMBIA CHA DA CENDRATA CO						
OUTPUT CHARACTERISTICS		_T \100\	2.95	I_{299}		V
Output Voltage High	VOH	I _L = 100 µA	2.95	2 2.99		V
		40°C to +125°C I _L = 10 mA		2.95		/ V
		-40°C to +125°C		2.93	/ /	\\ \\ \
Output Voltage Low	V_{OL}	$I_{L} = 100 \mu A$		$_{2}$ / /	′ 10 /	mV
Output Voltage Low	VOL	-40°C to +125°C		~ / /	10 /	/mV
		$I_{L} = 10 \text{ mA}$		30	55 /	LmV
	1	-40°C to +125°C				mV
Output Current	I_{OUT}			± 250		mA
		-40°C to +125°C				mA
Open Loop Impedance	Z _{OUT}	$f = 1 \text{ MHz}, A_V = 1$				Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7 \text{ V to 6 V}$	70			dB
11 5		$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$	68			dB
Supply Current/Amplifier	I_{SY}	$V_O = 0 V$		500	600	μA
		$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$		650		μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 10 \text{ k}\Omega$		2.7		V/µs
Settling Time	$t_{\rm S}$	To 0.01%				μs
Gain Bandwidth Product	GBP			2		MHz
Phase Margin	Øo			75		Degrees
Channel Separation	CS	$f = 1 \text{ kHz}, R_L = 10 \text{ k}\Omega$				dB
NOISE PERFORMANCE						
Voltage Noise	a n-n	0.1 Hz to 10 Hz				μV p-p
Voltage Noise Density	e _n p-p	f = 1 kHz		55		μν p-p nV/√Hz
Current Noise Density	$\begin{vmatrix} \mathbf{e_n} \\ \mathbf{i_n} \end{vmatrix}$	1 - 1 KHIL	1	00		pA/\sqrt{Hz}

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OP150/OP250/OP450

$\hline \textbf{ELECTRICAL CHARACTERISTICS} \text{ (@ $V_S = +5.0$ V, $V_{CM} = 0.05$ V, $V_0 = 1.4$ V, $T_A = +25^{\circ}$C, unless otherwise noted) }$

Parameter	Symbol	Conditions	Min	Тур	Max	Units
INPUT CHARACTERISTICS Offset Voltage OP150	V _{OS}	40°C < T < .195°C			5	mV
Offset Voltage OP250/OP450	V _{OS}	$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$			5	mV mV
Input Bias Current	I_{B}	$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$		30	50	mV pA
Input Offset Current	I _{OS}	$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$ $-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$		0.1	60 8 16	pA pA pA
Input Voltage Range Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0 V \text{ to } 5 V$	0 60		5	V dB
Large Signal Voltage Gain	A_{VO}	$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$ $\text{R}_{\text{L}} = 10 \text{ k}\Omega, \text{ V}_{\text{O}} = 0.3 \text{ V to } 4.7 \text{ V}$		40		dB V/mV
Large Signal Voltage Gain Large Signal Voltage Gain Offset Voltage Brift Bias Current Drift Offset Current Drift	Ανο Ανο ΔVος ΔΤ ΔΙ _Ο ς/ΔΤ	$ \begin{array}{c} -40^{\circ}\text{C} \leq T_{A} \leq +125^{\circ}\text{C} \\ R_{L} = 2 \text{ k}\Omega, V_{O} = 0.3 \text{ V to } 2.7 \text{ V} \\ R_{L} = 1 \text{ k}\Omega, V_{O} = 0.3 \text{ V to } 2.7 \text{ V} \\ \hline -40^{\circ}\text{C} \leq T_{A} \leq +125^{\circ}\text{C} \end{array} $	•	16 10 1.5 100 20		V/mV V/mV V/mV μV/°C pA/°C pA/°C
OUTPUT CHARACTERISTICS Output Voltage High	V _{OH}	$L = 100 \mu\text{A}$ -40°C to +125°C		4.99		¥ 7
Output Voltage Low	V _{OL}	$\begin{array}{c} I_L = 10 \text{ mA} \\ -40^{\circ}\text{C to } + 125^{\circ}\text{C} \\ I_L = 100 \mu\text{A} \\ -40^{\circ}\text{C to } + 125^{\circ}\text{C} \\ I_L = 10 \text{ mA} \end{array}$		$\begin{pmatrix} 4.96 \\ 2 \end{pmatrix}$		V V mV mV
Output Current	Iout	-40°C to +125°C -40°C to +125°C		± 250		m V mA mA
Open Loop Impedance	Z _{OUT}	$f = 1 \text{ MHz}, A_V = 1$				Ω
POWER SUPPLY Power Supply Rejection Ratio Supply Current/Amplifier	PSRR I _{SY}	$\begin{array}{c} V_S = 2.7 \; V \; to \; 6 \; V \\ -40^{\circ}C \leq T_A \leq +125^{\circ}C \\ V_O = 0 \; V \\ -40^{\circ}C \leq T_A \leq +125^{\circ}C \end{array}$	75 70	550	650	dB dB μA μA
DYNAMIC PERFORMANCE Slew Rate Full Power Bandwidth	SR BW _p	$R_L = 10 \text{ k}\Omega$ 1% Distortion		6.5		V/μs kHz
Settling Time Gain Bandwidth Product Phase Margin Channel Separation	t _S GBP Øo CS	To 0.01% $f = 1 \text{ kHz}, R_L = 10 \text{ k}\Omega$		4 75		μs MHz Degree: dB
NOISE PERFORMANCE Voltage Noise Voltage Noise Density Voltage Noise Density Current Noise Density	$\begin{array}{c} e_np\text{-}p\\ e_n\\ e_n\\ i_n \end{array}$	0.1 Hz to 10 Hz f = 1 kHz f = 10 kHz		55 35		$\mu V p-p \\ nV/\sqrt{Hz} \\ nV/\sqrt{Hz} \\ pA/\sqrt{Hz}$

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OP150/OP250/OP450

WAFER TEST LIMITS (@ $V_S = +5.0 \text{ V}$, $V_{CM} = 0 \text{ V}$, $T_A = +25 ^{\circ}\text{C}$ unless otherwise noted.)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V _{OS}		±10	mV max
Input Bias Current	$I_{\rm B}$		50	pA max
Input Offset Current	I_{OS}		10	pA max
Input Voltage Range	V_{CM}		V- to V+	V min
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0 \text{ V to } 10 \text{ V}$	60	dB min
Power Supply Rejection Ratio	PSRR	V = +2.7 V to +7 V	70	dB min
Large Signal Voltage Gain	A_{VO}	$R_L = 10 \text{ k}\Omega$		V/mV min
Output Voltage High	V_{OH}	$R_L = 2 k\Omega$ to GND	2.9	V min
Output Voltage Low	V_{OL}	$R_L = 2 k\Omega \text{ to } V +$	55	mV max
Supply Current/Amplifier	I_{SY}	$V_O = 0 V, R_L = \infty$	650	μA max

Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS ¹
Supply Voltage
Input Voltage
Differential Input Voltage 7 V
Output Short-Circuit Duration to GND ² \Indefinite
Storage Temperature Range
P, S, RT, RU Package65°C to +150°C
Operating Temperature Range
OP150/OP250/OP450G40°C to +125°C
Junction Temperature Range
P, S, RT, RU Package65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)+300°C

Package Type	θ_{JA}^{3}	$\theta_{ m JC}$	Units
5-Pin SOT (RT)	325		°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W
8-Pin TSSOP (RU)	240	43	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
14-Pin SOIC (S)	120	36	°C/W
14-Pin TSSOP(RU)	180	35	°C/W

ORD	ERING	GUIDE

Model	Temperature Range	Package Option
ØP1/50GS	-40°C to +125°C	8-Pin-SOIC
OP 150 GRT OP 150 GBC	-40°C to +125°C +25°C	5-Pin SOT DICE
OP250GP	7 40°C to +125°C	8-Pin Plastic DID
OP250GS	40°C to +125°C	8-Pin SOIC
OP250GRU	-40°C to +12/5°C	/8-Pfin TSSØP
OP250GBC	+25°C	DJCE
OP450GP	-40°C to +125°C	14-Pin Plastic DIP
OP450GS	-40°C to +125°C	14-Pin SOIC
OP450GRU	-40°C to +125°C	14-Pin TSSOP
OP450GBC	+25°C	DICE

NOTES

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP150/OP250/OP450 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



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¹Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

 $^{^2\}theta_{JA}$ is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

OP150/OP250/OP450

DICE CHARACTERISTICS

OP150 Die Size 0.00×0.00 Inch, 00 Sq. Mils Substrate (Die Backside) Is Connected to V-Transistor Count, 00.000. OP250 Die Size 0.044×0.045 Inch, 1,980 Sq. Mils Substrate (Die Backside) Is Connected to V-Transistor Count, 0.000. OP450 Die Size 0.052×0.058 Inch, 3,016 Sq. Mils Substrate (Die Backside) Is Connected to V-Transistor Count, 127.000.

