ANALOG DEVICES

Ultraprecision Operational Amplifier

OP177

FEATURES

Ultralow offset voltage
  T_A = 25°C, 25 μV maximum
Outstanding offset voltage drift 0.1 μV/°C maximum
Excellent open-loop gain and gain linearity
  12 V/μV typical
CMRR: 130 dB minimum
PSRR: 115 dB minimum
Low supply current 2.0 mA maximum
Fits industry-standard precision op amp sockets

PIN CONFIGURATION

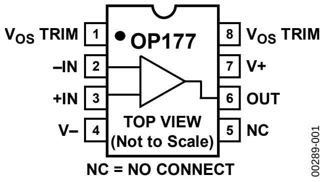


Figure 1. 8-Lead PDIP (P-Suffix), 8-Lead SOIC (S-Suffix)

GENERAL DESCRIPTION

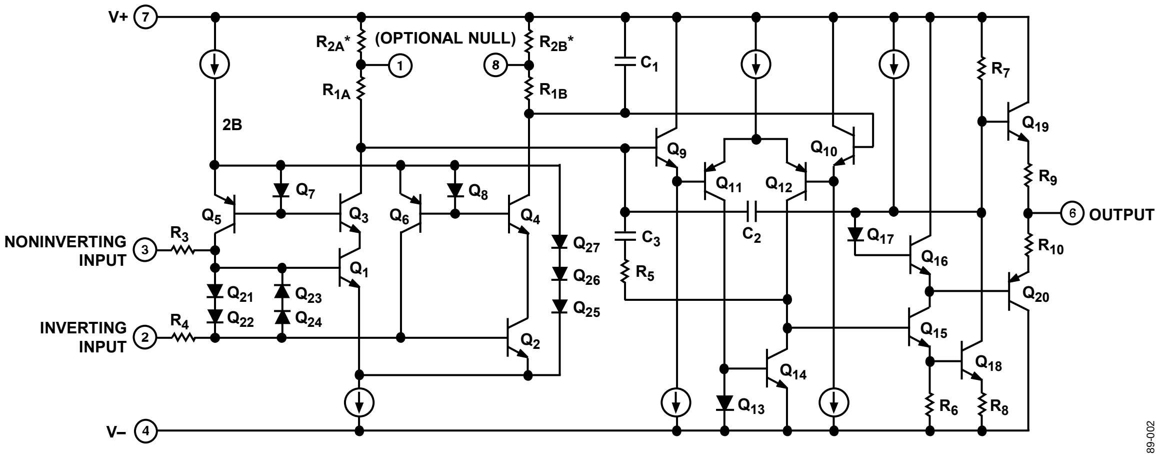
The OP177 features one of the highest precision performance of any op amp currently available. Offset voltage of the OP177 is only 25 μV maximum at room temperature. The ultralow V_{OS} of the OP177 combines with its exceptional offset voltage drift (TCV_{OS}) of 0.1 μV/°C maximum to eliminate the need for external V_{OS} adjustment and increases system accuracy over temperature.

The OP177 open-loop gain of 12 V/μV is maintained over the full ±10 V output range. CMRR of 130 dB minimum, PSRR of 120 dB minimum, and maximum supply current of 2 mA are just a few examples of the excellent performance of this operational amplifier. The combination of outstanding specifications of the OP177 ensures accurate performance in high closed-loop gain applications.

This low noise, bipolar input op amp is also a cost effective alternative to chopper-stabilized amplifiers. The OP177 provides chopper-type performance without the usual problems of high noise, low frequency chopper spikes, large physical size, limited common-mode input voltage range, and bulky external storage capacitors.

The OP177 is offered in the −40°C to +85°C extended industrial temperature ranges. This product is available in 8-lead PDIP, as well as the space saving 8-lead SOIC.

FUNCTIONAL BLOCK DIAGRAM



*R_{2A} AND R_{2B} ARE ELECTRONICALLY ADJUSTED ON CHIP AT FACTORY.

Figure 2. Simplified Schematic

Rev. E

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11/95—Rev. 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

@ V_S = ±15 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	OP177F Min	OP177F Typ	OP177F Max	OP177G Min	OP177G Typ	OP177G Max	Unit
INPUT OFFSET VOLTAGE	V_{OS}			10	25		20	60	µV
LONG-TERM INPUT OFFSET[1] Voltage Stability	ΔV_{OS}/time			0.3			0.4		µV/mo
INPUT OFFSET CURRENT	I_{OS}			0.3	1.5		0.3	2.8	nA
INPUT BIAS CURRENT	I_B		−0.2	+1.2	+2	−0.2	+1.2	+2.8	nA
INPUT NOISE VOLTAGE	e_n	f_O = 1 Hz to 100 Hz[2]		118	150		118	150	nV rms
INPUT NOISE CURRENT	i_n	f_O = 1 Hz to 100 Hz[2]		3	8		3	8	pA rms
INPUT RESISTANCE Differential Mode[3]	R_{IN}		26	45		18.5	45		MΩ
INPUT RESISTANCE COMMON MODE	R_{INCM}			200			200		GΩ
INPUT VOLTAGE RANGE[4]	IVR		±13	±14		±13	±14		V
COMMON-MODE REJECTION RATIO	CMRR	V_{CM} = ±13 V	130	140		115	140		dB
POWER SUPPLY REJECTION RATIO	PSRR	V_S = ±3 V to ±18 V	115	125		110	120		dB
LARGE SIGNAL VOLTAGE GAIN	A_{VO}	R_L ≥ 2 kΩ, V_O = ±10 V[5]	5000	12,000		2000	6000		V/mV
OUTPUT VOLTAGE SWING	V_O	R_L ≥ 10 kΩ	±13.5	±14.0		±13.5	±14.0		V
		R_L ≥ 2 kΩ	±12.5	±13.0		±12.5	±13.0		V
		R_L ≥ 1 kΩ	±12.0	±12.5		±12.0	±12.5		V
SLEW RATE[2]	SR	R_L ≥ 2 kΩ	0.1	0.3		0.1	0.3		V/µs
CLOSED-LOOP BANDWIDTH[2]	BW	A_{VCL} = 1	0.4	0.6		0.4	0.6		MHz
OPEN-LOOP OUTPUT RESISTANCE	R_O			60			60		Ω
POWER CONSUMPTION	P_D	V_S = ±15 V, no load		50	60		50	60	mW
		V_S = ±3 V, no load		3.5	4.5		3.5	4.5	mW
SUPPLY CURRENT	I_{SY}	V_S = ±15 V, no load		1.6	2		1.6	2	mA
OFFSET ADJUSTMENT RANGE		R_P = 20 kΩ		±3			±3		mV

[1] Long-term input offset voltage stability refers to the averaged trend line of V_{OS} vs. time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically less than 2.0 µV.

[2] Sample tested.

[3] Guaranteed by design.

[4] Guaranteed by CMRR test condition.

[5] To ensure high open-loop gain throughout the ±10 V output range, A_{VO} is tested at $-10\text{ V} \le V_O \le 0\text{ V}$, $0\text{ V} \le V_O \le +10\text{ V}$, and $-10\text{ V} \le V_O \le +10\text{ V}$.

@ V_S = ±15 V, −40°C ≤ T_A ≤ +85°C, unless otherwise noted.

Table 2.

			OP177F			OP177G			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
INPUT									
Input Offset Voltage	V_{OS}			15	40		20	100	μV
Average Input Offset Voltage Drift[1]	TCV_{OS}			0.1	0.3		0.7	1.2	μV/°C
Input Offset Current	I_{OS}			0.5	2.2		0.5	4.5	nA
Average Input Offset Current Drift[2]	TCI_{OS}			1.5	40		1.5	85	pA/°C
Input Bias Current	I_B		−0.2	+2.4	+4		+2.4	±6	nA
Average Input Bias Current Drift[2]	TCI_B			8	40		15	60	pA/°C
Input Voltage Range[3]	IVR		±13	±13.5		±13	±13.5		V
COMMON-MODE REJECTION RATIO	CMRR	V_{CM} = ±13 V	120	140		110	140		dB
POWER SUPPLY REJECTION RATIO	PSRR	V_S = ±3 V to ±18 V	110	120		106	115		dB
LARGE-SIGNAL VOLTAGE GAIN[4]	A_{VO}	R_L ≥ 2 kΩ, V_O = ±10 V	2000	6000		1000	4000		V/mV
OUTPUT VOLTAGE SWING	V_O	R_L ≥ 2 kΩ	±12	±13		±12	±13		V
POWER CONSUMPTION	P_D	V_S = ±15 V, no load		60	75		60	75	mW
SUPPLY CURRENT	I_{SY}	V_S = ±15 V, no load		2	2.5		2	2.5	mA

[1] TCV_{OS} is sample tested.
[2] Guaranteed by endpoint limits.
[3] Guaranteed by CMRR test condition.
[4] To ensure high open-loop gain throughout the ±10 V output range, A_{VO} is tested at −10 V ≤ V_O ≤ 0 V, 0 V ≤ V_O ≤ +10 V, and −10 V ≤ V_O ≤ +10 V.

TEST CIRCUITS

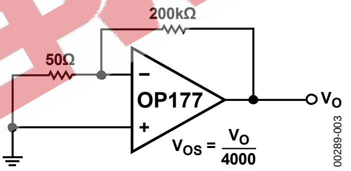


Figure 3. Typical Offset Voltage Test Circuit

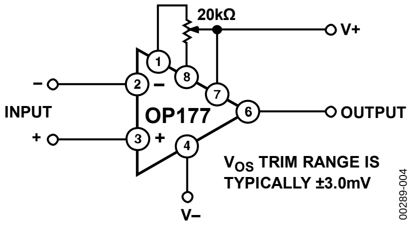


Figure 4. Optional Offset Nulling Circuit

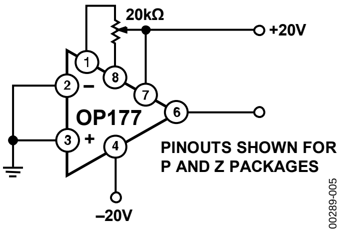


Figure 5. Burn-In Circuit

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Ratings
Supply Voltage	±22 V
Internal Power Dissipation[1]	500 mW
Differential Input Voltage	±30 V
Input Voltage	±22 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 60 sec)	300°C
DICE Junction Temperature (T_J)	−65°C to +150°C

[1] For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for worst-case mounting conditions, that is, θ_{JA} is specified for device in socket for PDIP; θ_{JA} is specified for device soldered to printed circuit board for SOIC package.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead PDIP (P-Suffix)	103	43	°C/W
8-Lead SOIC (S-Suffix)	158	43	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

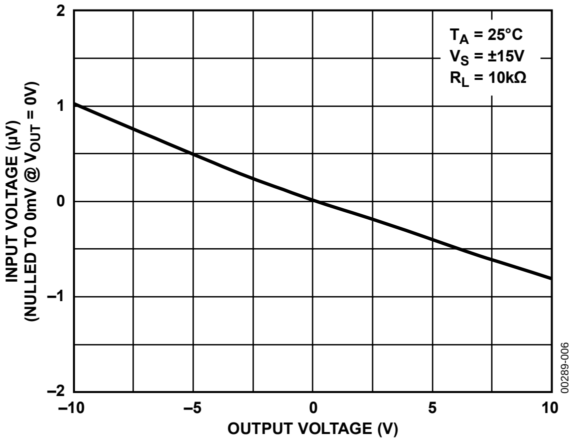


Figure 6. Gain Linearity (Input Voltage vs. Output Voltage)

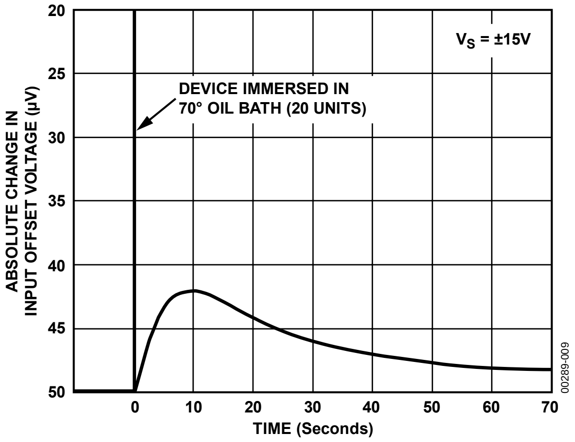


Figure 9. Offset Voltage Change Due to Thermal Shock

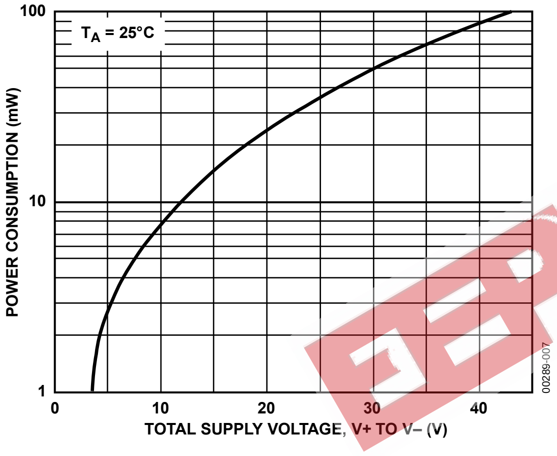


Figure 7. Power Consumption vs. Power Supply

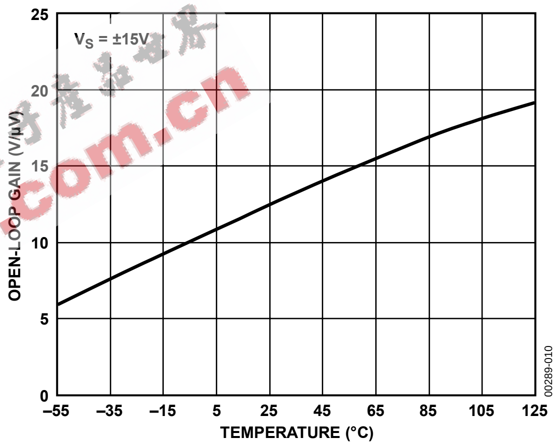


Figure 10. Open-Loop Gain vs. Temperature

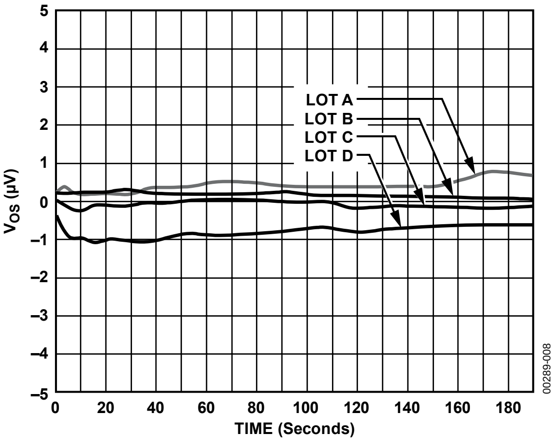


Figure 8. Warm-Up V_{OS} Drift (Normalized) Z Package

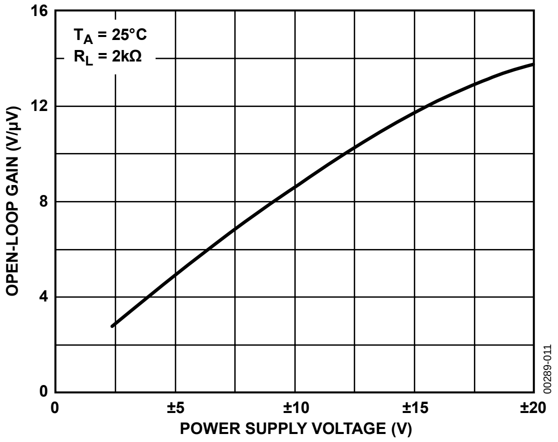


Figure 11. Open-Loop Gain vs. Power Supply Voltage

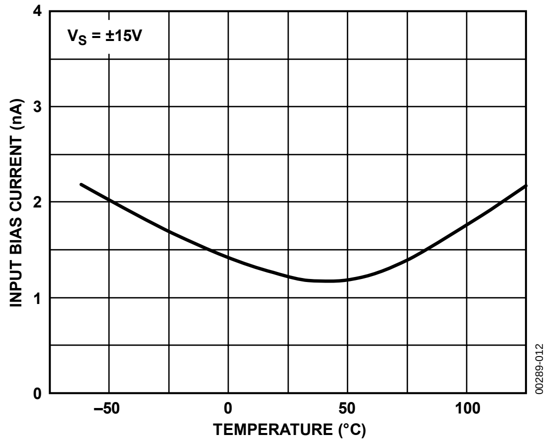


Figure 12. Input Bias Current vs. Temperature

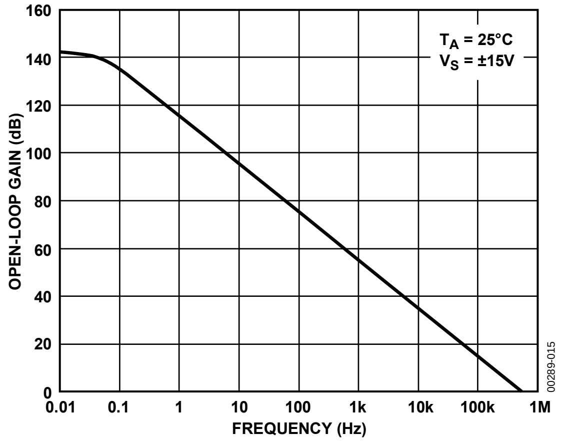


Figure 15. Open-Loop Frequency Response

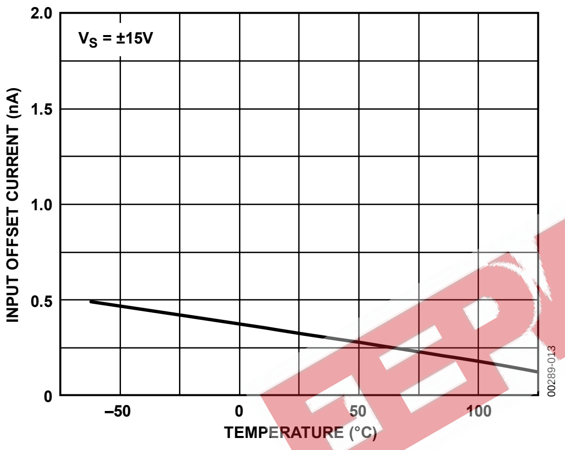


Figure 13. Input Offset Current vs. Temperature

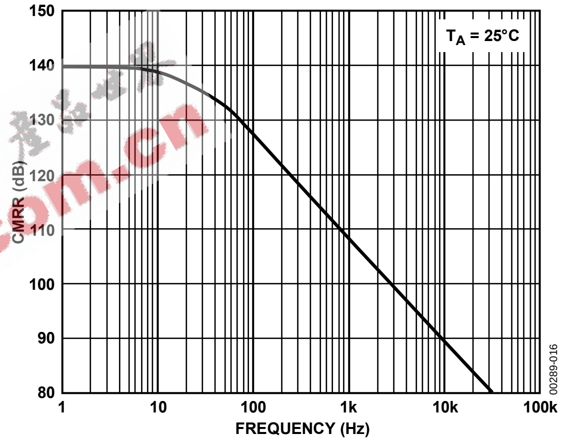


Figure 16. CMRR vs. Frequency

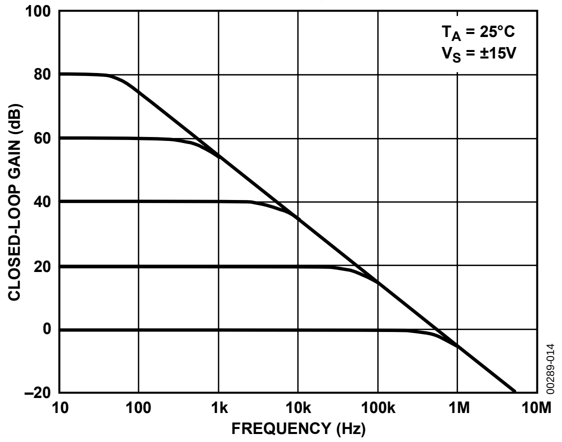


Figure 14. Closed-Loop Response for Various Gain Configurations

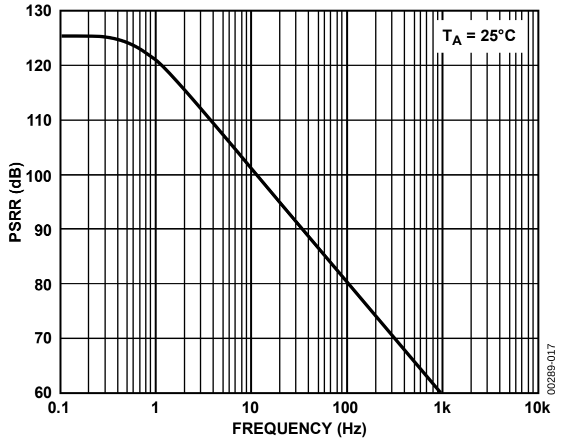


Figure 17. PSRR vs. Frequency

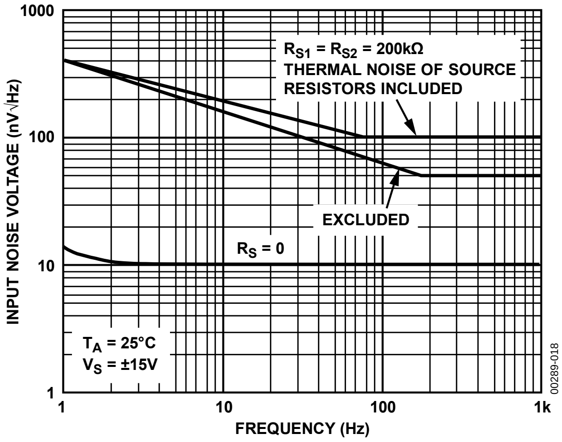


Figure 18. Total Input Noise Voltage vs. Frequency

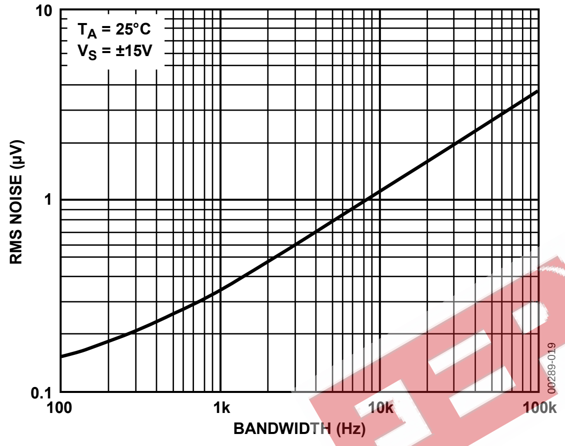


Figure 19. Input Wideband Noise vs. Bandwidth (0.1 Hz to Frequency Indicated)

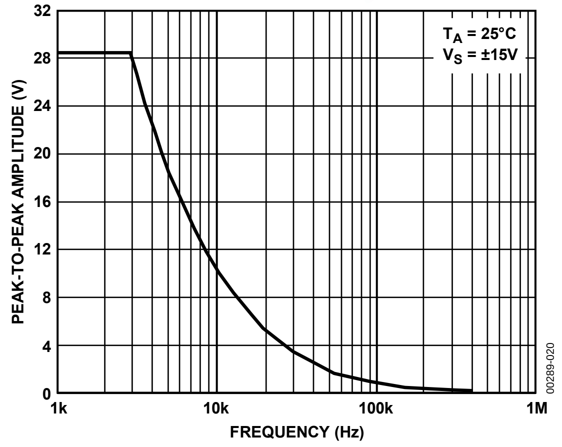


Figure 20. Maximum Output Swing vs. Frequency

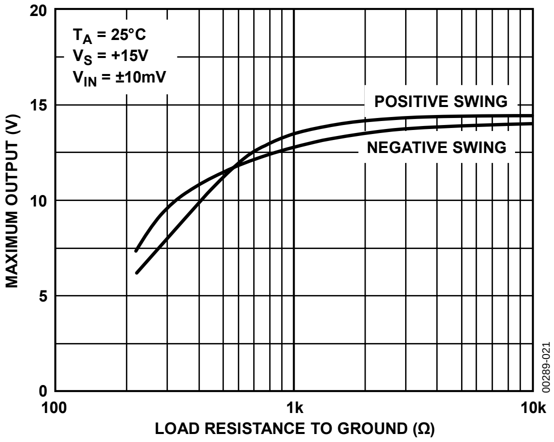


Figure 21. Maximum Output Voltage vs. Load Resistance

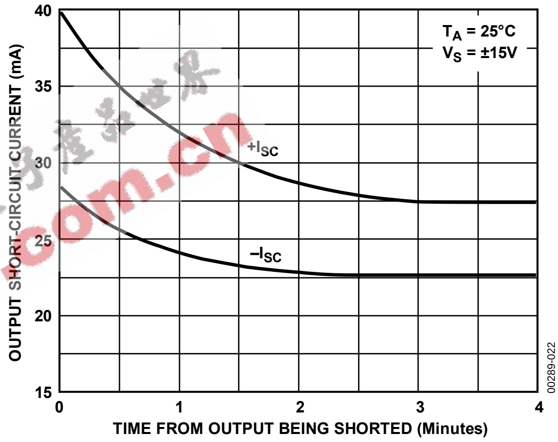


Figure 22. Output Short-Circuit Current vs. Time

APPLICATION INFORMATION

GAIN LINEARITY

The actual open-loop gain of most monolithic op amps varies at different output voltages. This nonlinearity causes errors in high closed-loop gain circuits.

It is important to know that the manufacturer's A_{VO} specification is only a part of the solution because all automated testers use endpoint testing and, therefore, show only the average gain. For example, Figure 23 shows a typical precision op amp with a respectable open-loop gain of 650 V/mV. However, the gain is not constant through the output voltage range, causing nonlinear errors. An ideal op amp shows a horizontal scope trace.

Figure 24 shows the OP177 output gain linearity trace with its truly impressive average A_{VO} of 12,000 V/mV. The output trace is virtually horizontal at all points, assuring extremely high gain accuracy. Analog Devices also performs additional testing to ensure consistent high open-loop gain at various output voltages. Figure 25 is a simple open-loop gain test circuit.

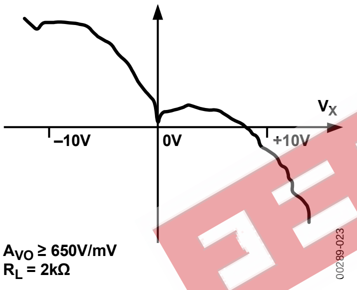


Figure 23. Typical Precision Op Amp

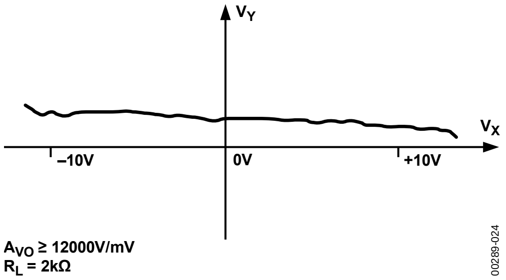


Figure 24. Output Gain Linearity Trace

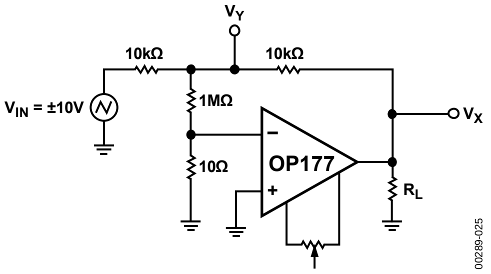


Figure 25. Open-Loop Gain Linearity Test Circuit

THERMOCOUPLE AMPLIFIER WITH COLD-JUNCTION COMPENSATION

An example of a precision circuit is a thermocouple amplifier that must accurately amplify very low level signals without introducing linearity and offset errors to the circuit. In this circuit, an S-type thermocouple with a Seebeck coefficient of 10.3 µV/°C produces 10.3 mV of output voltage at a temperature of 1000°C. The amplifier gain is set at 973.16, thus, it produces an output voltage of 10.024 V. Extended temperature ranges beyond 1500°C are accomplished by reducing the amplifier gain. The circuit uses a low cost diode to sense the temperature at the terminating junctions and, in turn, compensates for any ambient temperature change. The OP177, with its high open-loop gain plus low offset voltage and drift, combines to yield a precise temperature sensing circuit. Circuit values for other thermocouple types are listed in Table 5.

Table 5.

Thermocouple Type	Seebeck Coefficient	R1	R2	R7	R9
K	39.2 µV/°C	110 Ω	5.76 kΩ	102 kΩ	269 kΩ
J	50.2 µV/°C	100 Ω	4.02 kΩ	80.6 kΩ	200 kΩ
S	10.3 µV/°C	100 Ω	20.5 kΩ	392 kΩ	1.07 MΩ

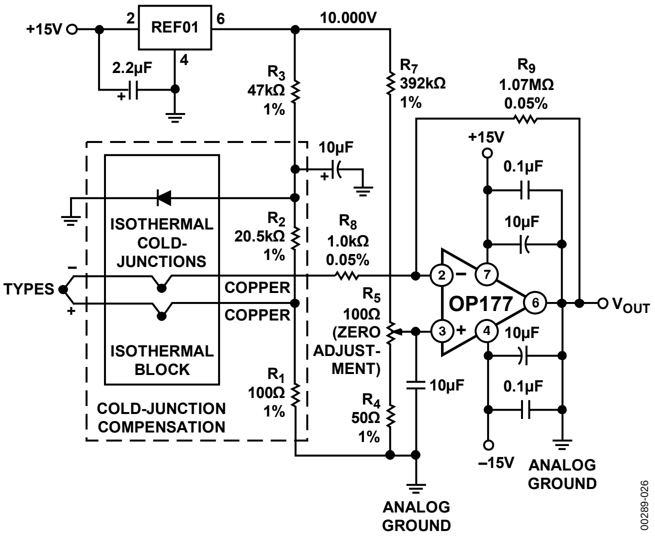


Figure 26. Thermocouple Amplifier with Cold Junction Compensation

PRECISION HIGH GAIN DIFFERENTIAL AMPLIFIER

The high gain, gain linearity, CMRR, and low TCV_{OS} of the OP177 make it possible to obtain performance not previously available in single stage, very high gain amplifier applications. See Figure 27.

For best CMR, $\frac{R1}{R2}$ must equal $\frac{R3}{R4}$

In this example, with a 10 mV differential signal, the maximum errors are listed in Table 6.

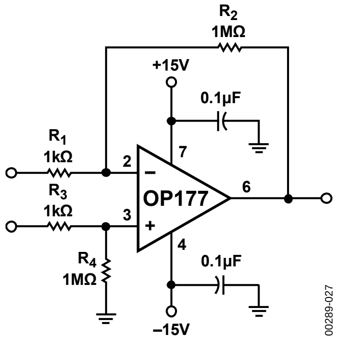


Figure 27. Precision High Gain Differential Amplifier

Table 6. High Gain Differential Amp Performance

Type	Amount
Common-Mode Voltage	0.1%/V
Gain Linearity, Worst Case	0.02%
TCV_{OS}	0.0003%/°C
TCI_{OS}	0.008%/°C

ISOLATING LARGE CAPACITIVE LOADS

The circuit shown in Figure 28 reduces maximum slew rate but allows driving capacitive loads of any size without instability. Because the 100 Ω resistor is inside the feedback loop, its effect on output impedance is reduced to insignificance by the high open loop gain of the OP177.

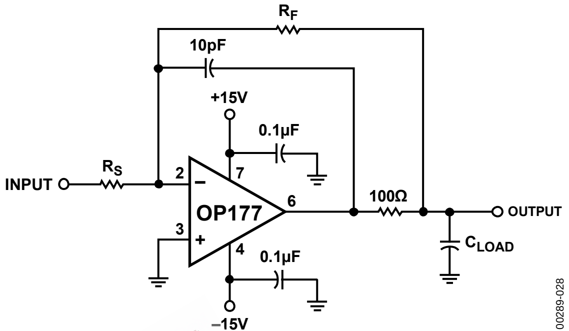


Figure 28. Isolating Capacitive Loads

BILATERAL CURRENT SOURCE

The current sources shown in Figure 29 supply both positive and negative currents into a grounded load.

Note that

$$Z_O = \frac{R5\left(\frac{R4}{R2}+1\right)}{\frac{R5+R4}{R2}-\frac{R3}{R1}}$$

and that for Z_O to be infinite

$$\frac{R5+R4}{R2}\ must = \frac{R3}{R1}$$

PRECISION ABSOLUTE VALUE AMPLIFIER

The high gain and low TCV_{OS} assure accurate operation with inputs from microvolts to volts. In this circuit, the signal always appears as a common-mode signal to the op amps (for details, see Figure 30).

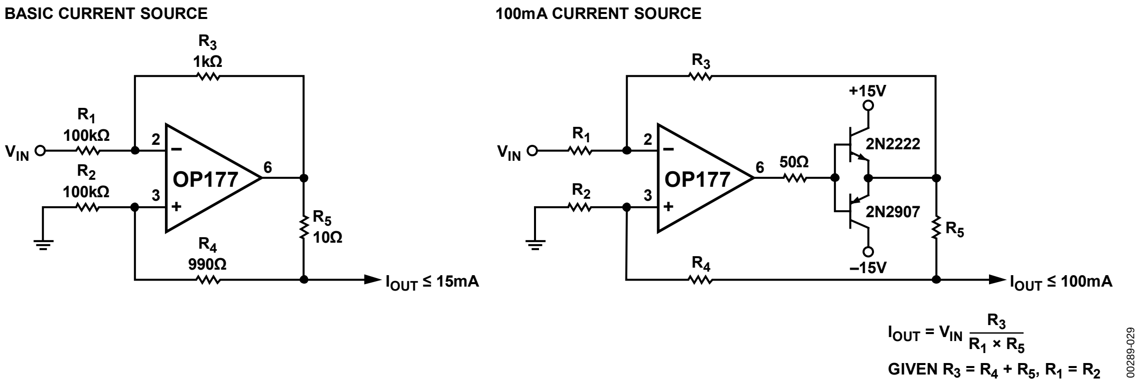


Figure 29. Bilateral Current Source

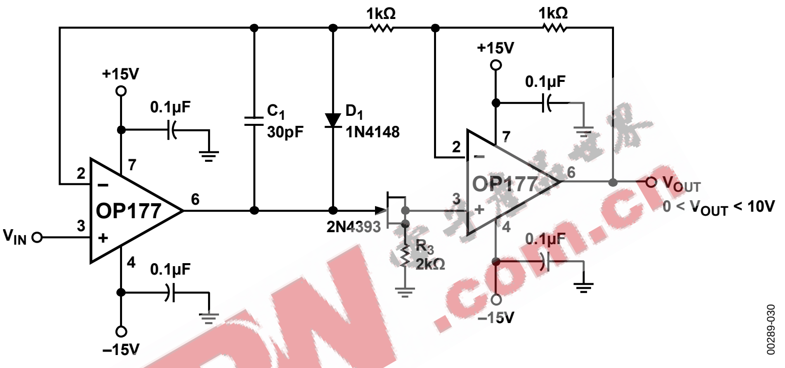


Figure 30. Precision Absolute Value Amplifier

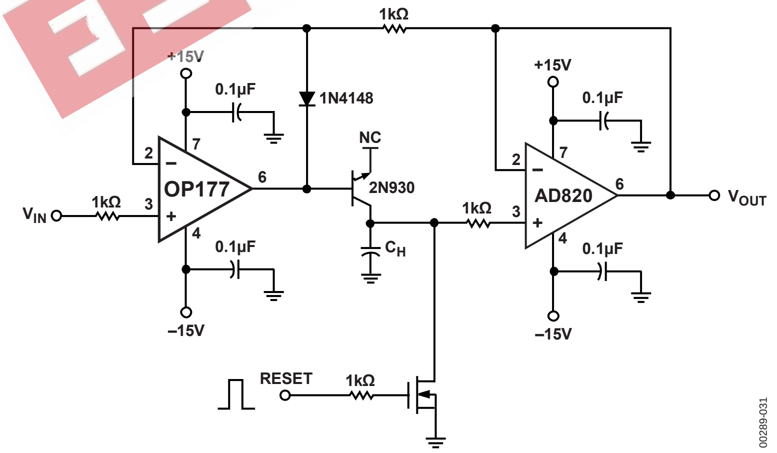


Figure 31. Precision Positive Peak Detector

PRECISION POSITIVE PEAK DETECTOR

In Figure 31, C_H must be polystyrene, Teflon®, or polyethylene to minimize dielectric absorption and leakage. The droop rate is determined by the size of C_H and the bias current of the AD820.

PRECISION THRESHOLD DETECTOR/AMPLIFIER

In Figure 32, when $V_{IN} < V_{TH}$, amplifier output swings negative, reverse biasing diode D_1. $V_{OUT} = V_{TH}$ if $R_L = \infty$. When $V_{IN} \geq V_{TH}$, the loop closes.

$$V_{OUT} = V_{TH} + (V_{IN} - V_{TH})\left(1 + \frac{R_F}{R_S}\right)$$

C_C is selected to smooth the response of the loop.

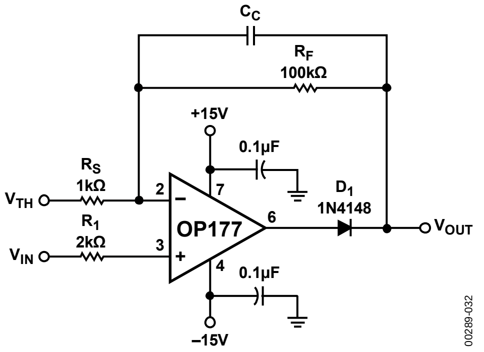
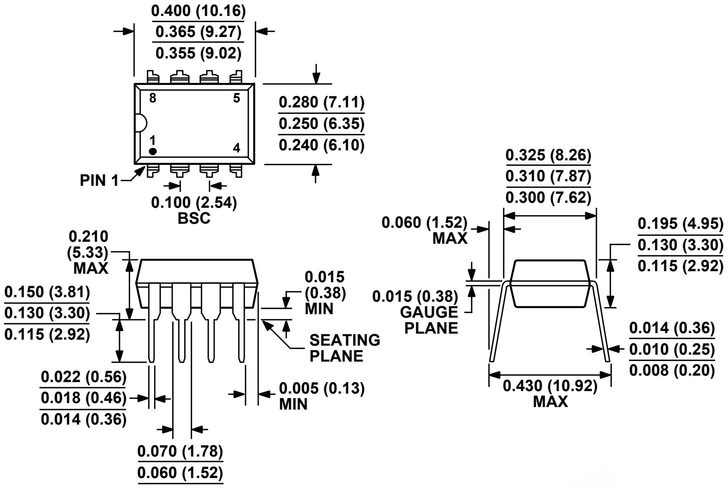


Figure 32. Precision Threshold Detector/Amplifier

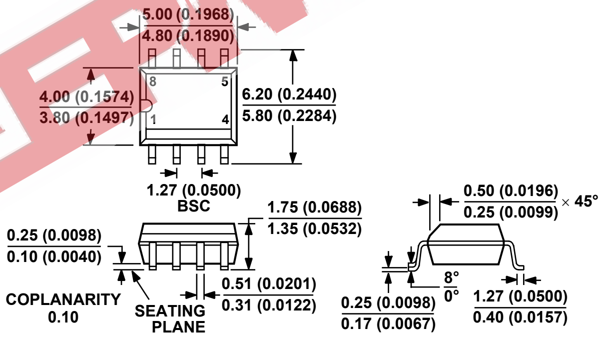
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001-BA

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 33. 8-Lead Plastic Dual In-Line Package (PDIP)
P-Suffix
(N-8)
Dimensions show in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 34. 8-Lead Standard Small Outline Package (SOIC_N)
S-Suffix
(R-8)
Dimensions shown in millimeters and(inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP177FP	−40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)
OP177FPZ[1]	−40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)
OP177GP	−40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)
OP177GPZ[1]	−40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)
OP177FS	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)
OP177FS-REEL	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)
OP177FS-REEL7	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)
OP177FSZ[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)
OP177FSZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)
OP177FSZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)
OP177GS	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)
OP177GS-REEL	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)
OP177GS-REEL7	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)
OP177GSZ[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)
OP177GSZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)
OP177GSZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)

[1] Z = Pb-free part.

NOTES

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