

### FEATURES

#### Ultralow offset voltage

$T_A = 25^\circ\text{C}$ , 25  $\mu\text{V}$  maximum

#### Outstanding offset voltage drift 0.1 $\mu\text{V}/^\circ\text{C}$ maximum

#### Excellent open-loop gain and gain linearity

12  $\text{V}/\mu\text{V}$  typical

#### CMRR: 130 dB minimum

#### PSRR: 115 dB minimum

#### Low supply current 2.0 mA maximum

#### Fits industry-standard precision op amp sockets

### GENERAL DESCRIPTION

The OP177 features one of the highest precision performance of any op amp currently available. Offset voltage of the OP177 is only 25  $\mu\text{V}$  maximum at room temperature. The ultralow  $V_{OS}$  of the OP177 combines with its exceptional offset voltage drift ( $\text{TCV}_{OS}$ ) of 0.1  $\mu\text{V}/^\circ\text{C}$  maximum to eliminate the need for external  $V_{OS}$  adjustment and increases system accuracy over temperature.

The OP177 open-loop gain of 12  $\text{V}/\mu\text{V}$  is maintained over the full  $\pm 10 \text{ V}$  output range. CMRR of 130 dB minimum, PSRR of 120 dB minimum, and maximum supply current of 2 mA are just a few examples of the excellent performance of this

operational amplifier. The combination of outstanding specifications of the OP177 ensures accurate performance in high closed-loop gain applications.

This low noise, bipolar input op amp is also a cost effective alternative to chopper-stabilized amplifiers. The OP177 provides chopper-type performance without the usual problems of high noise, low frequency chopper spikes, large physical size, limited common-mode input voltage range, and bulky external storage capacitors.

The OP177 is offered in the  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  extended industrial temperature ranges. This product is available in 8-lead PDIP, as well as the space saving 8-lead SOIC.

### PIN CONFIGURATION

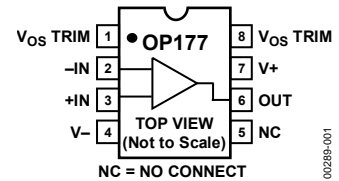
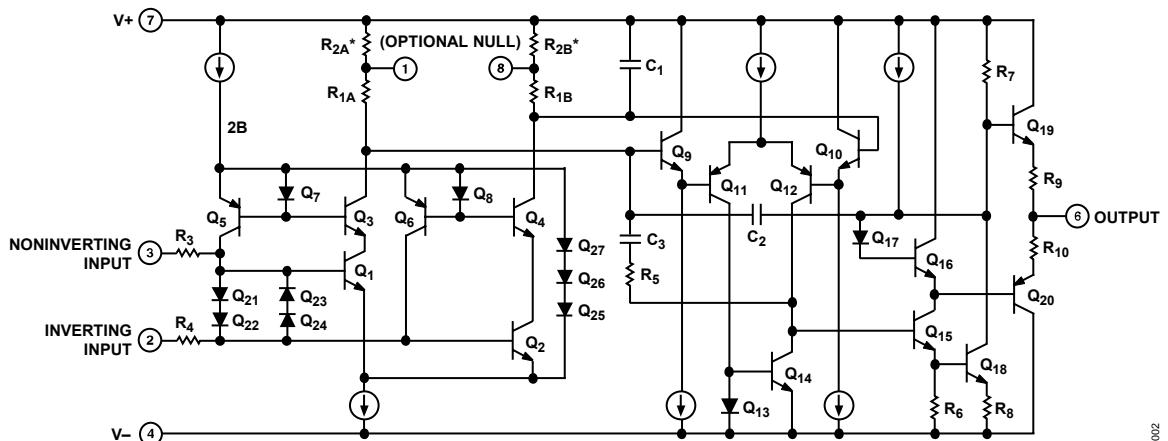


Figure 1. 8-Lead PDIP (P-Suffix),  
8-Lead SOIC (S-Suffix)

### FUNCTIONAL BLOCK DIAGRAM



\* $R_{2A}$  AND  $R_{2B}$  ARE ELECTRONICALLY ADJUSTED ON CHIP AT FACTORY.

Figure 2. Simplified Schematic

#### Rev. E

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**REVISION HISTORY**

**5/06—Rev. D to Rev. E**

Changes to Figure 1 .....	1
Change to Specifications Table 1 .....	3
Changes to Specifications Table 2.....	4
Changes to Table 3.....	5
Changes to Figure 23 and Figure 24.....	9
Changes to Figure 32.....	12
Updated the Ordering Guide .....	14

**4/06—Rev. C to Rev. D**

Change to Pin Configuration Caption.....	1
Changes to Features.....	1
Change to Table 2 .....	4
Change to Figure 2 .....	4
Changes to Figure 10 and Figure 11.....	6
Changes to Figure 12 through Figure 17 .....	7
Changes to Figure 18 through Figure 22 .....	8

Change to Figure 27 .....	10
Changes to Figure 30 and Figure 31.....	11
Updated Outline Dimensions.....	13
Changes to Ordering Guide.....	13

**1/05—Rev. B to Rev. C**

Edits to Features.....	1
Edits to General Description .....	1
Edits to Pin Connections.....	1
Edits to Electrical Characteristics .....	2, 3
Global deletion of references to OP177E .....	3, 4, 10
Edits to Absolute Maximum Ratings.....	5
Edits to Package Type .....	5
Edits to Ordering Guide .....	5
Edit to Outline Dimensions .....	11

**11/95—Rev. 0: Initial Version**

## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS

@  $V_S = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	OP177F			OP177G			Unit
			Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE	$V_{OS}$		10	25		20	60	$\mu\text{V}$	
LONG-TERM INPUT OFFSET <sup>1</sup> Voltage Stability	$\Delta V_{OS}/\text{time}$		0.3			0.4		$\mu\text{V}/\text{mo}$	
INPUT OFFSET CURRENT	$I_{OS}$		0.3	1.5		0.3	2.8	nA	
INPUT BIAS CURRENT	$I_B$		-0.2	+1.2	+2	-0.2	+1.2	+2.8	nA
INPUT NOISE VOLTAGE	$e_n$	$f_0 = 1\text{ Hz to }100\text{ Hz}^2$	118	150		118	150	nV rms	
INPUT NOISE CURRENT	$i_n$	$f_0 = 1\text{ Hz to }100\text{ Hz}^2$	3	8		3	8	pA rms	
INPUT RESISTANCE Differential Mode <sup>3</sup>	$R_{IN}$		26	45		18.5	45	M $\Omega$	
INPUT RESISTANCE COMMON MODE	$R_{INCM}$			200			200	G $\Omega$	
INPUT VOLTAGE RANGE <sup>4</sup>	IVR		$\pm 13$	$\pm 14$		$\pm 13$	$\pm 14$	V	
COMMON-MODE REJECTION RATIO	CMRR	$V_{CM} = \pm 13\text{ V}$	130	140		115	140	dB	
POWER SUPPLY REJECTION RATIO	PSRR	$V_S = \pm 3\text{ V to } \pm 18\text{ V}$	115	125		110	120	dB	
LARGE SIGNAL VOLTAGE GAIN	$A_{VO}$	$R_L \geq 2\text{ k}\Omega$ , $V_O = \pm 10\text{ V}^5$	5000	12,000		2000	6000	V/mV	
OUTPUT VOLTAGE SWING	$V_O$	$R_L \geq 10\text{ k}\Omega$	$\pm 13.5$	$\pm 14.0$		$\pm 13.5$	$\pm 14.0$	V	
		$R_L \geq 2\text{ k}\Omega$	$\pm 12.5$	$\pm 13.0$		$\pm 12.5$	$\pm 13.0$	V	
		$R_L \geq 1\text{ k}\Omega$	$\pm 12.0$	$\pm 12.5$		$\pm 12.0$	$\pm 12.5$	V	
SLEW RATE <sup>2</sup>	SR	$R_L \geq 2\text{ k}\Omega$	0.1	0.3		0.1	0.3	V/ $\mu\text{s}$	
CLOSED-LOOP BANDWIDTH <sup>2</sup>	BW	$A_{VCL} = 1$	0.4	0.6		0.4	0.6	MHz	
OPEN-LOOP OUTPUT RESISTANCE	$R_O$		60			60		$\Omega$	
POWER CONSUMPTION	$P_D$	$V_S = \pm 15\text{ V}$ , no load	50	60		50	60	mW	
		$V_S = \pm 3\text{ V}$ , no load	3.5	4.5		3.5	4.5	mW	
SUPPLY CURRENT	$I_{SY}$	$V_S = \pm 15\text{ V}$ , no load	1.6	2		1.6	2	mA	
OFFSET ADJUSTMENT RANGE		$R_P = 20\text{ k}\Omega$	$\pm 3$			$\pm 3$		mV	

<sup>1</sup> Long-term input offset voltage stability refers to the averaged trend line of  $V_{OS}$  vs. time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in  $V_{OS}$  during the first 30 operating days are typically less than  $2.0\ \mu\text{V}$ .

<sup>2</sup> Sample tested.

<sup>3</sup> Guaranteed by design.

<sup>4</sup> Guaranteed by CMRR test condition.

<sup>5</sup> To ensure high open-loop gain throughout the  $\pm 10\text{ V}$  output range,  $A_{VO}$  is tested at  $-10\text{ V} \leq V_O \leq 0\text{ V}$ ,  $0\text{ V} \leq V_O \leq +10\text{ V}$ , and  $-10\text{ V} \leq V_O \leq +10\text{ V}$ .

# OP177

@  $V_S = \pm 15\text{ V}$ ,  $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ , unless otherwise noted.

**Table 2.**

Parameter	Symbol	Conditions	OP177F			OP177G			Unit
			Min	Typ	Max	Min	Typ	Max	
INPUT									
Input Offset Voltage	$V_{OS}$			15	40		20	100	$\mu\text{V}$
Average Input Offset Voltage Drift <sup>1</sup>	$\text{TCV}_{OS}$			0.1	0.3		0.7	1.2	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	$I_{OS}$			0.5	2.2		0.5	4.5	nA
Average Input Offset Current Drift <sup>2</sup>	$\text{TCI}_{OS}$			1.5	40		1.5	85	$\text{pA}/^\circ\text{C}$
Input Bias Current	$I_B$		-0.2	+2.4	+4		+2.4	$\pm 6$	nA
Average Input Bias Current Drift <sup>2</sup>	$\text{TCI}_B$			8	40		15	60	$\text{pA}/^\circ\text{C}$
Input Voltage Range <sup>3</sup>	IVR		$\pm 13$	$\pm 13.5$		$\pm 13$	$\pm 13.5$		V
COMMON-MODE REJECTION RATIO	CMRR	$V_{CM} = \pm 13\text{ V}$	120	140		110	140		dB
POWER SUPPLY REJECTION RATIO	PSRR	$V_S = \pm 3\text{ V}$ to $\pm 18\text{ V}$	110	120		106	115		dB
LARGE-SIGNAL VOLTAGE GAIN <sup>4</sup>	$A_{VO}$	$R_L \geq 2\text{ k}\Omega$ , $V_O = \pm 10\text{ V}$	2000	6000		1000	4000		V/mV
OUTPUT VOLTAGE SWING	$V_O$	$R_L \geq 2\text{ k}\Omega$	$\pm 12$	$\pm 13$		$\pm 12$	$\pm 13$		V
POWER CONSUMPTION	$P_D$	$V_S = \pm 15\text{ V}$ , no load		60	75		60	75	mW
SUPPLY CURRENT	$I_S$	$V_S = \pm 15\text{ V}$ , no load		20	2.5		2	2.5	mA

<sup>1</sup>  $\text{TCV}_{OS}$  is sample tested.

<sup>2</sup> Guaranteed by endpoint limits.

<sup>3</sup> Guaranteed by CMRR test condition.

<sup>4</sup> To ensure high open-loop gain throughout the  $\pm 10\text{ V}$  output range,  $A_{VO}$  is tested at  $-10\text{ V} \leq V_O \leq 0\text{ V}$ ,  $0\text{ V} \leq V_O \leq +10\text{ V}$ , and  $-10\text{ V} \leq V_O \leq +10\text{ V}$ .

## TEST CIRCUITS

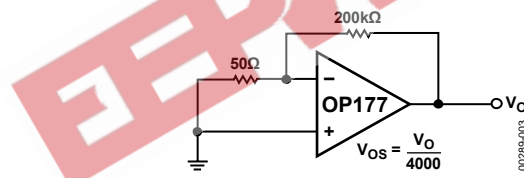


Figure 3. Typical Offset Voltage Test Circuit

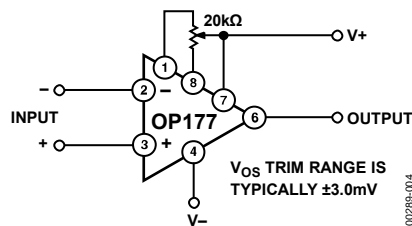


Figure 4. Optional Offset Nulling Circuit

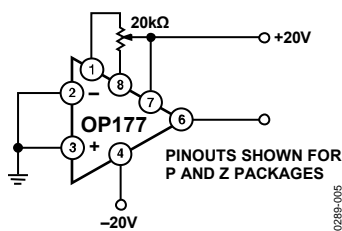


Figure 5. Burn-In Circuit

## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Ratings
Supply Voltage	±22 V
Internal Power Dissipation <sup>1</sup>	500 mW
Differential Input Voltage	±30 V
Input Voltage	±22 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 60 sec)	300°C
DICE Junction Temperature (T <sub>J</sub> )	−65°C to +150°C

<sup>1</sup> For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### THERMAL RESISTANCE

$\theta_{JA}$  is specified for worst-case mounting conditions, that is,  $\theta_{JA}$  is specified for device in socket for PDIP;  $\theta_{JA}$  is specified for device soldered to printed circuit board for SOIC package.

Table 4. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
8-Lead PDIP (P-Suffix)	103	43	°C/W
8-Lead SOIC (S-Suffix)	158	43	°C/W

### ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TYPICAL PERFORMANCE CHARACTERISTICS

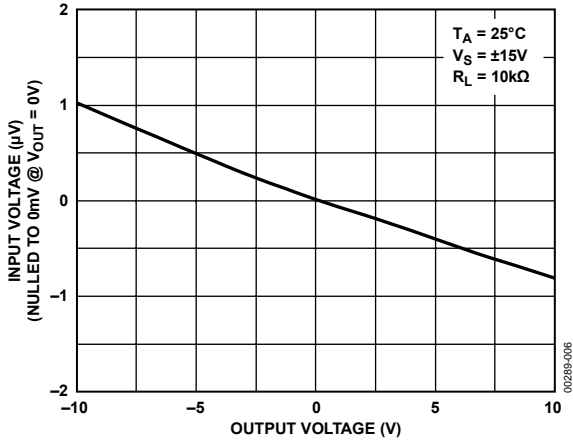


Figure 6. Gain Linearity (Input Voltage vs. Output Voltage)

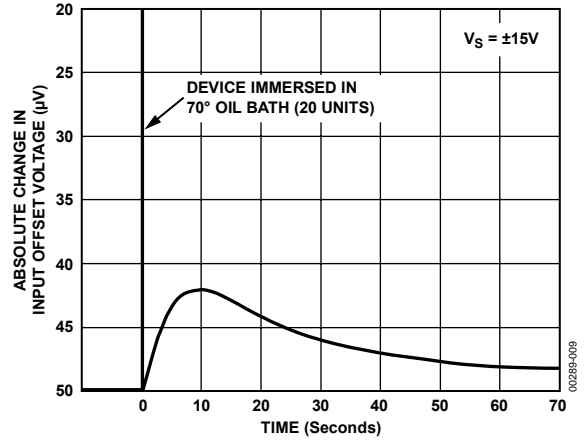


Figure 9. Offset Voltage Change Due to Thermal Shock

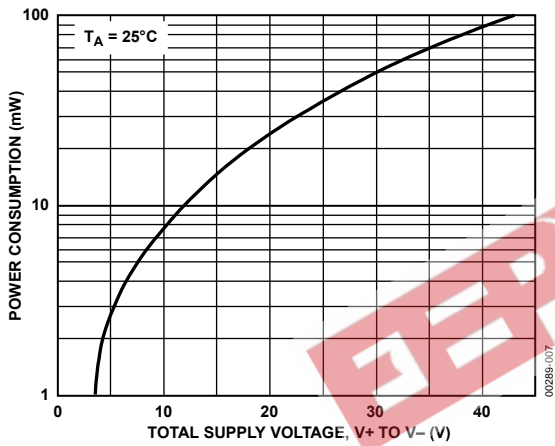


Figure 7. Power Consumption vs. Power Supply

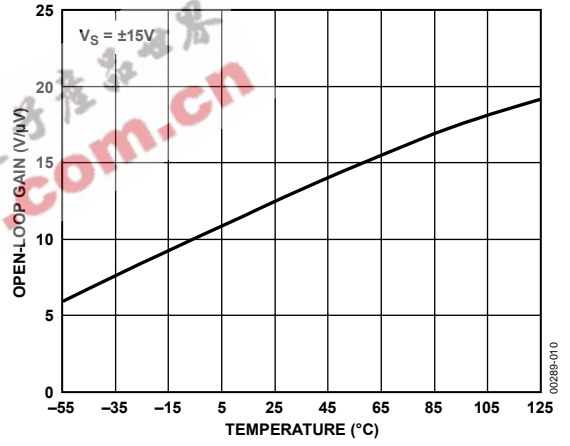


Figure 10. Open-Loop Gain vs. Temperature

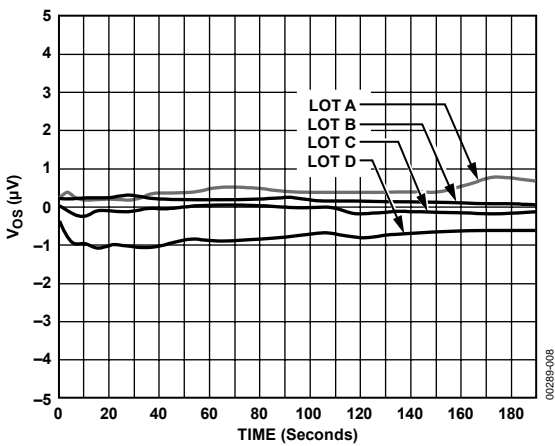


Figure 8. Warm-Up  $V_{OS}$  Drift (Normalized) Z Package

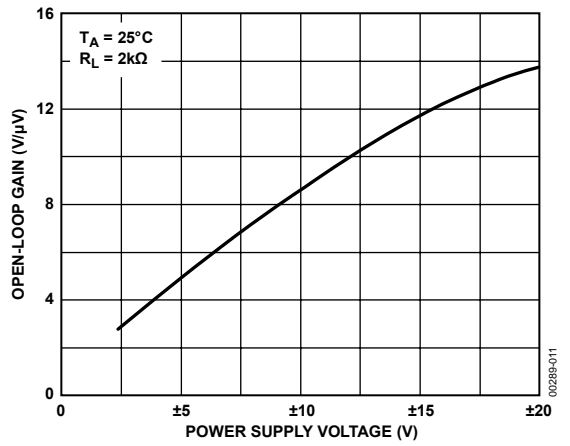


Figure 11. Open-Loop Gain vs. Power Supply Voltage

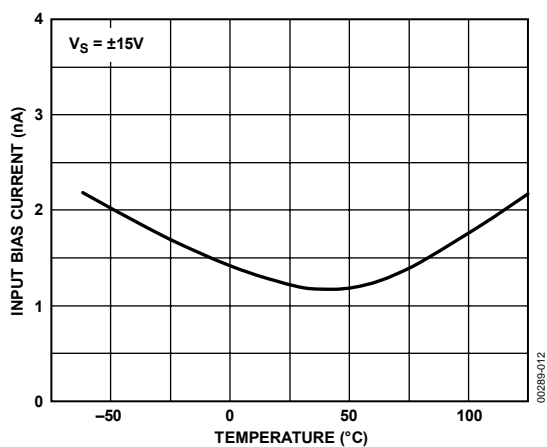


Figure 12. Input Bias Current vs. Temperature

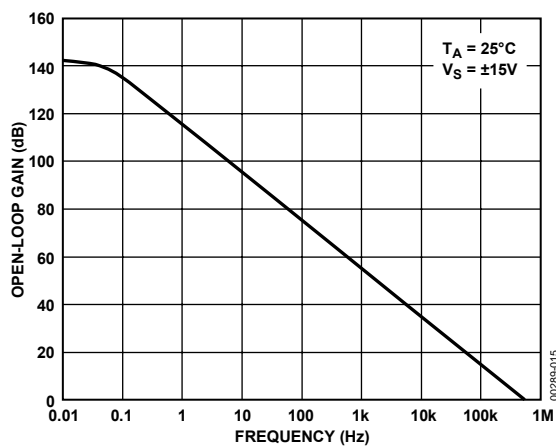


Figure 15. Open-Loop Frequency Response

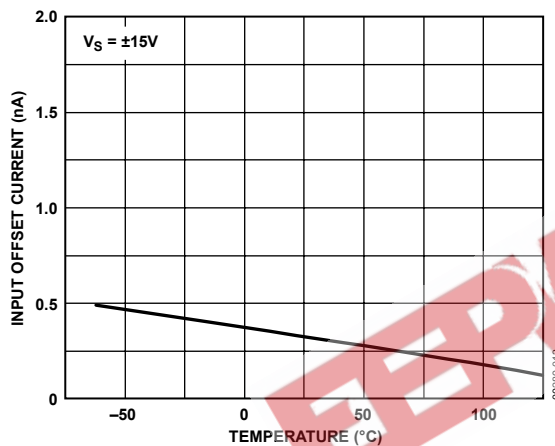


Figure 13. Input Offset Current vs. Temperature

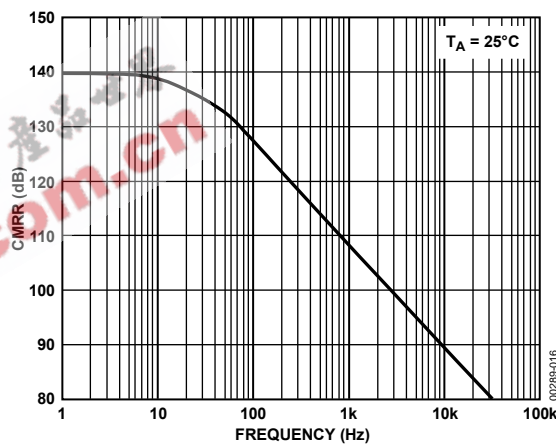


Figure 16. CMRR vs. Frequency

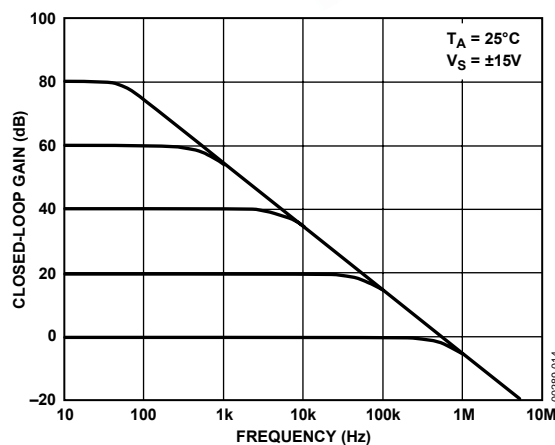


Figure 14. Closed-Loop Response for Various Gain Configurations

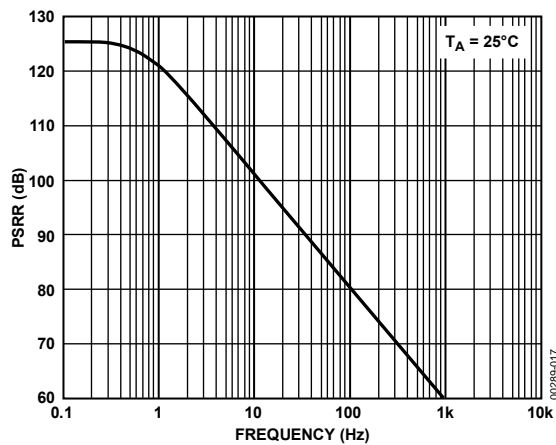


Figure 17. PSRR vs. Frequency

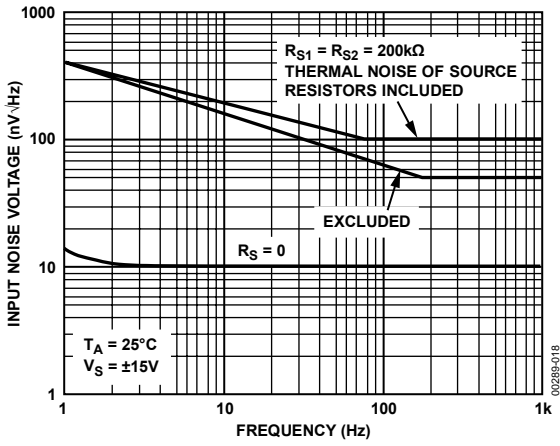


Figure 18. Total Input Noise Voltage vs. Frequency

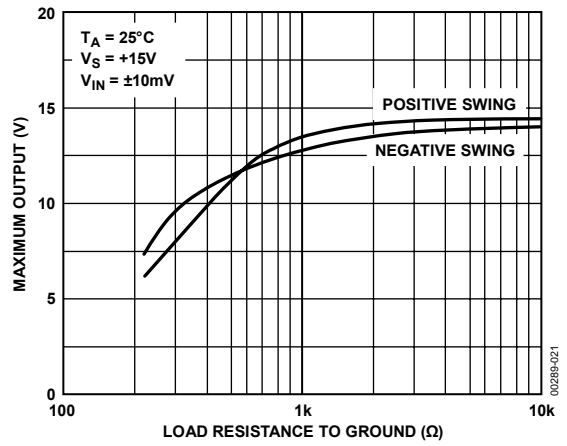


Figure 21. Maximum Output Voltage vs. Load Resistance

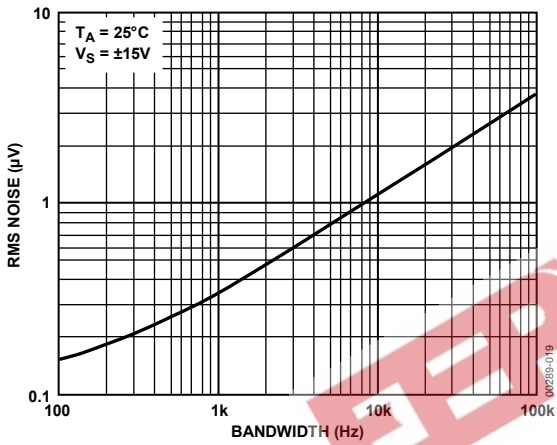


Figure 19. Input Wideband Noise vs. Bandwidth (0.1 Hz to Frequency Indicated)

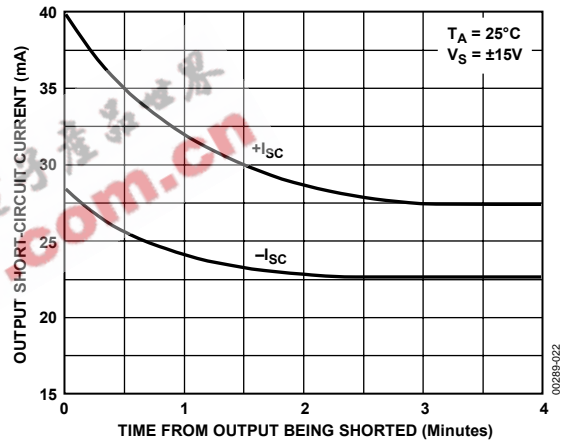


Figure 22. Output Short-Circuit Current vs. Time

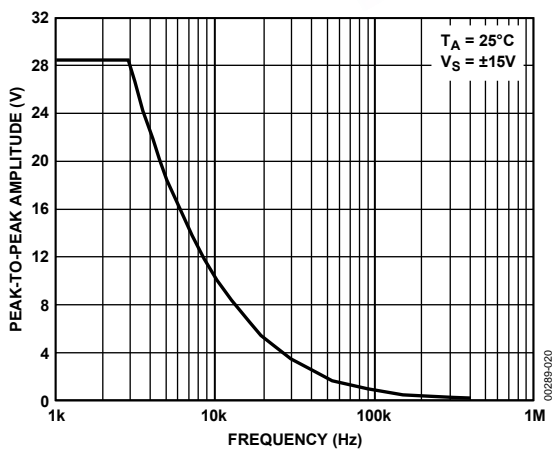


Figure 20. Maximum Output Swing vs. Frequency



## APPLICATION INFORMATION

### GAIN LINEARITY

The actual open-loop gain of most monolithic op amps varies at different output voltages. This nonlinearity causes errors in high closed-loop gain circuits.

It is important to know that the manufacturer's  $A_{VO}$  specification is only a part of the solution because all automated testers use endpoint testing and, therefore, show only the average gain. For example, Figure 23 shows a typical precision op amp with a respectable open-loop gain of 650 V/mV. However, the gain is not constant through the output voltage range, causing non-linear errors. An ideal op amp shows a horizontal scope trace.

Figure 24 shows the OP177 output gain linearity trace with its truly impressive average  $A_{VO}$  of 12,000 V/mV. The output trace is virtually horizontal at all points, assuring extremely high gain accuracy. Analog Devices also performs additional testing to ensure consistent high open-loop gain at various output voltages. Figure 25 is a simple open-loop gain test circuit.

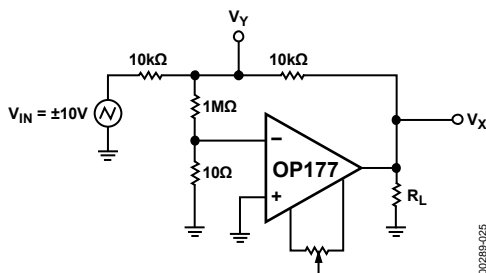
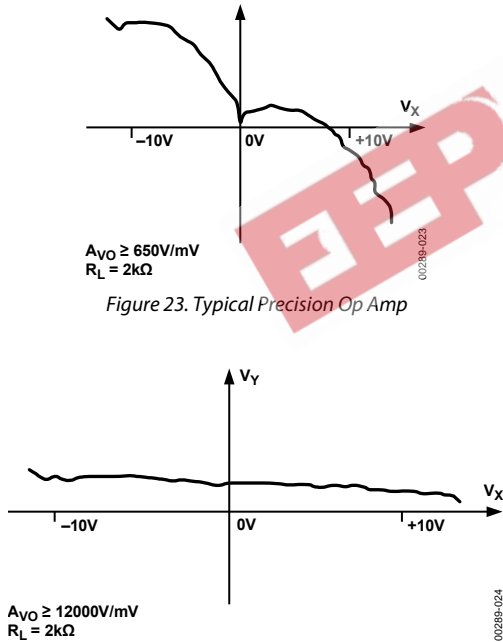


Figure 25. Open-Loop Gain Linearity Test Circuit

### THERMOCOUPLE AMPLIFIER WITH COLD-JUNCTION COMPENSATION

An example of a precision circuit is a thermocouple amplifier that must accurately amplify very low level signals without introducing linearity and offset errors to the circuit. In this circuit, an S-type thermocouple with a Seebeck coefficient of  $10.3 \mu\text{V}/^\circ\text{C}$  produces 10.3 mV of output voltage at a temperature of  $1000^\circ\text{C}$ . The amplifier gain is set at 973.16, thus, it produces an output voltage of 10.024 V. Extended temperature ranges beyond  $1500^\circ\text{C}$  are accomplished by reducing the amplifier gain. The circuit uses a low cost diode to sense the temperature at the terminating junctions and, in turn, compensates for any ambient temperature change. The OP177, with its high open-loop gain plus low offset voltage and drift, combines to yield a precise temperature sensing circuit. Circuit values for other thermocouple types are listed in Table 5.

Table 5.

Thermocouple Type	Seebeck Coefficient	R1	R2	R7	R9
K	$39.2 \mu\text{V}/^\circ\text{C}$	$110 \Omega$	$5.76 \text{ k}\Omega$	$102 \text{ k}\Omega$	$269 \text{ k}\Omega$
J	$50.2 \mu\text{V}/^\circ\text{C}$	$100 \Omega$	$4.02 \text{ k}\Omega$	$80.6 \text{ k}\Omega$	$200 \text{ k}\Omega$
S	$10.3 \mu\text{V}/^\circ\text{C}$	$100 \Omega$	$20.5 \text{ k}\Omega$	$392 \text{ k}\Omega$	$1.07 \text{ M}\Omega$

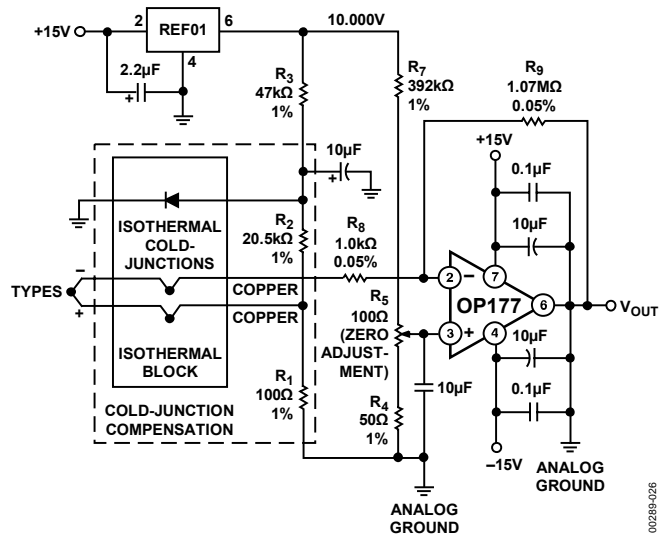


Figure 26. Thermocouple Amplifier with Cold Junction Compensation

# OP177

## PRECISION HIGH GAIN DIFFERENTIAL AMPLIFIER

The high gain, gain linearity, CMRR, and low  $TCV_{OS}$  of the OP177 make it possible to obtain performance not previously available in single stage, very high gain amplifier applications. See Figure 27.

For best CMR,  $\frac{R1}{R2}$  must equal  $\frac{R3}{R4}$

In this example, with a 10 mV differential signal, the maximum errors are listed in Table 6.

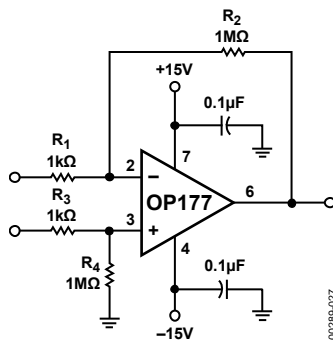


Figure 27. Precision High Gain Differential Amplifier

Table 6. High Gain Differential Amp Performance

Type	Amount
Common-Mode Voltage	0.1%/V
Gain Linearity, Worst Case	0.02%
$TCV_{OS}$	0.0003%/°C
$TC_{los}$	0.008%/°C

## ISOLATING LARGE CAPACITIVE LOADS

The circuit shown in Figure 28 reduces maximum slew rate but allows driving capacitive loads of any size without instability. Because the 100 Ω resistor is inside the feedback loop, its effect on output impedance is reduced to insignificance by the high open loop gain of the OP177.

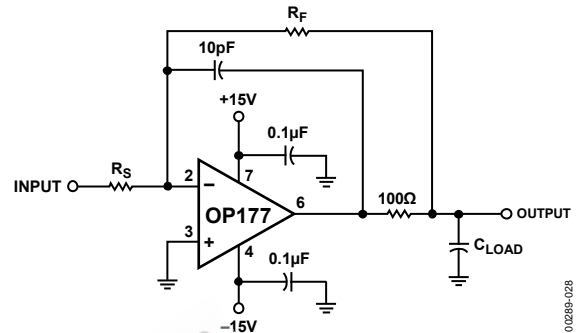


Figure 28. Isolating Capacitive Loads

## BILATERAL CURRENT SOURCE

The current sources shown in Figure 29 supply both positive and negative currents into a grounded load.

Note that

$$Z_o = \frac{R5 \left( \frac{R4}{R2} + 1 \right)}{\frac{R5 + R4}{R2} - \frac{R3}{R1}}$$

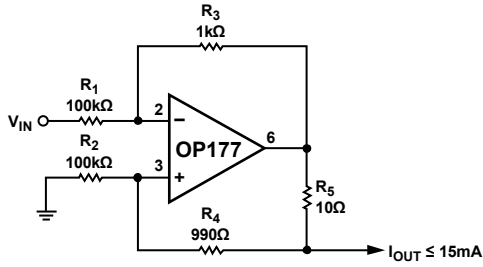
and that for  $Z_o$  to be infinite

$$\frac{R5 + R4}{R2} \text{ must} = \frac{R3}{R1}$$

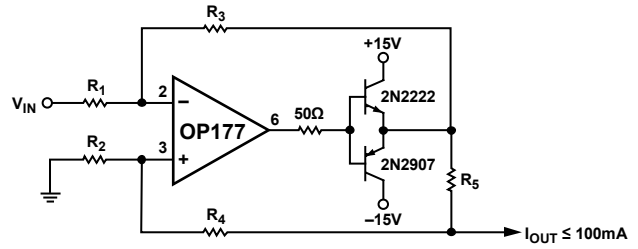
## PRECISION ABSOLUTE VALUE AMPLIFIER

The high gain and low  $TCV_{OS}$  assure accurate operation with inputs from microvolts to volts. In this circuit, the signal always appears as a common-mode signal to the op amps (for details, see Figure 30).

BASIC CURRENT SOURCE



100mA CURRENT SOURCE



$$I_{OUT} = V_{IN} \frac{R_3}{R_1 \times R_5}$$

GIVEN  $R_3 = R_4 + R_5$ ,  $R_1 = R_2$

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Figure 29. Bilateral Current Source

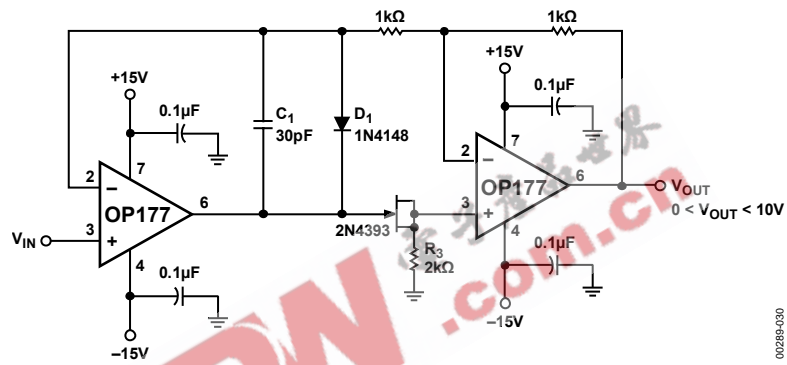


Figure 30. Precision Absolute Value Amplifier

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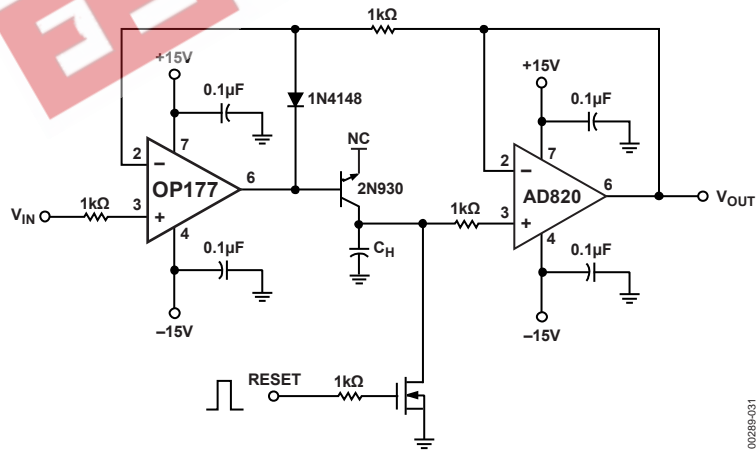


Figure 31. Precision Positive Peak Detector

00289-031

# OP177

## PRECISION POSITIVE PEAK DETECTOR

In Figure 31,  $C_H$  must be polystyrene, Teflon®, or polyethylene to minimize dielectric absorption and leakage. The droop rate is determined by the size of  $C_H$  and the bias current of the AD820.

## PRECISION THRESHOLD DETECTOR/AMPLIFIER

In Figure 32, when  $V_{IN} < V_{TH}$ , amplifier output swings negative, reverse biasing diode  $D_1$ .  $V_{OUT} = V_{TH}$  if  $R_L = \infty$ . When  $V_{IN} \geq V_{TH}$ , the loop closes.

$$V_{OUT} = V_{TH} + (V_{IN} - V_{TH}) \left( 1 + \frac{R_F}{R_S} \right)$$

$C_C$  is selected to smooth the response of the loop.

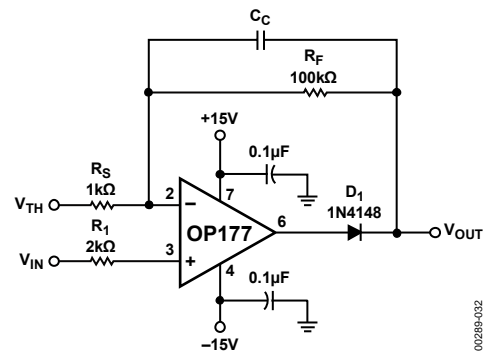
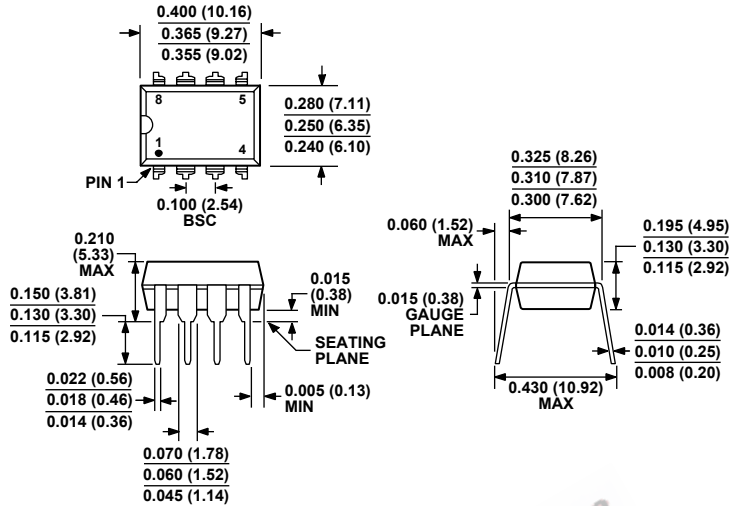


Figure 32. Precision Threshold Detector/Amplifier

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# OUTLINE DIMENSIONS

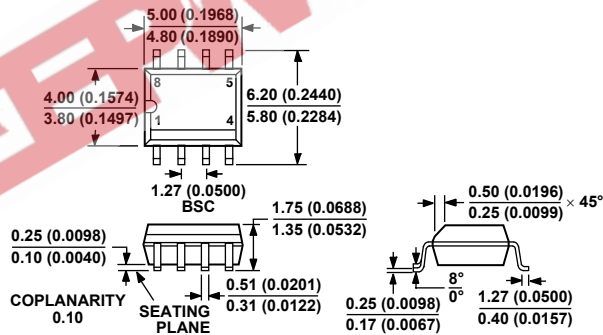


COMPLIANT TO JEDEC STANDARDS MS-001-BA  
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 33. 8-Lead Plastic Dual In-Line Package (PDIP)

P-Suffix  
(N-8)

Dimensions show in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 34. 8-Lead Standard Small Outline Package (SOIC\_N)

S-Suffix  
(R-8)

Dimensions shown in millimeters and (inches)

# OP177

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP177FP	-40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)
OP177FPZ <sup>1</sup>	-40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)
OP177GP	-40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)
OP177GPZ <sup>1</sup>	-40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)
OP177FS	-40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)
OP177FS-REEL	-40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)
OP177FS-REEL7	-40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)
OP177FSZ <sup>1</sup>	-40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)
OP177FSZ-REEL <sup>1</sup>	-40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)
OP177FSZ-REEL7 <sup>1</sup>	-40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)
OP177GS	-40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)
OP177GS-REEL	-40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)
OP177GS-REEL7	-40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)
OP177GSZ <sup>1</sup>	-40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)
OP177GSZ-REEL <sup>1</sup>	-40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)
OP177GSZ-REEL7 <sup>1</sup>	-40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)

<sup>1</sup> Z = Pb-free part.

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