

FEATURES

Significant Performance Advantages over LF155 and LF157 Devices

- Low Input Offset Voltages: 500 μV Max**
- Low Input Offset Voltage Drift: 2.0 $\mu\text{V}/^\circ\text{C}$**
- Minimum Slew Rate Guaranteed on All Models**
- Temperature-Compensated Input Bias Currents**
- Bias Current Specified Warmed-Up Over Temperature**
- Internal Compensation**
- Low Input Noise Current: 0.01 $\text{pA}/\sqrt{\text{Hz}}$**
- High Common-Mode Rejection Ratio: 100 dB**
- Models with MIL-STD 883 Processing Available**

OP15

- 156 Speed with 155 Dissipation: 80 mW Typ**
- Wide Bandwidth: 6 MHz**
- High Slew Rate: 13 $\text{V}/\mu\text{s}$**
- Fast Settling to $\pm 0.1\%$: 1,200 ns**

OP17

- Highest Slew Rate: 60 $\text{V}/\mu\text{s}$**
- Fastest Settling to $\pm 0.1\%$: 600 ns**
- Highest Gain Bandwidth Product ($A_{\text{VCL}} = 5 \text{ Min}$): 30 MHz**
- Guaranteed Input Bias Current @ 125°C**

GENERAL DESCRIPTION

The ADI-JFET input series of devices offer clear advantages over industry-generic devices and are superior in both cost and performance to many dielectrically-isolated and hybrid op amps. All devices offer offset voltages as low as 0.5 mV with TCV_{OS} guaranteed to 5 $\mu\text{V}/^\circ\text{C}$. A unique input bias cancellation circuit reduces the I_{B} by a factor 10 over conventional designs. In addition ADI specifies I_{B} and I_{OS} with the devices warmed up and operating at 25°C ambient.

These devices were designed to provide real precision performance along with high speed. Although they can be nulled, the design objective was to provide low offset-voltage without nulling. Systems generally become more cost effective as the number of trim circuits is decreased. ADI achieves this performance by use of an improved bipolar compatible JFET process coupled with on chip, zener-zap offset trimming.

The OP15 provides an excellent combinations of high speed and low input offset voltage. In addition, the OP15 offers the speed of the 156A op amp with the power dissipation of a 155A. The combination of a low input offset voltage of 500 μV , slew rate of 13 $\text{V}/\mu\text{s}$, and settling time of 1,200 ns to 0.1% makes the OP15 an op amp of both precision and speed. The additional features of low supply current coupled with an input bias current makes the OP15 ideal for a wide range of applications.

The OP17 has a slew rate of 60 $\text{V}/\mu\text{s}$ and is the best choice for applications requiring high closed-loop gain with high speed. See OP42 datasheet for unity gain applications and the OP215 datasheet for a dual configuration of the OP15.

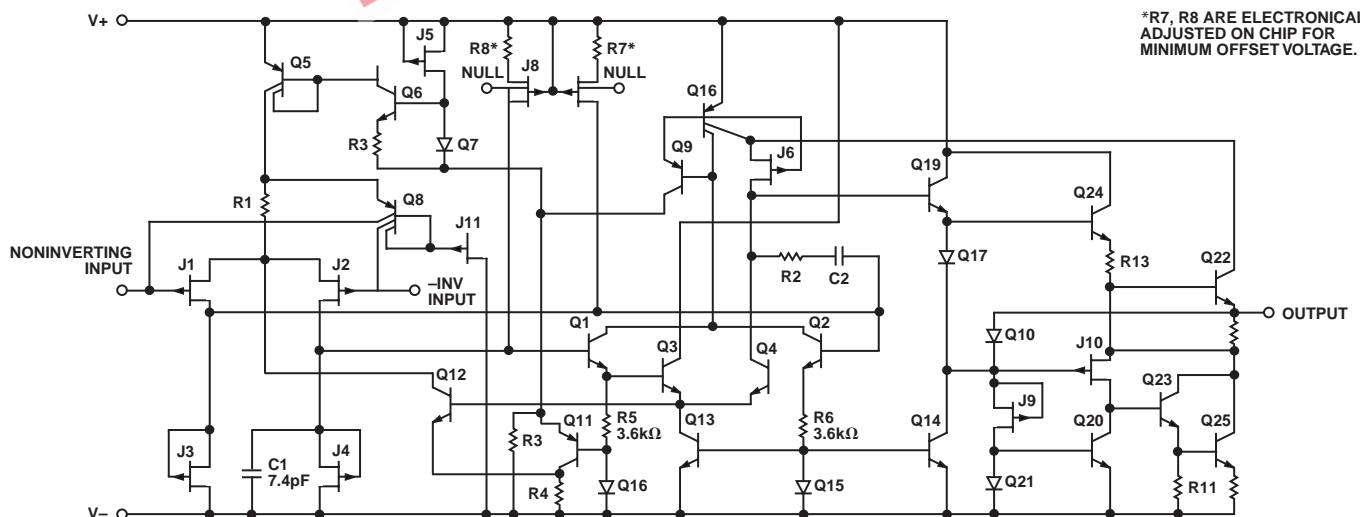


Figure 1. Simplified Schematic

REV. A

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OP15/OP17–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ $V_S = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Conditions	OP15A, OP15E OP17A, OP17E			OP15F OP17F			OP15G OP17G			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{OS}	$R_S = 50\ \Omega$		0.2	0.5		0.4	1.0		0.5	3.0	mV
Input Offset Current	I_{OS}	$T_J = 25^\circ\text{C}^1$ Device Operating		3	10		6	20		12	50	pA
		$T_J = 25^\circ\text{C}^1$ Device Operating		5	22		10	40		20	100	pA
		$T_J = 25^\circ\text{C}^1$ Device Operating		3	10		6	20		12	50	pA
		$T_J = 25^\circ\text{C}^1$ Device Operating		5	25		10	50		20	125	pA
Input Bias Current	I_B	$T_J = 25^\circ\text{C}^1$ Device Operating		± 15	± 50		± 30	± 100		± 60	± 200	pA
		$T_J = 25^\circ\text{C}^1$ Device Operating		± 18	± 110		± 40	± 200		± 80	± 400	pA
		$T_J = 25^\circ\text{C}^1$ Device Operating		± 15	± 50		± 30	± 100		± 60	± 200	pA
		$T_J = 25^\circ\text{C}^1$ Device Operating		± 20	± 130		± 40	± 250		± 80	± 500	pA
Input Resistance	R_{IN}			10^{12}			10^{12}			10^{12}		Ω
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2\ \text{k}\Omega$ $V_O = \pm 10\ \text{V}$	100	240		75	220		50	200		V/mV
Output Voltage Swing	V_O	$R_L = 10\ \text{k}\Omega$ $R_L = 2\ \text{k}\Omega$	± 12 ± 11	± 13 ± 12.7		± 12 ± 11	± 13 ± 12.7		± 12 ± 11	± 13 ± 12.7		V V
Supply Current	I_{SY}	OP15 OP17		2.7 4.6	4.0 7.0		2.7 4.6	4.0 7.0		2.8 4.8	5.0 8.0	mA mA
Slew Rate ²	SR	$A_{VCL} = 1$, OP15 $A_{VCL} = 5$, OP17	10 45	13 60		7.5 35	11 50		5 25	9 40		V/ μs V/ μs
Gain Bandwidth ³ Product	GBW	OP15 OP17	4.0 20	6.0 30		3.5 15	5.7 28		3.0 11	5.4 26		MHz MHz
Closed-Loop Bandwidth	CLBW	$A_{VCL} = 1$, OP15 $A_{VCL} = 5$, OP17		14 11			13 10			12 9		MHz MHz
Settling Time	t_s	$T_O = 0.01\%$ $T_O = 0.05\%$ $T_O = 0.10\%$ $T_O = 0.01\%$ $T_O = 0.05\%$ $T_O = 0.10\%$		4.5 1.5 1.2 1.5 0.7 0.6			4.5 1.5 1.2 1.5 0.7 0.6			4.7 1.6 1.3 1.6 0.8 0.7		μs μs μs μs μs μs
Input Voltage Range	IVR			± 10.5			± 10.5			± 10.3		V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10.5\ \text{V}$ $V_{CM} = \pm 10.3\ \text{V}$	86	100		86	100		82	96		dB dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10\ \text{V}$ to $\pm 18\ \text{V}$ $V_S = \pm 10\ \text{V}$ to $\pm 18\ \text{V}$		10	51		10	51		10	80	$\mu\text{V}/\text{V}$ $\mu\text{V}/\text{V}$
Input Noise Voltage Density	e_n	$f_O = 100\ \text{Hz}$ $f_O = 1\ \text{kHz}$		20 15			20 15			20 15		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$
Input Noise Current Density	i_n	$f_O = 100\ \text{Hz}$ $f_O = 1\ \text{kHz}$		0.01 0.01			0.01 0.01			0.01 0.01		$\text{pA}/\sqrt{\text{Hz}}$ $\text{pA}/\sqrt{\text{Hz}}$
Input Capacitance	C_{IN}			3			3			3		pF

NOTES

¹Input bias current is specified for two different conditions. The $T_J = 25^\circ\text{C}$ specification is with the junction at ambient temperature; the device operating specification is with the device operating in a warmed-up condition at 25°C ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B versus T_J and I_B versus T_A . ADI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.

²Settling time is defined here for a unity gain inverter connection using $2\ \text{k}\Omega$ resistors. It is the time required for the error voltage (the voltages at the inverting input pin on the amplifier) to settle to within a specified percent of its final value from the time a $10\ \text{V}$ step input is applied to the inverter. See settling time test circuit.

³Sample tested.

⁴Settling time is defined here for $A_V = -5$ connection with $R_F = 2\ \text{k}\Omega$. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a $2\ \text{V}$ step input is applied to the inverter. See settling time test circuit.

Electrical Characteristics (@ $V_S = \pm 15\text{ V}$, $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Offset Voltage	V_{OS}	$R_S = 50\ \Omega$		0.4	0.9	mV
Average Input Offset Voltage Drift ¹ Without External Trim	TCV_{OS}	$R_P = 100\ \Omega$		2	5	$\mu\text{V}/^\circ\text{C}$
With External Trim	TCV_{OSn}			2		$\mu\text{V}/^\circ\text{C}$
Input Offset Current ² OP17	I_{OS}	$T_J = 125^\circ\text{C}$ $T_A = 125^\circ\text{C}$, device operating		0.6 1.0	4.0 8.5	nA nA
Input Bias Current ² OP17	I_B	$T_J = 125^\circ\text{C}$ $T_A = 125^\circ\text{C}$, device operating		± 1.2 ± 2.0	± 5.0 ± 11	nA nA
Input Voltage Range	IVR		± 10.4			V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10.4\text{ V}$	85	97		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10\text{ V}$ to $\pm 18\text{ V}$		15	57	$\mu\text{V}/\text{V}$
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2\text{ k}\Omega$, $V_O = \pm 10\text{ V}$	35	120		V/mV
Output Voltage Swing	V_O	$R_L \geq 10\text{ k}\Omega$	± 12	± 13		V

NOTES

¹Sample tested.

²Input bias current is specified for two different conditions. The $T_J = 25^\circ\text{C}$ specification is with the junction at ambient temperature; the device operating specification is with the device operating in a warmed-up condition at 25°C ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B versus T_J and I_B versus T_A . ADI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.

ELECTRICAL CHARACTERISTICS (@ $V_S = \pm 15\text{ V}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ for E and F grades, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ for G grades unless otherwise noted)

Parameter	Symbol	Conditions	OP15E/OP17E			OP15F/OP17F			OP15G/OP17G			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{OS}	$R_S = 50\ \Omega$		0.3	0.75		0.55	1.5		0.7	3.8	mV
Average Input Offset Voltage Drift ¹ Without External Trim	TCV_{OS}	$R_P = 100\ \Omega$		2	5		3	10		4	30	$\mu\text{V}/^\circ\text{C}$
With External Trim	TCV_{OSn}			2			3			4		$\mu\text{V}/^\circ\text{C}$
Input Offset Current ² OP15	I_{OS}	$T_J = 70^\circ\text{C}$		0.04	0.30		0.06	0.45		0.08	0.85	nA
		$T_A = 70^\circ\text{C}$, Device Operating		0.06	0.55		0.08	0.80		0.10	1.2	nA
OP17		$T_J = 70^\circ\text{C}$		0.04	0.30		0.06	0.45		0.08	0.85	nA
		$T_A = 70^\circ\text{C}$, Device Operating		0.07	0.70		0.10	1.1		0.15	1.7	nA
Input Bias Current ² OP15	I_B	$T_J = 70^\circ\text{C}$		± 0.10	± 0.40		± 0.12	± 0.60		± 0.14	± 0.80	nA
		$T_A = 70^\circ\text{C}$, Device Operating		± 0.13	± 0.75		± 0.16	± 1.1		± 0.19	± 1.5	nA
OP17		$T_J = 70^\circ\text{C}$		± 0.10	± 0.40		± 0.12	± 0.60		± 0.14	± 0.80	nA
		$T_A = 70^\circ\text{C}$, Device Operating		± 0.15	± 0.90		± 0.20	± 1.4		± 0.25	± 2.0	nA
Input Voltage Range	IVR		± 10.4			± 10.4			± 10.25			V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10.4\text{ V}$ $V_{CM} = \pm 10.25\text{ V}$	85	98		85	96		80	94		dB dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10\text{ V}$ to $\pm 18\text{ V}$ $V_S = \pm 10\text{ V}$ to $\pm 15\text{ V}$		13	57		13	57		20	100	$\mu\text{V}/\text{V}$ $\mu\text{V}/\text{V}$
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2\text{ k}\Omega$ $V_O = \pm 10\text{ V}$	65	200		50	180		35	160		V/mV
Output Voltage Swing	V_O	$R_L \geq 10\text{ k}\Omega$	± 12	± 13		± 12	± 13		± 12	± 13		V

NOTES

¹Sample tested.

²Input bias current is specified for two different conditions. The $T_J = 25^\circ\text{C}$ specification is with the junction at ambient temperature; the device operating specification is with the device operating in a warmed-up condition at 25°C ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B versus T_J and I_B versus T_A . ADI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.

OP15/OP17-SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS¹

Supply Voltage	
All Devices Except C, G (Packaged) and GR Grades	±22 V
C, G (Packaged) and GR Grades	±18 V
Operating Temperature	
A Grade	-55°C to +125°C
E, F Grades	0°C to 70°C
G Grade	-40°C to +85°C
Maximum Junction Temperature	
	150°C
Differential Input Voltage	
All Devices Except C, G Grades	±40 V
C, G Grades	±30 V
Input Voltage ²	
All Devices Except C, G Grades	±20 V
C, G Grades	±16 V
Input Voltage	
OP15E, OP15F	±20 V
OP15G	±16 V
OP17A, OP17E, OP17F	±20 V
OP17G	±16 V
Output Short-Circuit Duration	
	Indefinite
Storage Temperature Range	
	-65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	
	300°C

NOTES

*Absolute Maximum Ratings apply to packaged parts, unless otherwise noted.

Package Type	θ_{JA} *	θ_{JC}	Unit
8-Lead Hermetic DIP (Z)	148	16	°C/W
8-Lead SO (S)	158	43	°C/W
TO-99 (J)	150	18	°C/W

* θ_{JA} is specified for worst-case mounting conditions, i.e., θ_{JA} is specified for device in socket for CERPDP and PDIP packages; θ_{JA} is specified for device soldered to printed circuit board for SO packages.

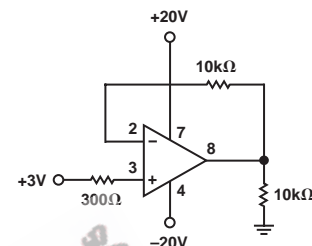
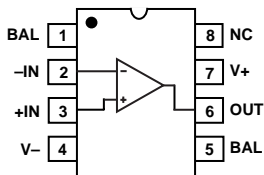
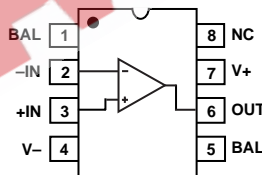


Figure 2. Burn-In Circuit

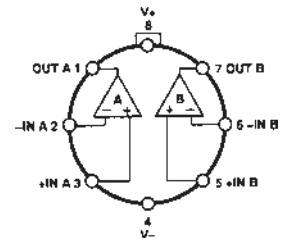
8-Lead CERPDP (Z-Suffix)



8-Lead SOIC (S-Suffix)



8-Lead TO-99 (J-Suffix)



ORDERING GUIDE

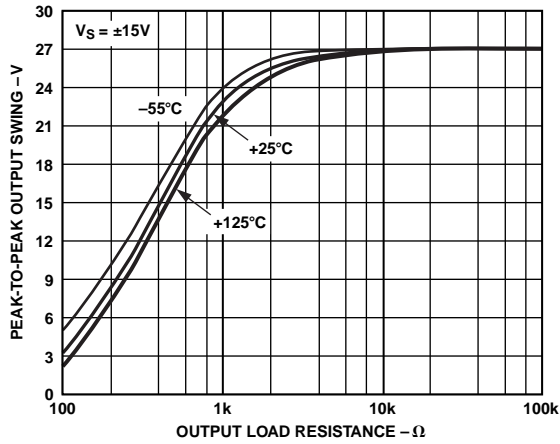
$T_A = 25^\circ\text{C}$ $V_{OS\text{ MAX}}$ (mV)	Package Options			Operating Temperature Range
	TO-99	CERPDP	SOIC	
0.5	OP17EJ	OP15EZ OP17EZ		COM
1.0	OP15FJ* OP17FJ	OP15FZ* OP17FZ		COM
3.0	OP15GJ*	OP15GZ* OP17GZ	OP15GS*	XIND

For military processed devices, please refer to the Standard Microcircuit Drawing (SMD) available at www.dscc.dl.mil/programs/milspec/default.asp.

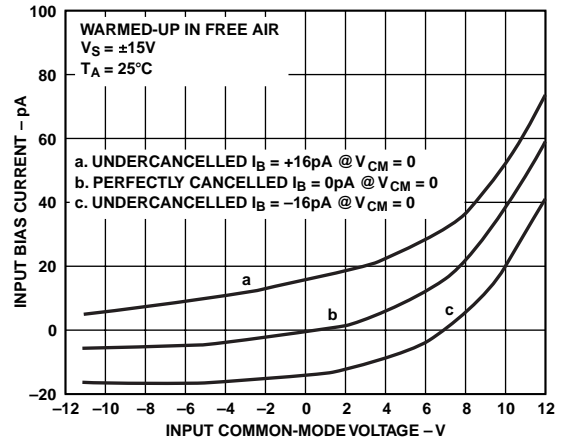
SMD Part Number	ADI Equivalent
5962-8954201GA*	OP15AJMDA
5962-8954201PA*	OP15AZMDA
5962-8954301GA*	OP16AJMDA
5962-8954301PA*	OP16AZMDA

*Not recommended for new designs. Obsolete April 2002.

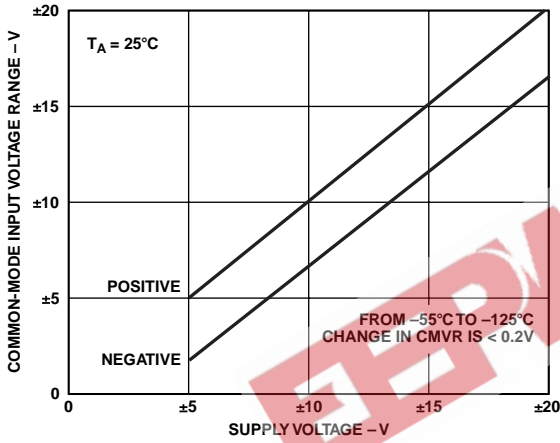
Typical Performance Characteristics –OP15/OP17



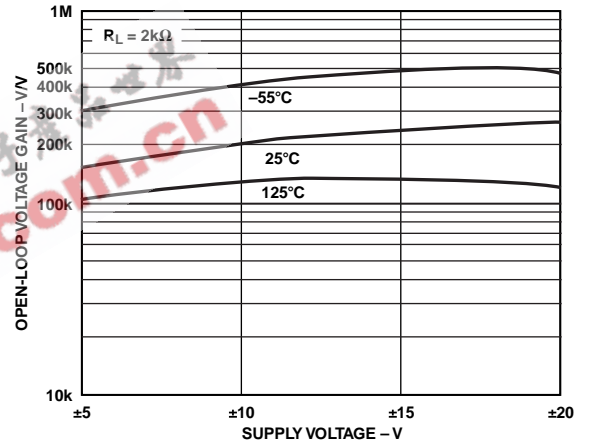
TPC 1. Maximum Output Swing vs. Load Performance



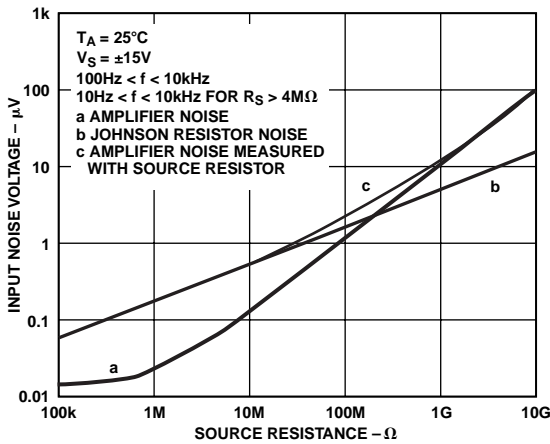
TPC 4. Input Bias Current vs. Common-Mode Voltage



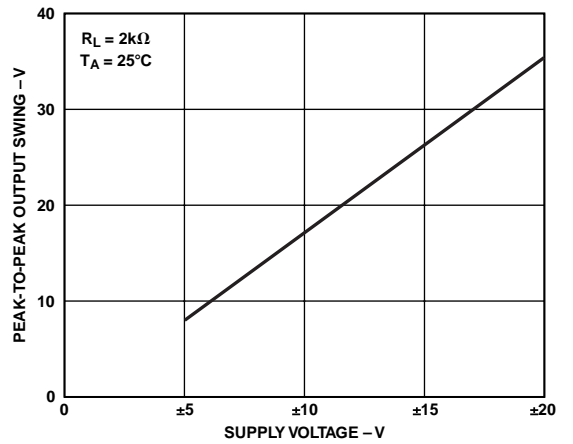
TPC 2. Common-Mode Input Voltage Range vs. Supply Voltage



TPC 5. Open-Loop Voltage Gain vs. Supply Voltage

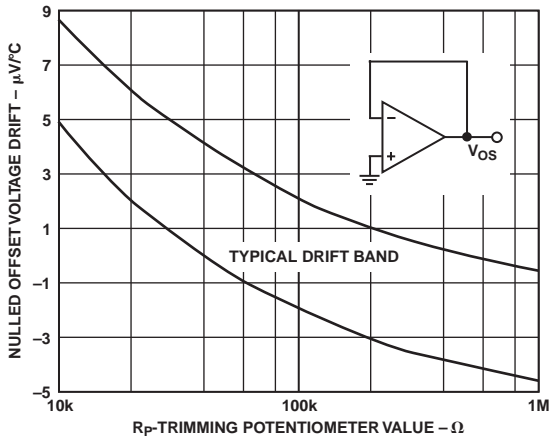


TPC 3. Voltage Noise vs. Source Resistance

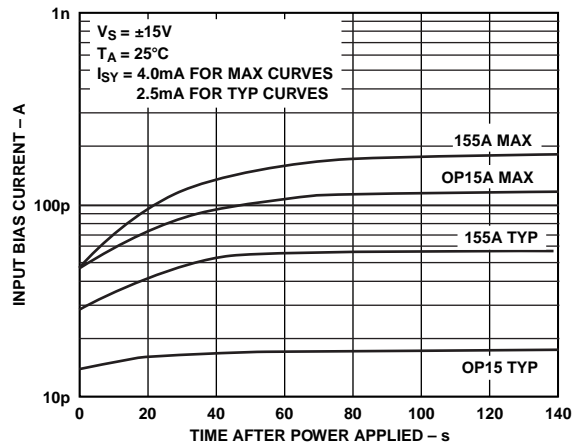


TPC 6. Output Voltage Swing vs. Supply Voltage

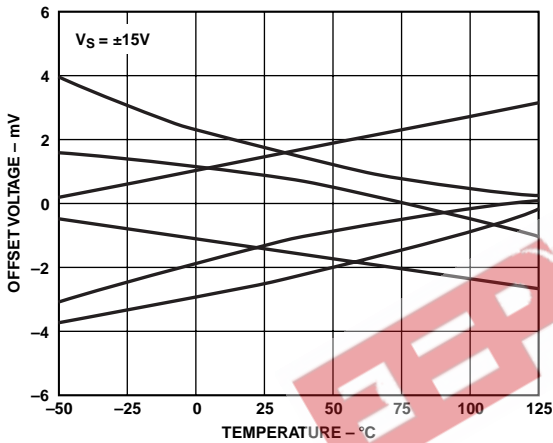
OP15/OP17



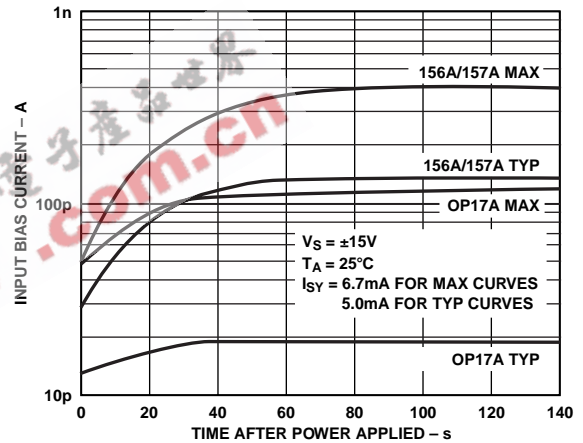
TPC 7. Nulled Offset Voltage Drift vs. Potentiometer Size



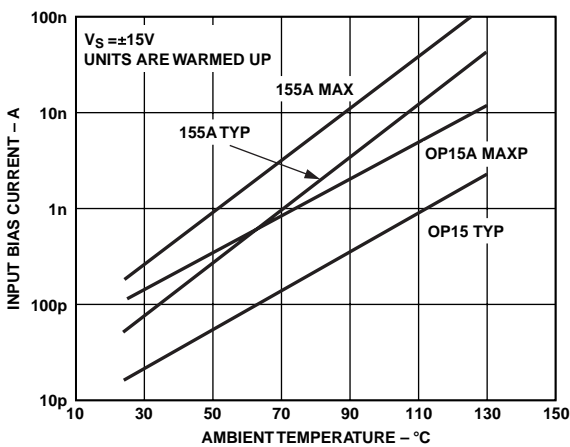
TPC 10. OP15 Bias Current vs. Time in Free Air



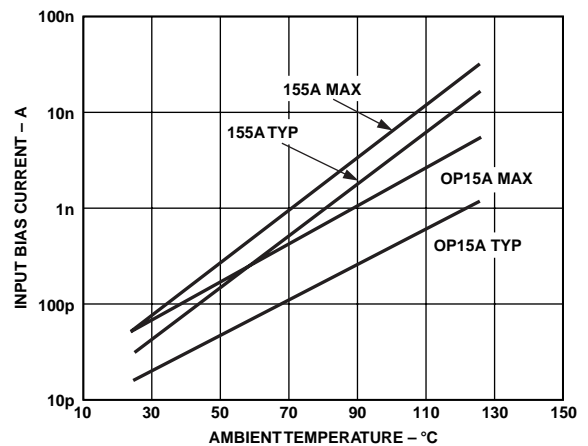
TPC 8. Offset Voltage Drift vs. Temperature of Representative Units



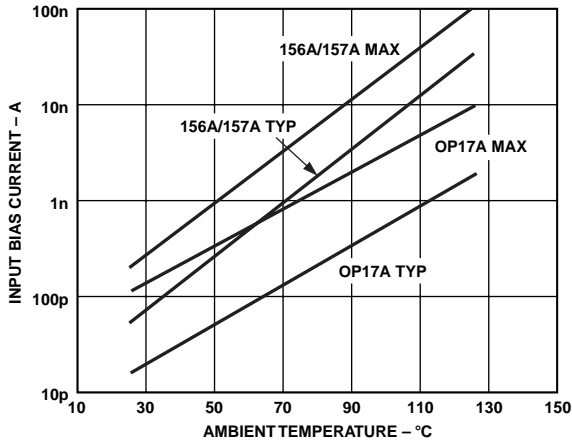
TPC 11. OP17 Bias Current vs. Time in Free Air



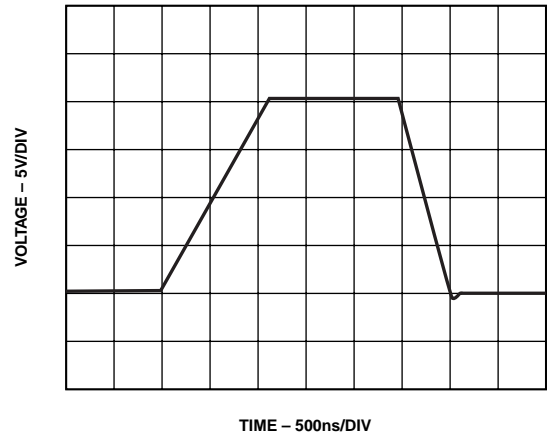
TPC 9. Input Bias Current vs. Ambient Temperature (Units Warmed Up in Free Air)



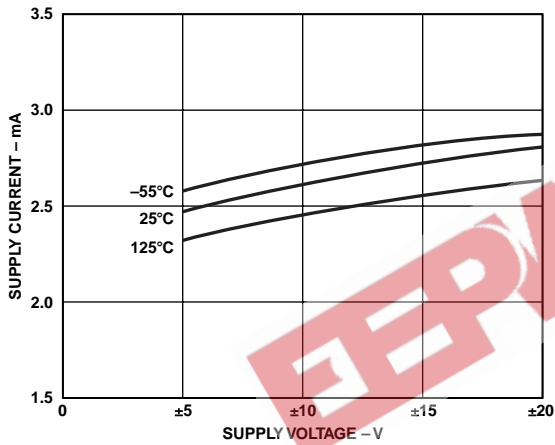
TPC 12. OP15 Input Bias Current vs. Ambient Temperature (Units Warmed Up in Free Air)



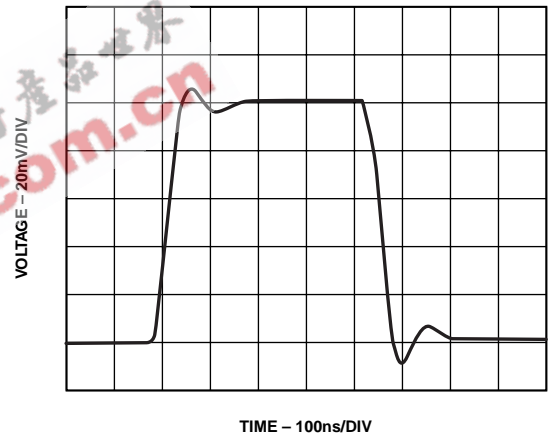
TPC 13. OP17 Input Bias Current vs. Ambient Temperature (Units Warmed Up in Free Air)



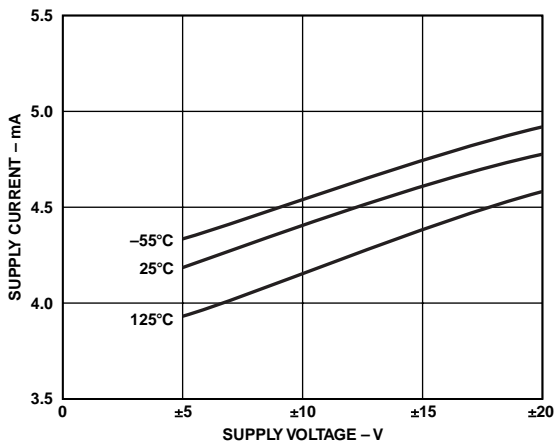
TPC 16. OP15 Large Signal Transient Response



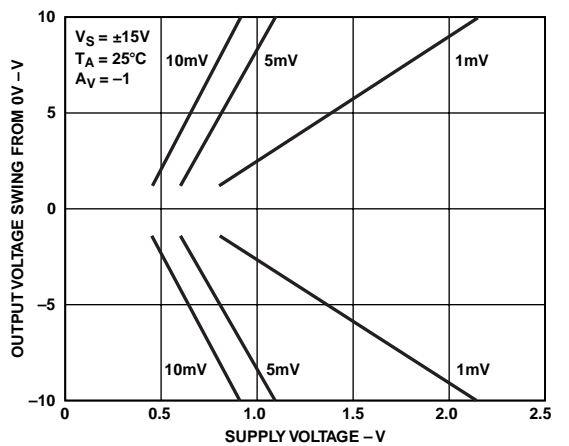
TPC 14. OP15 Supply Current vs. Supply Voltage



TPC 17. OP15 Small Signal Transient Response

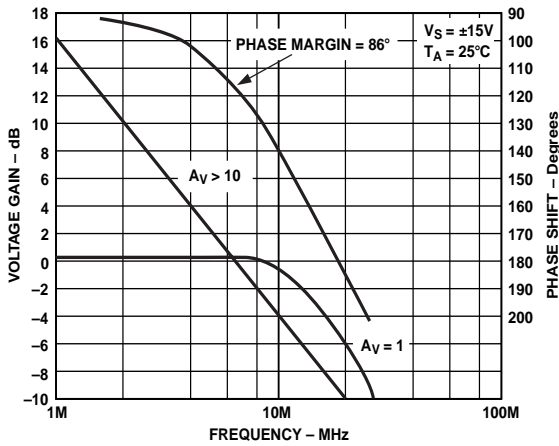


TPC 15. OP17 Supply Current vs. Supply Voltage

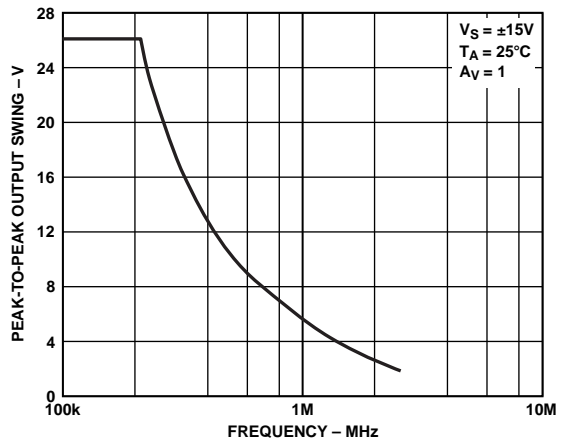


TPC 18. OP15 Settling Time

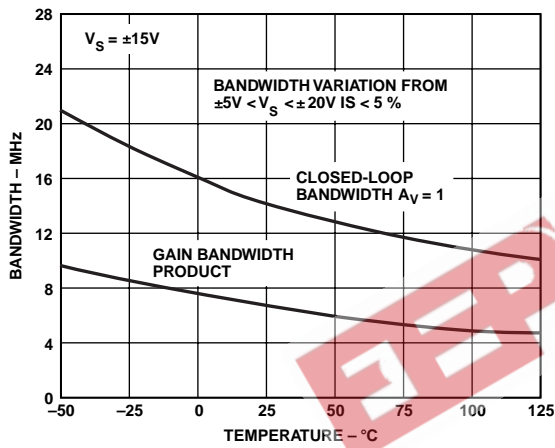
OP15/OP17



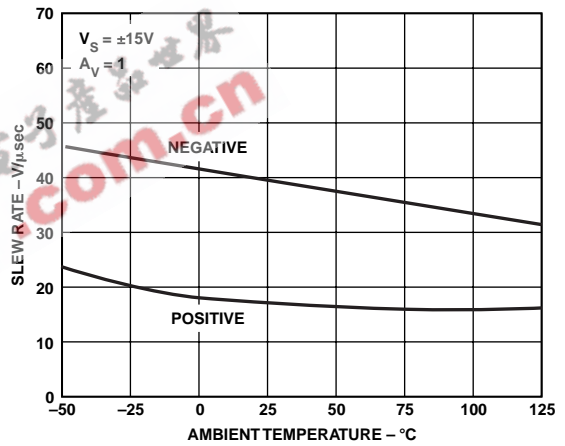
TPC 19. OP15 Closed-Loop Bandwidth and Phase vs. Frequency



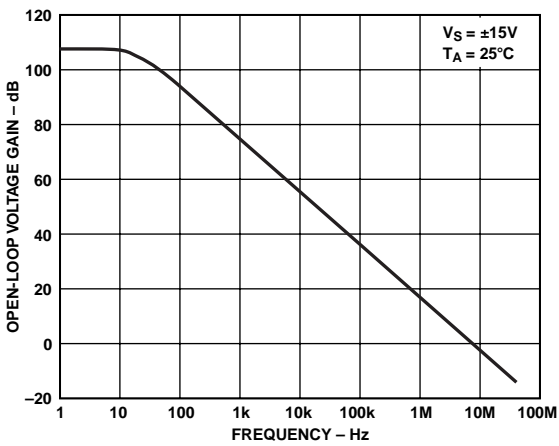
TPC 22. OP15 Maximum Output Swing vs. Frequency



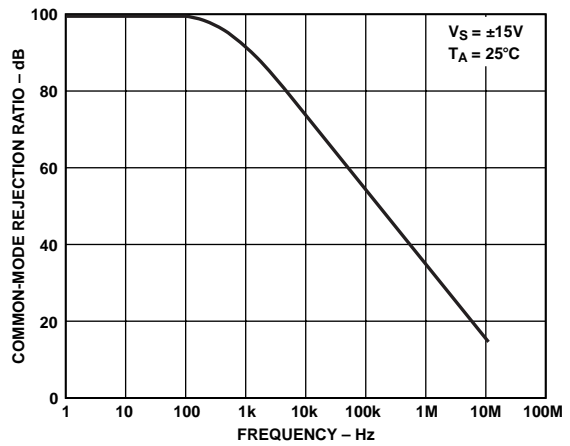
TPC 20. OP15 Bandwidth vs. Temperature



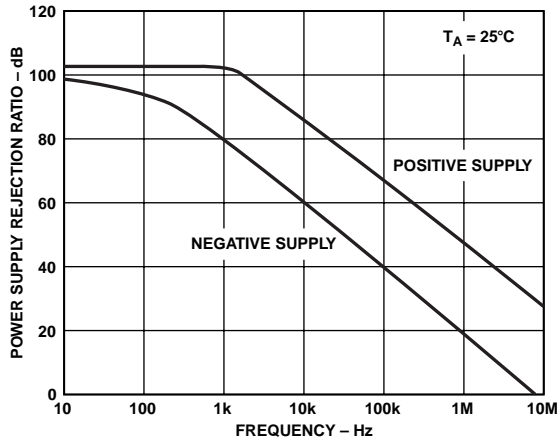
TPC 23. OP15 Slew Rate vs. Temperature



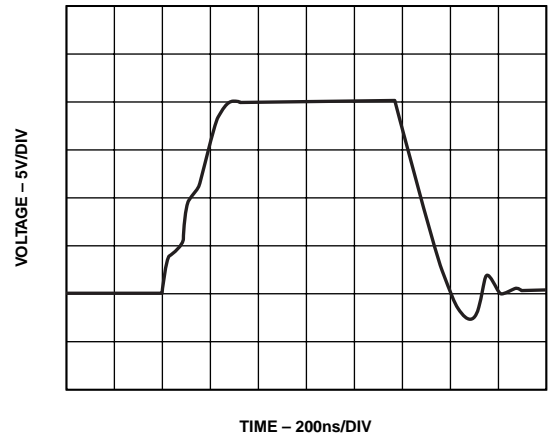
TPC 21. OP15 Open-Loop Gain vs. Frequency



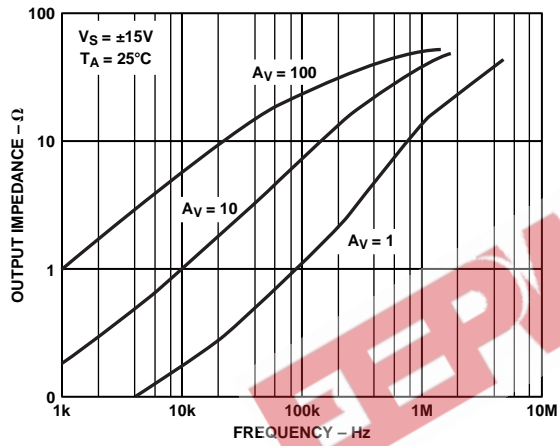
TPC 24. OP15 Common-Mode Rejection Ratio vs. Frequency



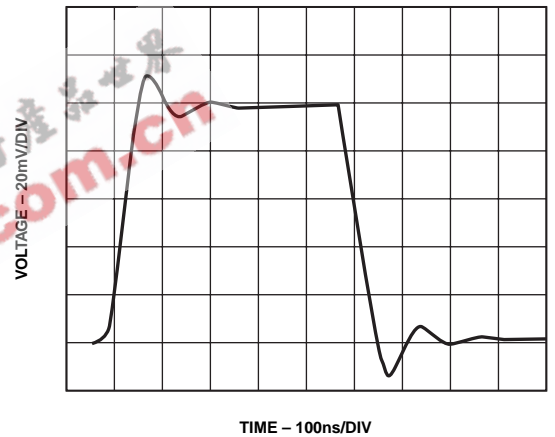
TPC 25. OP15 Power Supply Rejection Ratio vs. Frequency



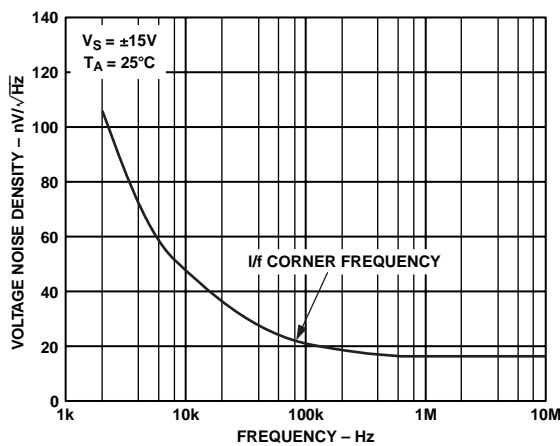
TPC 28. OP17 Large Signal Transient Response



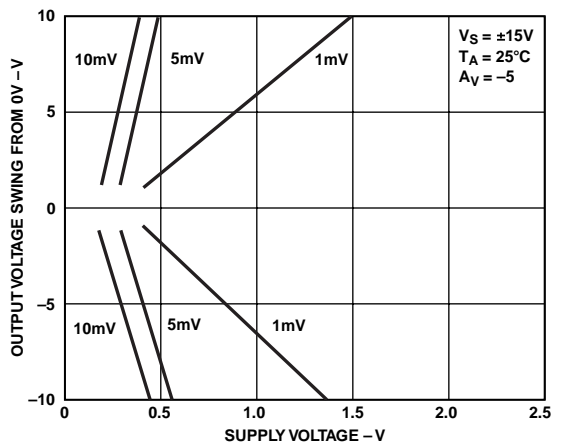
TPC 26. OP15 Output Impedance vs. Frequency



TPC 29. OP17 Small Signal Transient Response

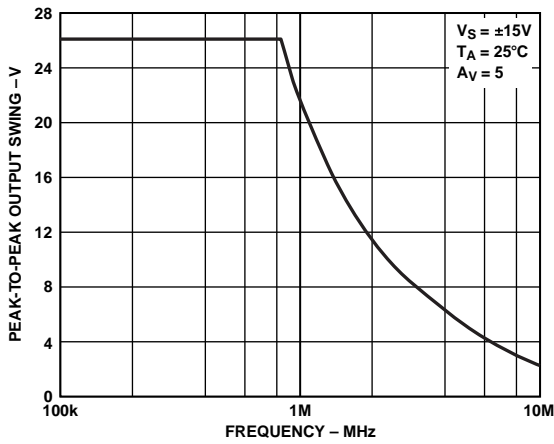


TPC 27. OP15 Voltage Noise Density vs. Frequency

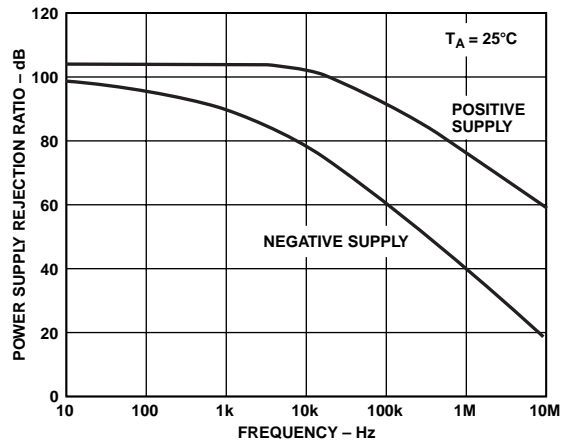


TPC 30. OP17 Settling Time

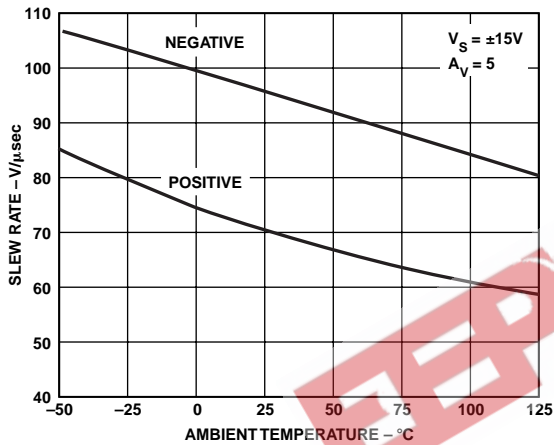
OP15/OP17



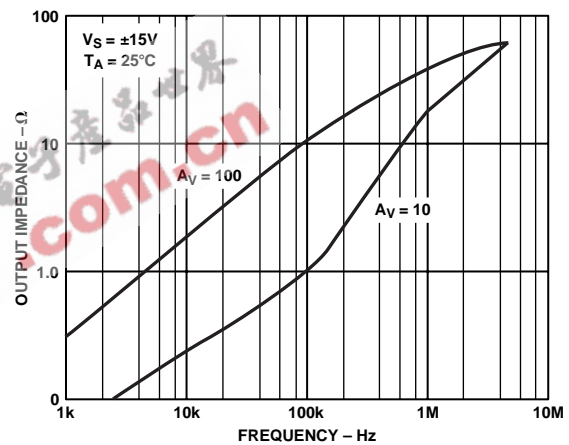
TPC 31. OP17 Maximum Output Swing vs. Frequency



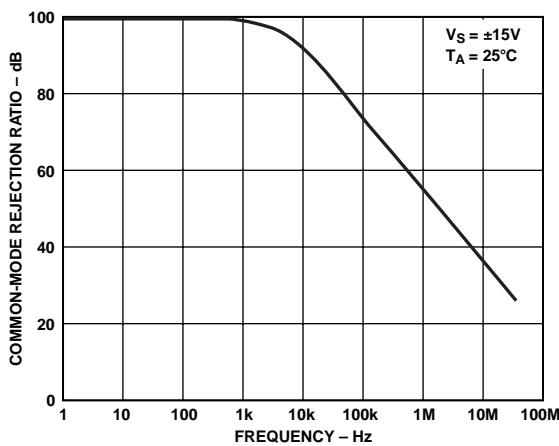
TPC 34. OP17 Power Supply Rejection Ratio vs. Frequency



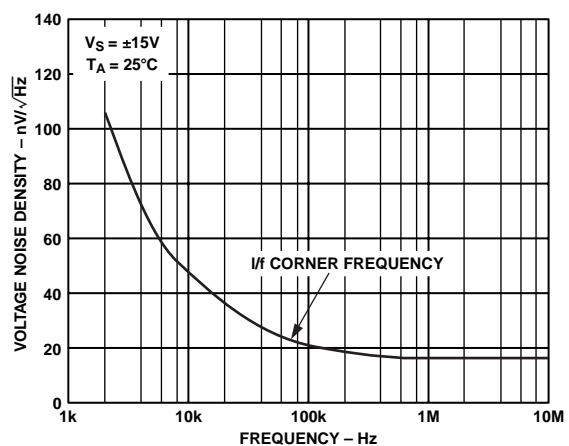
TPC 32. OP17 Slew Rate vs. Temperature



TPC 35. OP17 Output Impedance vs. Frequency

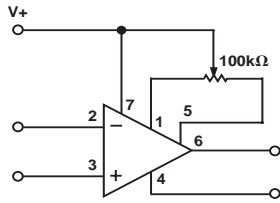


TPC 33. OP17 Common-Mode Rejection Ratio vs. Frequency



TPC 36. OP17 Voltage Noise vs. Frequency

TEST CIRCUITS



NOTE: V_{OS} CAN BE TRIMMED WITH POTENTIOMETERS RANGING FROM 10kΩ TO 1MΩ. FOR MOST UNITS TCV_{OS} WILL BE MINIMIZED WHEN V_{OS} IS ADJUSTED WITH A 100kΩ POTENTIOMETER

Figure 3. Input Offset Voltage Nulling

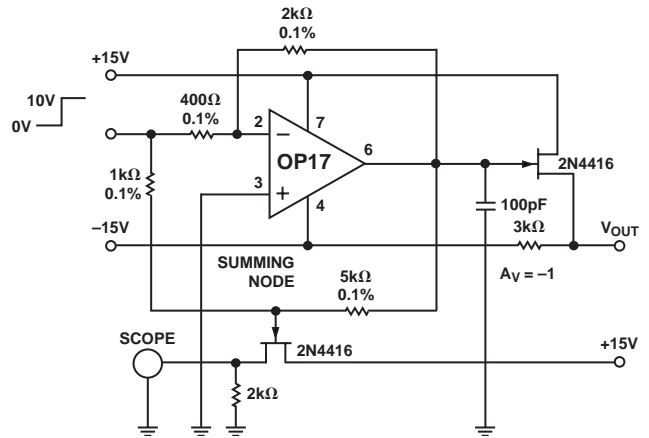


Figure 6. OP17 Settling Time Test Circuit

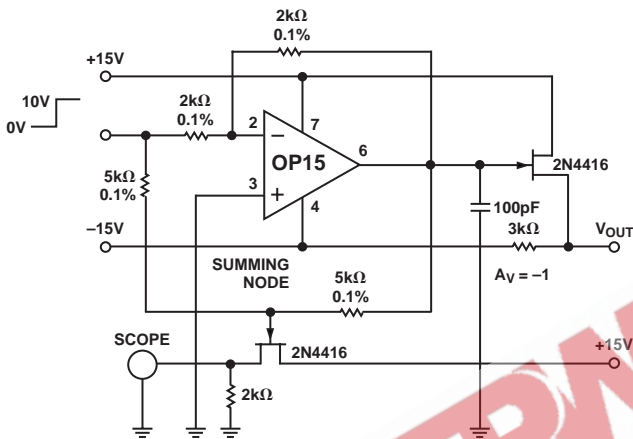


Figure 4. OP15 Settling Time Test Circuit

APPLICATION INFORMATION

Dynamic Operating Considerations

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance for the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of this pole. In many instances the frequency of this pole is much greater than the expected, 3 dB frequency of the close-loop gain, and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency, a lead capacitor should be placed from the output to the negative input of the op amp. The value of the added capacitor should be such that the RC time-constant of this capacitor and the resistance it parallels is greater than, or equal to, the original feedback pole time constant.

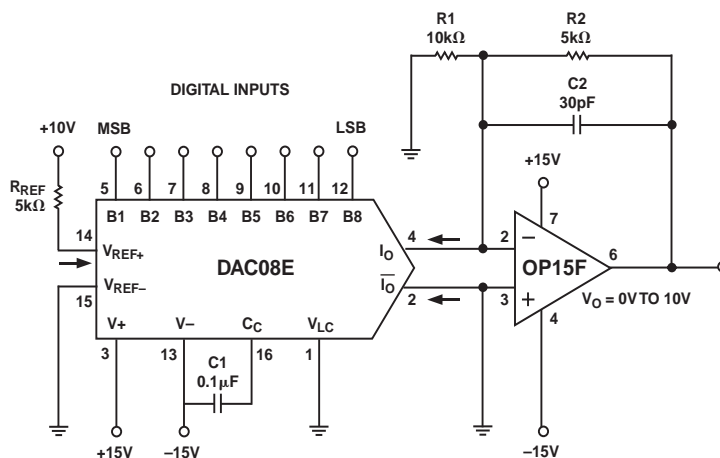


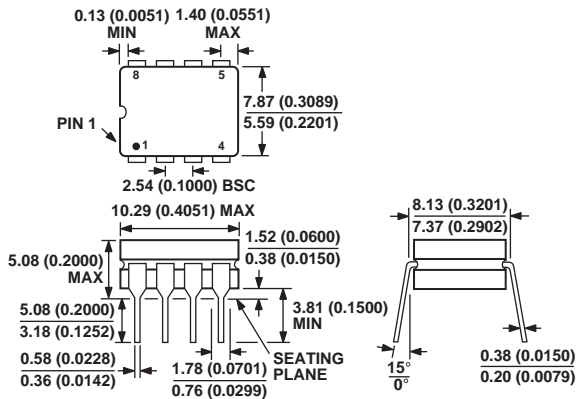
Figure 5. Current-to-Voltage Amplifier Output

OP15/OP17

OUTLINE DIMENSIONS

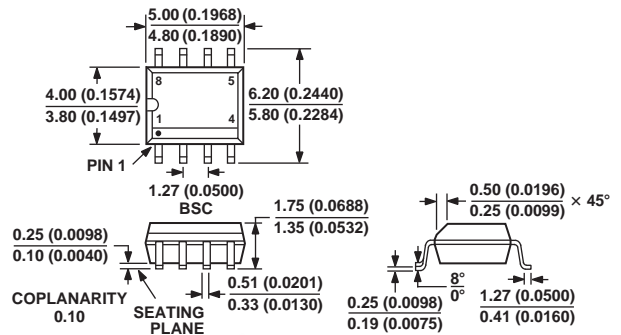
Dimensions shown in millimeters and (inches).

8-Lead Ceramic Dip – Glass Hermetic Seal [CERDIP] (Q-8)



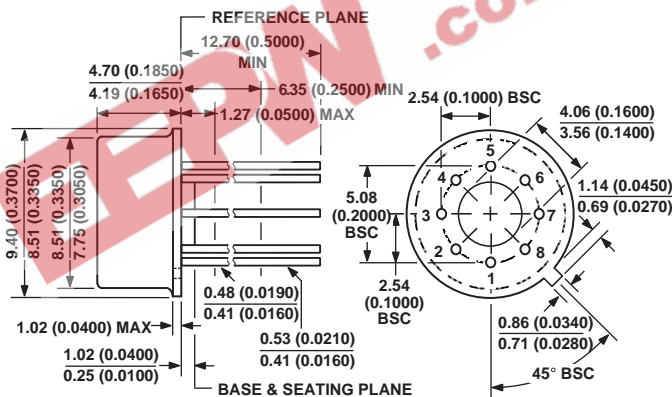
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Standard Small Outline Package [SOIC] Narrow Body (R-8)



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COMPLIANT TO JEDEC STANDARDS MS-012AA

8-Lead Metal Can [TO-99] (H-08)



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COMPLIANT TO JEDEC STANDARDS MO-002AK

Revision History

Location	Page
9/02—Data Sheet changed from REV. 0 to REV. A.	
Deleted OP16	Universal
Edits to FEATURES	1
Edits to GENERAL DESCRIPTION	1
Edits to SPECIFICATIONS	2
Edits to ORDERING GUIDE	2
Edits to ABSOLUTE MAXIMUM RATINGS	2
Edits to DICE CHARACTERISTICS	6
Edits to WAFER TEST LIMITS	6
Deleted 12 TPCs	11-12
Updated OUTLINE DIMENSIONS	12