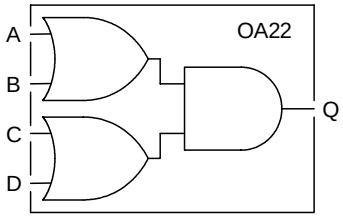
OA22 is an OR/AND circuit providing the logical function Q = [(A+B).(C+D)].

Truth Table

A	B	C	D	Q
L	L	X	X	L
X	X	L	L	L
X	H	H	X	H
X	H	X	H	H
H	X	X	H	H
H	X	H	X	H



Capacitance

	Ci (pF)
A	0.056
B	0.048
C	0.052
D	0.045

Area

0.81 mils^2

Power

2.60 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(L) with L = Output Load [pF]

AC Characteristics : Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

Characteristics	Symbol	SL = 0.1			SL = 2.0		
		L = 0.1	L = 0.7	L = 1.0	L = 0.1	L = 0.7	L = 1.0
Delay A to Q	tpdar	0.50	1.86	2.58	0.63	1.97	2.67
	tpdaf	0.52	1.63	2.15	0.78	1.89	2.42
Delay B to Q	tpdbr	0.54	1.89	2.64	0.72	2.04	2.74
	tpdbf	0.54	1.65	2.22	0.72	1.83	2.35
Delay C to Q	tpdcr	0.53	1.88	2.61	0.59	1.91	2.61
	tpdcf	0.58	1.71	2.21	0.88	1.99	2.53
Delay D to Q	tpddr	0.57	1.95	2.61	0.65	1.98	2.67
	tpddf	0.62	1.74	2.27	0.81	1.92	2.47
Output Slope A to Q	op_slar	0.92	5.33	7.55	0.88	5.21	7.48
	op_slaf	0.68	3.66	4.88	0.71	3.57	5.28
Output Slope B to Q	op_slbr	0.92	5.33	7.47	0.87	5.23	7.48
	op_slbf	0.70	3.63	5.08	0.72	3.56	5.13
Output Slope C to Q	op_slcr	0.92	5.32	7.52	0.91	5.21	7.47
	op_slcf	0.70	3.57	5.01	0.72	3.66	5.31
Output Slope D to Q	op_sldr	0.92	5.32	7.52	0.88	5.22	7.48
	op_sldf	0.71	3.58	5.31	0.70	3.60	5.07