

**PART NUMBERING GUIDE**

Environmental/Mechanical Specifications on page F5

<b>OEH 100 48 A T - 30.000MHz</b>	
<b>Package</b> OEH = 14 Pin Dip / 5.0Vdc / HCMOS-TTL OEH3 = 14 Pin Dip / 3.3Vdc / HCMOS-TTL	<b>Pin One Connection</b> Blank = No Connect, T = Tri State Enable High
<b>Inclusive Stability</b> 100= +/-100ppm, 50= +/-50ppm, 30= +/-30ppm, 25= +/-25ppm, 20= +/-20ppm, 15= +/-15ppm, 10= +/-10ppm	<b>Output Symmetry</b> Blank = 40/60%, A = 45/55%
	<b>Operating Temperature Range</b> Blank = 0°C to 70°C, 27 = -20°C to 70°C, 48 = -40°C to 85°C

**ELECTRICAL SPECIFICATIONS**

Revision: 1995-B

<b>Frequency Range</b>	250kHz to 106.250MHz
<b>Operating Temperature Range</b>	0°C to 70°C / -20°C to 70°C / -40°C to 85°C
<b>Storage Temperature Range</b>	-55°C to 125°C
<b>Supply Voltage</b>	5.0Vdc ±10%, 3.3Vdc ±10%
<b>Input Current</b>	250.000kHz to 24.000MHz: 30mA Maximum 24.001MHz to 50.000MHz: 45mA Maximum 50.001MHz to 66.667MHz: 60mA Maximum 66.668MHz to 106.250MHz: 80mA Maximum
<b>Frequency Tolerance / Stability</b>	Inclusive of Operating Temperature Range, Supply Voltage and Load: ±100ppm, ±50ppm, ±30ppm, ±25ppm, ±20ppm, ±15ppm or ±10ppm (20, 15, 10 = 0°C to 70°C Only)
<b>Output Voltage Logic High (Voh)</b>	w/TTL Load: 2.4Vdc Minimum w/HCMOS Load: Vdd - 0.5Vdc Minimum
<b>Output Voltage Logic Low (Vol)</b>	w/TTL Load: 0.4Vdc Maximum w/HCMOS Load: 0.5Vdc Maximum
<b>Rise Time</b>	0.4Vdc to 2.4Vdc w/TTL Load; 20% to 80% of Waveform w/HCMOS Load <=66.667MHz: 5nSeconds Maximum
<b>Fall Time</b>	0.4Vdc to 2.4Vdc w/TTL Load; 20% to 80% of Waveform w/HCMOS Load >66.667MHz: 3nSeconds Maximum
<b>Duty Cycle</b>	@1.4Vdc w/TTL Load; @50% w/HCMOS Load: 50 ±10% (Standard) @1.4Vdc w/TTL Load or w/HCMOS Load: 50±5% (Optional) @50% of Waveform w/LSTTL or HCMOS Load >66.667MHz: 50±5% (Optional)
<b>Load Drive Capability</b>	250.000kHz to 24.000MHz: 10TTL or 50pF HCMOS Load 24.001MHz to 66.667MHz: 10TTL or 15pF HCMOS Load 66.668MHz to 150.000MHz: 10LSTTL or 15pF HCMOS Load
<b>Pin 1 Tristate Input Voltage</b>	No Connection: Enables Output VIH: +2.2Vdc Minimum to Enable Output VIL: +0.8Vdc Maximum to Disable Output
<b>Aging (@ 25°C)</b>	±5ppm / year Maximum
<b>Start Up Time</b>	10mSeconds Maximum
<b>Absolute Clock Jitter</b>	±100pSeconds Maximum
<b>One Sigma Clock Jitter</b>	±25pSeconds Maximum

**MECHANICAL DIMENSIONS**

**Marking Guide**

Top view dimensions: 14.0 MAX (width), 9.8 MAX (length), 4.7 MAX (pin spacing).

Side view dimensions: 0.51 ±0.203 (pin height), 0.25 MIN (pin thickness).

Pin layout dimensions: 7.620 ±0.203 (pin pitch), 5.08 ±0.20 (pin offset).

Line 1: Blank or 3 - Frequency  
Line 2: CEI YM

Blank = 5.0V  
3 = 3.3V  
CEI = Caliber Electronics Inc.  
YM = Date Code (Year / Month)

Pin 1: No Connect or Tri-State      Pin 8: Output  
Pin 7: Case Ground                      Pin 14: Supply Voltage