

# DATA SHEET

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## **OQ2535HP** **SDH/SONET STM16/OC48** **multiplexer**

Product specification  
Supersedes data of 1997 Nov 27  
File under Integrated Circuits, IC19

1999 Oct 04

# SDH/SONET STM16/OC48 multiplexer

# OQ2535HP

### FEATURES

- Normal and loop (test) modes
- 3.3 V TTL compatible data inputs
- Differential Current-Mode Logic (CML) clock and data outputs
- 5 V TTL clock output (low speed interface)
- High input sensitivity (100 mV for the high speed clock input)
- Boundary Scan Test (BST) at low speed interface, in accordance with "IEEE Std 1149.1-1990"
- Low power dissipation (typically 1.65 W).

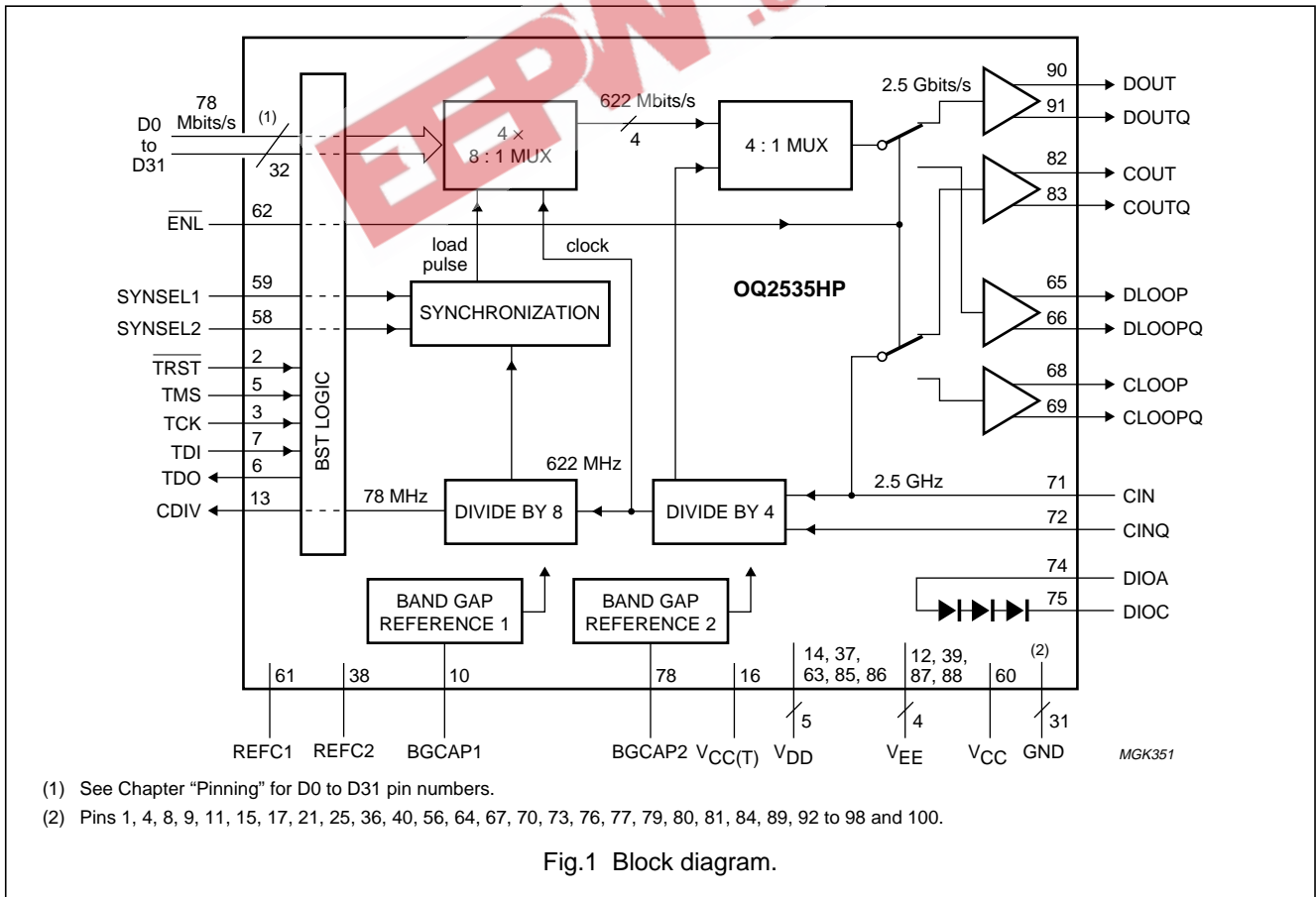
### GENERAL DESCRIPTION

The OQ2535HP is a 32-channel multiplexer intended for use in STM16/OC48 applications. It combines data from a total of  $32 \times 78$  Mbits/s input channels onto a single 2.5 Gbits/s output channel. It features 3.3 V TTL data inputs and a 5 V TTL clock output at the low speed interface, and CML compatible inputs and outputs at the high speed interface.

### ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OQ2535HP	HLQFP100	plastic heat-dissipating low profile quad flat package; 100 leads; body $14 \times 14 \times 1.4$ mm	SOT470-1

### BLOCK DIAGRAM



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## PINNING

SYMBOL	PIN	TYPE <sup>(1)</sup>	DESCRIPTION
GND	1	S	ground
TRS	2	I	test reset input for BST mode (active LOW)
TCK	3	I	test clock input for BST mode
GND	4	S	ground
TMS	5	I	test mode select input for BST mode
TDO	6	O	serial test data output for BST mode
TDI	7	I	serial test data input for BST mode
GND	8	S	ground
GND	9	S	ground
BGCAP1	10	A	pin for connecting external band gap decoupling capacitor (4 × 8 : 1 MUX)
GND	11	S	ground
V <sub>EE</sub>	12	S	supply voltage (−4.5 V)
CDIV	13	O	78 MHz clock output
V <sub>DD</sub>	14	S	supply voltage (+3.3 V)
GND	15	S	ground
V <sub>CC(T)</sub>	16	S	supply voltage for TTL buffer (+5.0 V); not connected internally to V <sub>CC</sub>
GND	17	S	ground
D31	18	I	78 Mb/s data input channel for D31
D27	19	I	78 Mb/s data input channel for D27
D23	20	I	78 Mb/s data input channel for D23
GND	21	S	ground
D19	22	I	78 Mb/s data input channel for D19
D15	23	I	78 Mb/s data input channel for D15
D11	24	I	78 Mb/s data input channel for D11
GND	25	S	ground
D7	26	I	78 Mb/s data input channel for D7
D3	27	I	78 Mb/s data input channel for D3
D30	28	I	78 Mb/s data input channel for D30
D26	29	I	78 Mb/s data input channel for D26
D22	30	I	78 Mb/s data input channel for D22
D18	31	I	78 Mb/s data input channel for D18
D14	32	I	78 Mb/s data input channel for D14
D10	33	I	78 Mb/s data input channel for D10
D6	34	I	78 Mb/s data input channel for D6
D2	35	I	78 Mb/s data input channel for D2
GND	36	S	ground
V <sub>DD</sub>	37	S	supply voltage (+3.3 V)
REFC2	38	A	pin for connecting external reference decoupling capacitor (3.3 V CMOS reference)
V <sub>EE</sub>	39	S	supply voltage (−4.5 V)

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SYMBOL	PIN	TYPE <sup>(1)</sup>	DESCRIPTION
GND	40	S	ground
D29	41	I	78 Mbits/s data input channel for D29
D25	42	I	78 Mbits/s data input channel for D25
D21	43	I	78 Mbits/s data input channel for D21
D17	44	I	78 Mbits/s data input channel for D17
D13	45	I	78 Mbits/s data input channel for D13
D9	46	I	78 Mbits/s data input channel for D9
D5	47	I	78 Mbits/s data input channel for D5
D1	48	I	78 Mbits/s data input channel for D1
D28	49	I	78 Mbits/s data input channel for D28
D24	50	I	78 Mbits/s data input channel for D24
D20	51	I	78 Mbits/s data input channel for D20
D16	52	I	78 Mbits/s data input channel for D16
D12	53	I	78 Mbits/s data input channel for D12
D8	54	I	78 Mbits/s data input channel for D8
D4	55	I	78 Mbits/s data input channel for D4
GND	56	S	ground
D0	57	I	78 Mbits/s data input channel for D0
SYNSEL2	58	I	selection input 2 for synchronization pulse timing
SYNSEL1	59	I	selection input 1 for synchronization pulse timing
V <sub>CC</sub>	60	S	supply voltage (+5.0 V)
REFC1	61	A	pin for connecting external reference decoupling capacitor (for standard TTL reference)
ENL	62	I	loop mode enable (active LOW)
V <sub>DD</sub>	63	S	supply voltage (+3.3 V)
GND	64	S	ground
DLOOP	65	O	data output to demultiplexer IC OQ2536 (loop mode)
DLOOPQ	66	O	inverted data output to demultiplexer IC OQ2536 (loop mode)
GND	67	S	ground
CLOOP	68	O	clock output to demultiplexer IC OQ2536 (loop mode)
CLOOPQ	69	O	inverted clock output to demultiplexer IC OQ2536 (loop mode)
GND	70	S	ground
CIN	71	I	clock input from VCO IC
CINQ	72	I	inverted clock input from VCO IC
GND	73	S	ground
DIOA	74	A	anode of temperature diode array
DIOC	75	A	cathode of temperature diode array
GND	76	S	ground
GND	77	S	ground
BGCAP2	78	A	pin for connecting external band gap decoupling capacitor (4 : 1 MUX)
GND	79	S	ground

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SYMBOL	PIN	TYPE <sup>(1)</sup>	DESCRIPTION
GND	80	S	ground
GND	81	S	ground
COOUT	82	O	clock output to laser driver IC
COOUTQ	83	O	inverted clock output to laser driver IC
GND	84	S	ground
V <sub>DD</sub>	85	S	supply voltage (+3.3 V)
V <sub>DD</sub>	86	S	supply voltage (+3.3 V)
V <sub>EE</sub>	87	S	supply voltage (-4.5 V)
V <sub>EE</sub>	88	S	supply voltage (-4.5 V)
GND	89	S	ground
DOOUT	90	O	data output to laser driver IC
DOOUTQ	91	O	inverted data output to laser driver IC
GND	92	S	ground
GND	93	S	ground
GND	94	S	ground
GND	95	S	ground
GND	96	S	ground
GND	97	S	ground
GND	98	S	ground
i.c.	99	-	internally connected, to be left open-circuit
GND	100	S	ground

**Note**

1. Pin type abbreviations: O = Output, I = Input, S = power Supply, A = Analog function.

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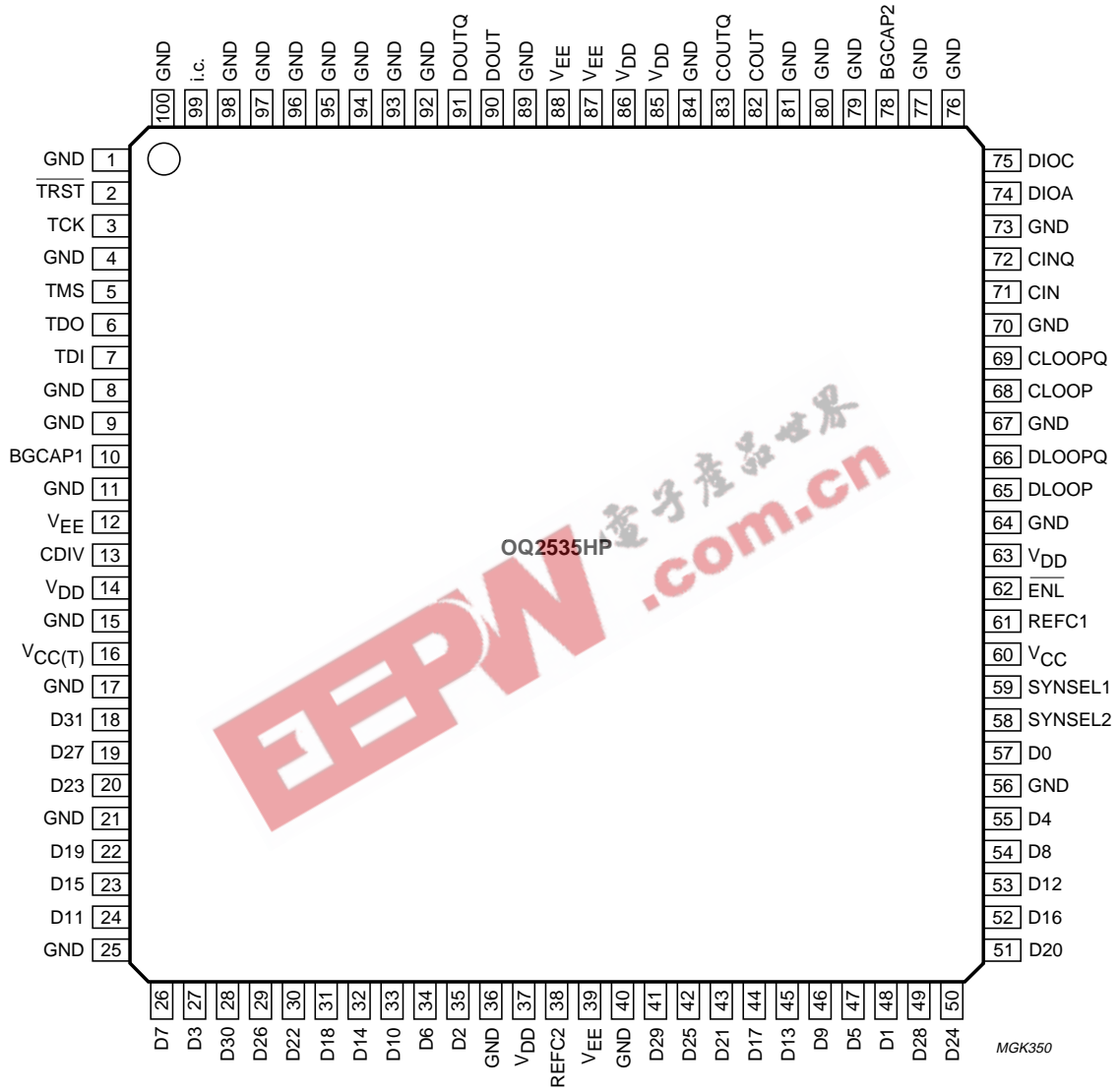


Fig.2 Pin configuration.

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**FUNCTIONAL DESCRIPTION**

The OQ2535HP is a 32-channel multiplexer intended for use in STM16/OC48 applications. It multiplexes  $32 \times 78$  Mbits/s input channels onto a single 2.5 Gbits/s output channel.

The multiplexing is performed in two stages. The 32 input channels are fed into four 8 : 1 multiplexers to generate four 622 Mbits/s channels. These four channels are then combined into a single 2.5 Gbits/s data stream.

The  $\overline{\text{ENL}}$  control input is used for switching between normal and loop modes. When loop mode is enabled, ( $\overline{\text{ENL}} = \text{LOW}$ ), the output signal is switched to DLOOP and DLOOPQ (these outputs could be connected to the DLOOP and DLOOPQ inputs on the OQ2536HP demultiplexer to form part of a test loop).

The 2.5 GHz clock at CIN and CINQ is used as the system reference. It is divided down to 78 MHz and made available on the CDIV TTL output for timing the input data (D0 to D31).

**Low bit rate stage: 4 × 8 : 1 MUX**

This part of the circuit consists of four 8-bit shift registers, each acting as an 8 : 1 multiplexer, together with a synchronization block.

The 32 data input signals are loaded into the shift registers before being shifted out on a 622 MHz clock.

The load pulse for the shift registers is generated in the synchronization block. The inputs SYNSEL1 and SYNSEL2 can be used to adjust the phase of the load pulse with respect to the input data (see Table 3) to synchronize the data and clock signals.

**High bit rate stage: 4 : 1 MUX**

The four 622 Mbits/s data outputs from the low bit rate stage are combined into a single 2.5 Gbits/s data stream in two stages: two 2 : 1 multiplexers are used to generate two 1244 Mbits/s data streams; these signals are then fed into a third 2 : 1 multiplexer to generate the 2.5 Gbits/s data stream.

The 2.5 Gbits/s serial data stream is passed either to the DOUT and DOUTQ outputs (normal mode), or to the DLOOP and DLOOPQ outputs (loop mode). The output sequence is D31 (MSB) to D0 (LSB). Data and clock output buffers are terminated internally with 100  $\Omega$  resistors to GND and are capable of driving 50  $\Omega$  loads. The unused output buffers are switched off to help minimize power dissipation.

The outputs CLOOP, CLOOPQ, DLOOP and DLOOPQ are terminated internally with 100  $\Omega$  resistors to GND and are specifically designed to drive 50  $\Omega$  printed-circuit board transmission lines.

The 2.5 GHz clock connected to CIN and CINQ is terminated internally with 50  $\Omega$  to GND.

**Power supply connections**

The power supply pins need to be individually decoupled using chip capacitors mounted as close as possible to the IC. If multiple decoupling capacitors are used for a single supply node, they must be placed close to each other to avoid RF resonance.

To minimize low frequency switching noise in the vicinity of the OQ2535HP, all power supply lines should be filtered once by an LC-circuit with a low cut-off frequency (as shown in the application diagram, Fig.6).  $V_{CC(T)}$  needs to be filtered separately via an LC-circuit because of the high switching currents present at the CDIV TTL output. As this current contains only 78 MHz harmonics, filtering can be achieved with relatively small values of L and C.

**Ground connection**

The ground connection on the printed-circuit board needs to be a large copper area fill connected to a common ground plane with low inductance.

**RF connections**

A coupled stripline or microstrip with an odd mode characteristic impedance of 50  $\Omega$  (nominal value) should be used for the RF connections on the printed-circuit board. The connections should be kept as short as possible. This applies to the CML differential line pairs CIN and CINQ, DOUT and DOUTQ, COUT and COUTQ, DLOOP and DLOOPQ, and CLOOP and CLOOPQ. In addition, the following lines should not vary in length by more than 5 mm:

- CIN and CINQ
- DOUT, DOUTQ, COUT and COUTQ
- DLOOP, DLOOPQ, CLOOP and CLOOPQ.

**Interface to transmit logic**

The 78 Mbits/s interface lines, CDIV and D0 to D31, should not vary in length by more than 20 mm. The parasitic capacitance of these lines should be as small as possible.

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**ESD protection**

All pads are protected by ESD protection diodes with the exception of the high frequency outputs DOUT, DOUTQ, DLOOP, DLOOPQ, COUT, COUTQ, CLOOP and CLOOPQ and clock inputs CIN and CINQ.

**Cooling**

In many cases it is necessary to mount a special cooling device on the package. The thermal resistance from junction to case,  $R_{th\ j-c}$  and from junction to ambient,  $R_{th\ j-a}$ , are given in Chapter "Thermal characteristics". Since the heat-slug in the package is connected to the die, the cooling device should be electrically isolated.

To calculate if a heatsink is necessary, the maximum allowed total thermal resistance  $R_{th}$  is calculated as:

$$R_{th} = \frac{T_j - T_{amb}}{P_{tot}} \tag{1}$$

where:

$R_{th}$  = total thermal resistance from junction to ambient in the application

$T_j$  = junction temperature

$T_{amb}$  = ambient temperature.

As long as  $R_{th}$  is greater than  $R_{th\ j-a}$  of the OQ2536HP including environmental conditions such as air flow and board layout, no heatsink is necessary.

For example if  $T_j = 120\text{ }^\circ\text{C}$ ,  $T_{amb} = 55\text{ }^\circ\text{C}$  and  $P_{tot} = 1.65\text{ W}$ , then:

$$R_{th} = \frac{(120 - 55)}{1.65} = 39.4\text{ K/W} \tag{2}$$

which is more than the worst case  $R_{th\ j-a} = 33\text{ K/W}$ , so no heatsink is necessary.

Another example; if for safety reasons  $T_j$  should stay as low as  $110\text{ }^\circ\text{C}$ , while  $T_{amb} = 85\text{ }^\circ\text{C}$  and  $P_{tot} = 2\text{ W}$ , then:

$$R_{th} = \frac{(110 - 85)}{2.0} = 12.5\text{ K/W} \tag{3}$$

In this case extra cooling is needed. The thermal resistance of the heatsink is calculated as follows:

$$R_{th\ h-a} \leq \left( \frac{1}{R_{th}} - \frac{1}{R_{th\ j-a}} \right)^{-1} - R_{th\ j-c} - R_{th\ c-h} \tag{4}$$

where:

$R_{th\ h-a}$  = thermal resistance from heatsink to ambient

$R_{th\ c-h}$  = thermal resistance from case to heatsink

$R_{th\ j-c}$  = thermal resistance from junction to case, see Chapter "Thermal characteristics".

If for instance  $R_{th\ c-h} = 0.5\text{ K/W}$  and  $R_{th\ j-a} = 33\text{ K/W}$  then:

$$R_{th\ h-a} \leq \left( \frac{1}{12.5} - \frac{1}{33} \right)^{-1} - 3.1 \tag{5}$$

$$\leq 17.0\text{ K/W}$$

**Built in temperature sensor**

Three series-connected diodes have been integrated for measuring junction temperature. The diode array, accessed by means of the DIOA (anode) and DIOC (cathode) pins, has a temperature dependency of approximately  $-6\text{ mV}/^\circ\text{C}$ . With a diode current of  $1\text{ mA}$ , the voltage will be somewhere in the range of  $1.7$  to  $2.5\text{ V}$ , depending on temperature.

**Boundary Scan Test (BST) interface**

Boundary scan test logic has been implemented for all digital inputs and outputs on the low frequency interface, in accordance with "IEEE Std 1149.1-1990". All scan tests other than SAMPLE mode are available. The boundary scan test logic consists of a TAP controller, a BYPASS register, a 2-bit instruction register, a 32-bit identification register and a 36-bit boundary scan register (the last two are combined). The architecture of the TAP controller and the BYPASS register is in accordance with IEEE recommendations. The four command modes, selected by means of the instruction register, are: EXTEST (00), PRELOAD (01), IDCODE (10) and BYPASS (11). All boundary scan test inputs, TDI, TMS, TCK and  $\overline{\text{TRST}}$ , have internal pull-up resistors. The maximum test clock frequency at TCK is  $12\text{ MHz}$ .

**Table 1** BST identifier code

VERSION	OQ	2535 (BINARY)	PHILIPS SEMICONDUCTORS	LSB <sup>(1)</sup>
0001	01	00 1001 1110 0111	0000 0010 101	1

**Note**

1. LSB is shifted out first on the TDO pin.



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**Table 2** BST bit order

BIT NUMBER	SYMBOL	PIN
35 (MSB)	CDIV	13
34	ENL	62
33	SYNSEL2	58
32	SYNSEL1	59
31	D31	18
30	D30	28
29	D29	41
28	D28	49
27	D27	19
26	D26	29
25	D25	42
24	D24	50
23	D23	20
22	D22	30
21	D21	43
20	D20	51
19	D19	22
18	D18	31
17	D17	44
16	D16	52
15	D15	23
14	D14	32
13	D13	45
12	D12	53
11	D11	24
10	D10	33
9	D9	46
8	D8	54
7	D7	26
6	D6	34
5	D5	47
4	D4	55
3	D3	27
2	D2	35
1	D1	48
0 (LSB) <sup>(1)</sup>	D0	57

**Note**

1. LSB is shifted out first on the TDO pin.

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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{CC}, V_{CC(T)}$	supply voltage	-0.5	+6.0	V
$V_{EE}$	supply voltage	-6.0	+0.5	V
$V_{DD}$	supply voltage	-0.5	+5.0	V
$V_n$	DC voltage			
	pins 18 to 20, 22 to 24, 26 to 35, 41 to 55 and 57	-0.5	$V_{DD} + 0.5$	V
	pins 2, 3, 5, 7, 38, 61 and 62	-0.5	$V_{CC} + 0.5$	V
	pins 65, 66, 68, 69, 71, 72, 82, 83, 90 and 91	-1.0	+0.5	V
	pins 10 and 78	$V_{EE} - 0.5$	0.5	V
	pins 74 and 75	$V_{EE} - 0.5$	$V_{CC} + 0.5$	V
$I_n$	DC current			
	pins 6 and 13	-	50	mA
	pins 74 and 75	-	10	mA
$P_{tot}$	total power dissipation	-	2.35	W
$T_j$	junction temperature	-	120	°C
$T_{stg}$	storage temperature	-65	+150	°C

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-c}$	thermal resistance from junction to case		2.6	K/W
$R_{th\ j-a}$	thermal resistance from junction to ambient	see note 1		
		airflow = 0 ft/min	33	K/W
		airflow = 100 ft/min	28	K/W
		airflow = 200 ft/min	25	K/W
		airflow = 400 ft/min	22	K/W
		airflow = 600 ft/min	20	K/W

**Note**

1. The thermal resistance from junction to ambient is strongly depending on the board design and airflow. The values given in the table are typical values and are measured on a single sided test board with dimensions of  $76 \times 114 \times 1.6$  mm. Better values can be obtained when mounted on multilayer boards with large ground planes.

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## DC CHARACTERISTICS

All typical values are at  $T_{amb} = 25\text{ °C}$  and at typical supply voltages; minimum and maximum values are valid over the entire ambient temperature range and supply voltage range.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>General</b>						
$V_{CC}, V_{CC(T)}$	supply voltage	note 1	4.75	5.0	5.25	V
$V_{EE}$	supply voltage		-4.75	-4.5	-4.25	V
$V_{DD}$	supply voltage		3.14	3.3	3.47	V
$I_{CC}$	supply current		-	2.3	4	mA
$I_{CC(T)}$	supply current		-	20	40	mA
$I_{EE}$	supply current		-	265	400	mA
$I_{DD}$	supply current		-	20	28	mA
$P_{tot}$	total power dissipation		-	1.65	2.35	W
$T_j$	junction temperature		-	-	120	°C
$T_{amb}$	ambient temperature		-40	-	+85	°C
<b>TTL 3.3 V inputs: D0 to D31; note 2</b>						
$V_{IL}$	LOW-level input voltage		-	-	0.8	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
$I_{IL}$	LOW-level input current		-65	-	0	μA
$I_{IH}$	HIGH-level input current		0	-	110	μA
<b>TTL inputs: ENL, SYNSEL1, SYNSEL2, TDI, TCK, TMS and TRST</b>						
$V_{IL}$	LOW-level input voltage		-	-	0.8	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
$I_{IL}$	LOW-level input current	note 3	-100	-	0	μA
$I_{IH}$	HIGH-level input current	note 3	0	-	210	μA
<b>CML clock inputs: CIN and CINQ; note 4</b>						
$V_{i(p-p)}$	input voltage (peak-to-peak value)	50 Ω measurement system	100	250	500	mV
$V_{IO}$	permitted input offset voltage		-25	-	+25	mV
$V_I, V_{IQ}$	input voltages		-600	-	+250	mV
$Z_i$	single ended input impedance	for DC signal	-	50	-	Ω
<b>TTL outputs: CDIV and TDO; note 5</b>						
$V_{OL}$	LOW-level output voltage	$I_{OL} = 4\text{ mA}$	-	0.3	0.5	V
$V_{OH}$	HIGH-level output voltage	$I_{OH} = -400\text{ μA}$	2.4	4.0	-	V
$I_{OZ}$	output current in high-impedance state		-	-	1	μA
<b>CML outputs in normal mode: COUT, COUTQ, DOUT and DOUTQ; note 4</b>						
$V_{o(p-p)}$	output voltage (peak-to-peak value)	outputs terminated externally with 50 Ω resistors	230	300	500	mV
$V_{OO}$	output offset voltage		-25	0	+25	mV
$V_O, V_{OQ}$	output voltages		-600	-	0	mV
$Z_o$	output impedance	for DC signal	-	100	-	Ω

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>CML outputs in loop mode: CLOOP, CLOOPQ, DLOOP and DLOOPQ; note 4</b>						
$V_{o(p-p)}$	output voltage (peak-to-peak value)	outputs terminated externally with $50\ \Omega$	230	300	500	mV
$V_{OO}$	output offset voltage		-25	0	+25	mV
$V_O, V_{OQ}$	output voltages		-600	-	0	mV
$Z_o$	output impedance	for DC signal	-	100	-	$\Omega$
<b>Temperature diode array</b>						
$\Delta V_{DIOA-DIOC}$	diode voltage range; note 6	$I_{I(d)} = 1\ \text{mA}$	-	2.1	-	V

Notes

- $V_{CC}$  and  $V_{CC(T)}$  require the same power supply voltage. However, a filter is needed to isolate  $V_{CC(T)}$  because of the high peak currents that occur at 78 MHz.
- The output sequence is D31 (MSB) to D0 (LSB).
- Only for inputs  $\overline{\text{ENL}}$ ,  $\text{SYNSEL1}$  and  $\text{SYNSEL2}$ .  $\text{TDI}$ ,  $\text{TMS}$ ,  $\text{TCK}$  and  $\overline{\text{TRST}}$  are connected to  $V_{CC}$  through  $90\ \text{k}\Omega$  resistors.
- See Fig.3 for symbol definitions.
- TDO is switched to high impedance state if BST is inactive.
- The temperature diode array can be used to measure the temperature of the die. The temperature dependency of this voltage is approximately  $-6\ \text{mV/K}$ .

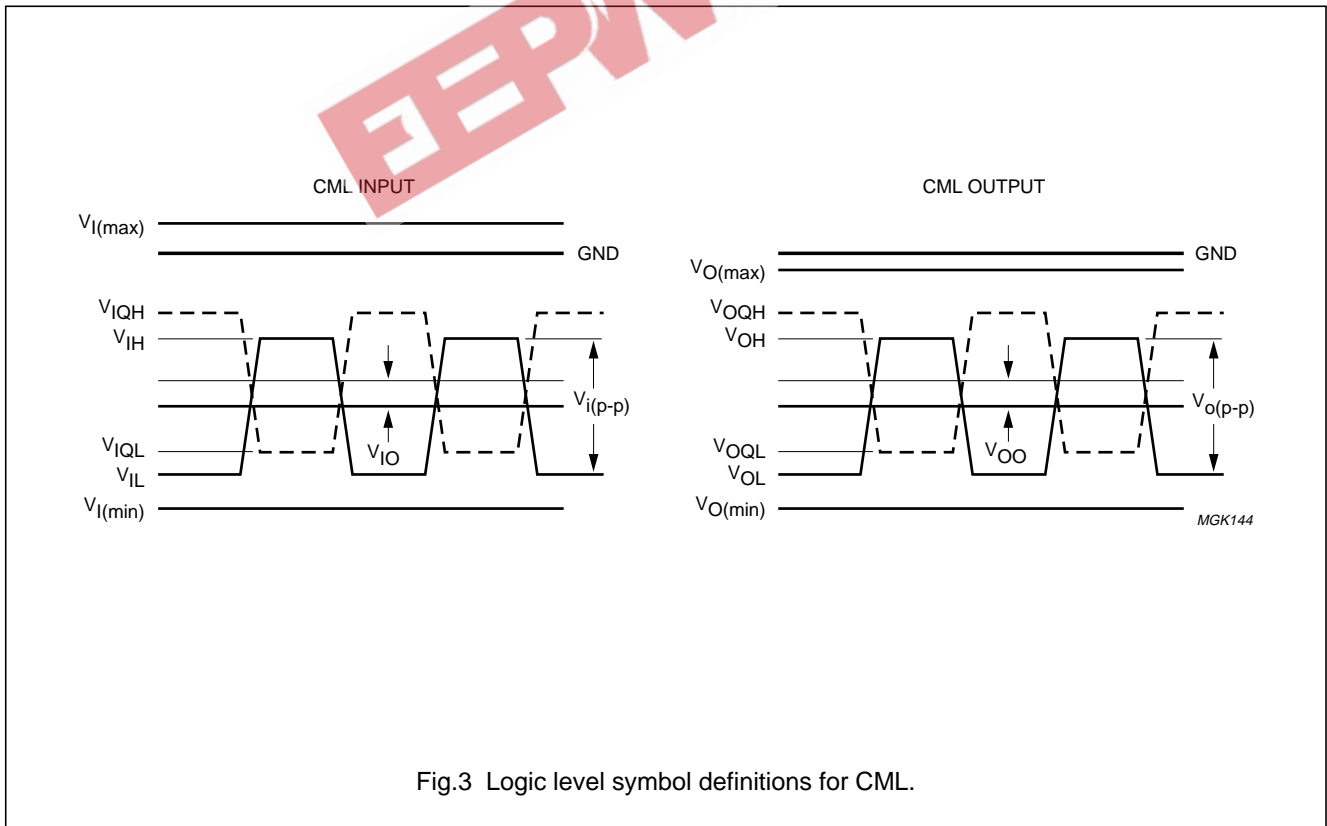


Fig.3 Logic level symbol definitions for CML.

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**TIMING**

Typical values at  $T_{amb} = 25\text{ }^{\circ}\text{C}$  and at typical supply voltages; minimum and maximum values are valid over the entire ambient temperature range and supply voltage range.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>TTL input timing</b>						
$f_{clk(CDIV)}$	low speed output clock frequency	$f_{clk(CIN)} = 2.488\text{ GHz}$	–	77.76	–	MHz
$t_{r(CDIV)}, t_{f(CDIV)}$	CDIV rise/fall time	capacitive load of 15 pF	–	–	2600	ps
$t_{su}$	input data set-up time	note 1	1200	–	–	ps
$t_h$	input data hold time	note 1	2600	–	–	ps
<b>CML output timing; note 2</b>						
$f_{clk(COUT)}$	output clock frequency	$f_{clk(CIN)} = 2.488\text{ GHz}$	–	2.488	–	GHz
$t_{CDV}$	clock edge to data valid time		–	–	250	ps
$t_{DI}$	data invalid time		–	–	120	ps
$t_{r(CML)}, t_{f(CML)}$	CML output rise/fall time		–	–	150	ps
$\delta_{COUT}$	output clock duty factor		45	50	55	%

**Notes**

1. The set-up and hold times given are valid for  $SYNSEL1 = SYNSEL2 = \text{HIGH}$ . Different  $SYNSEL1$ ,  $SYNSEL2$  combinations will produce different set-up and hold times (see Table 3).
2. All CML outputs must be terminated externally with  $50\ \Omega$  to GND. The specified timing characteristics are applicable in both normal and loop modes.

**Table 3** Timing relationship between the clock edge and the data valid region (minimum values)

SYNSEL2	SYNSEL1	$t_{su}$	$t_h$	UNIT
HIGH	HIGH	1200	2600	ps
HIGH	LOW	2800	1000	ps
LOW	HIGH	1700	2100	ps
LOW	LOW	3300	500	ps

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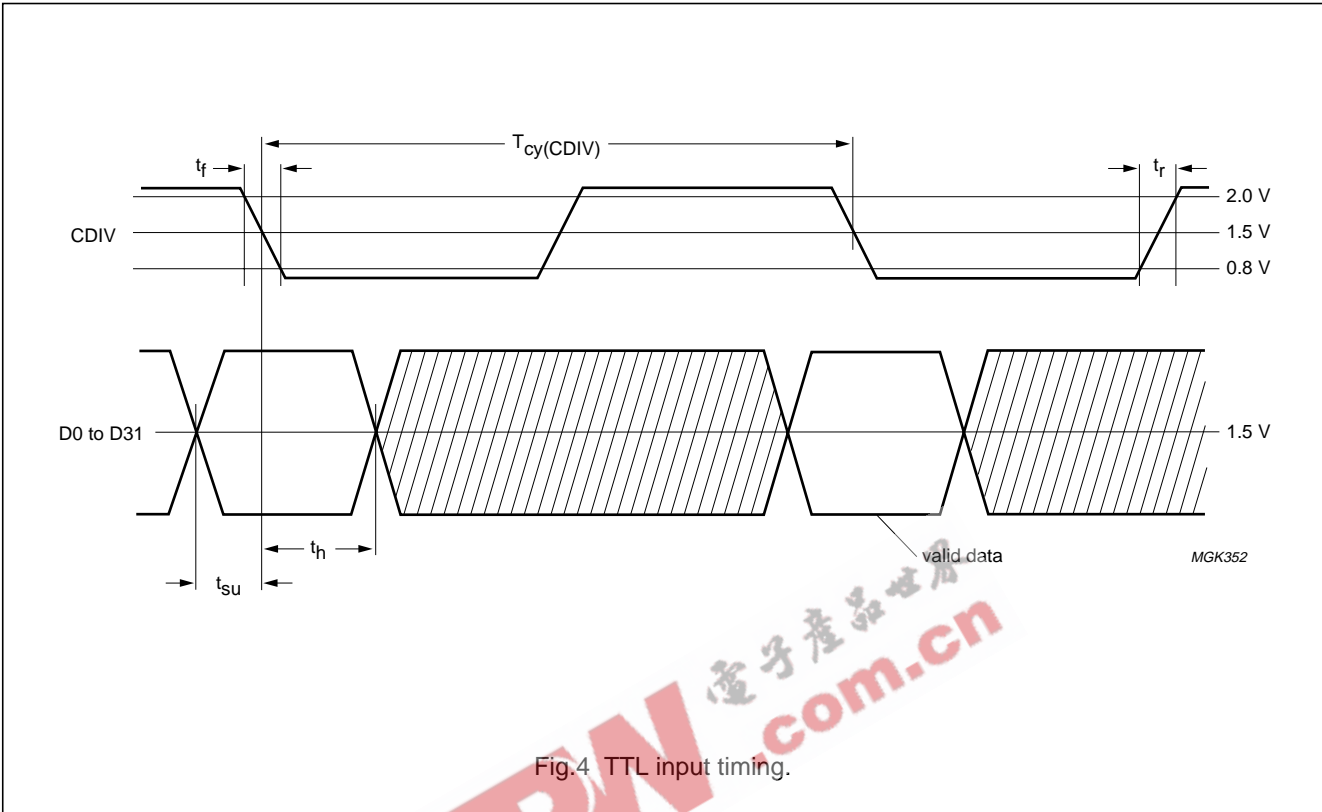


Fig.4 TTL input timing.

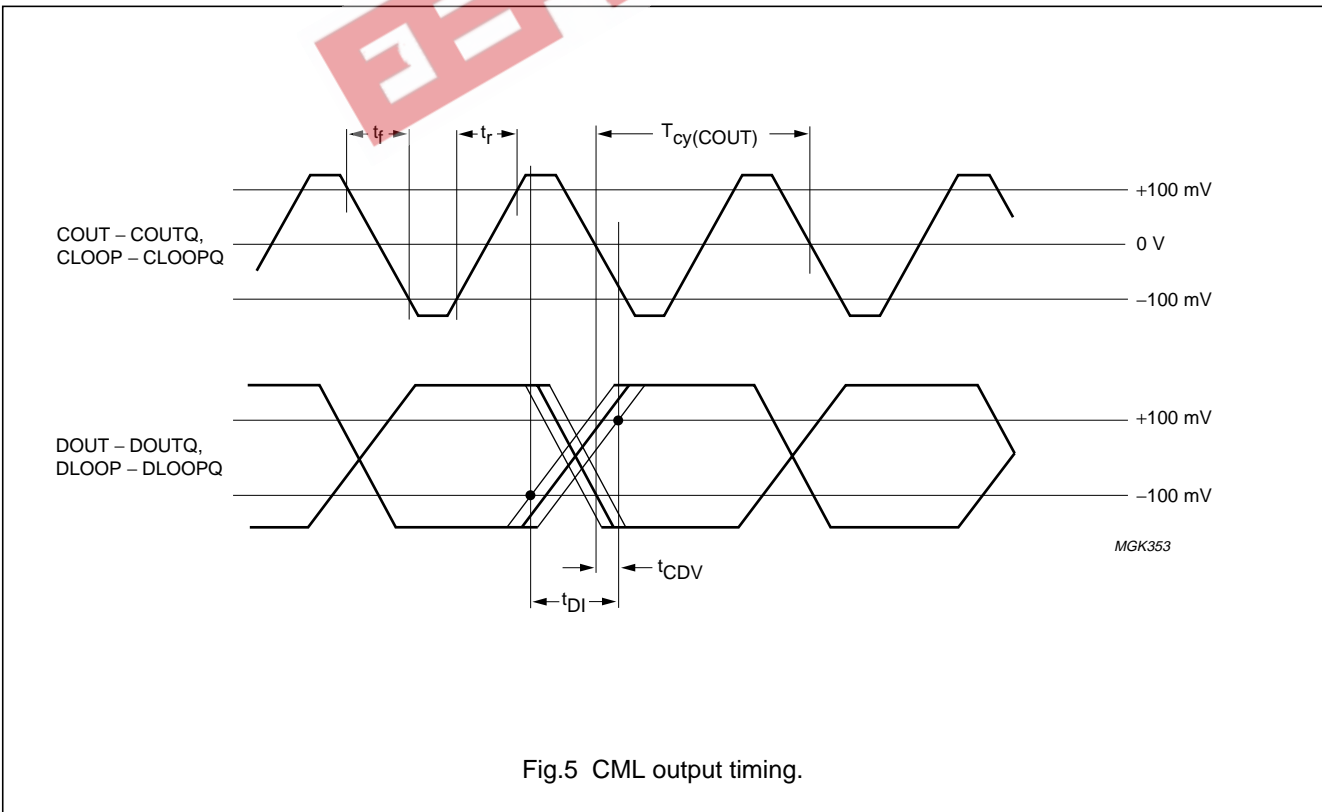


Fig.5 CML output timing.

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APPLICATION INFORMATION

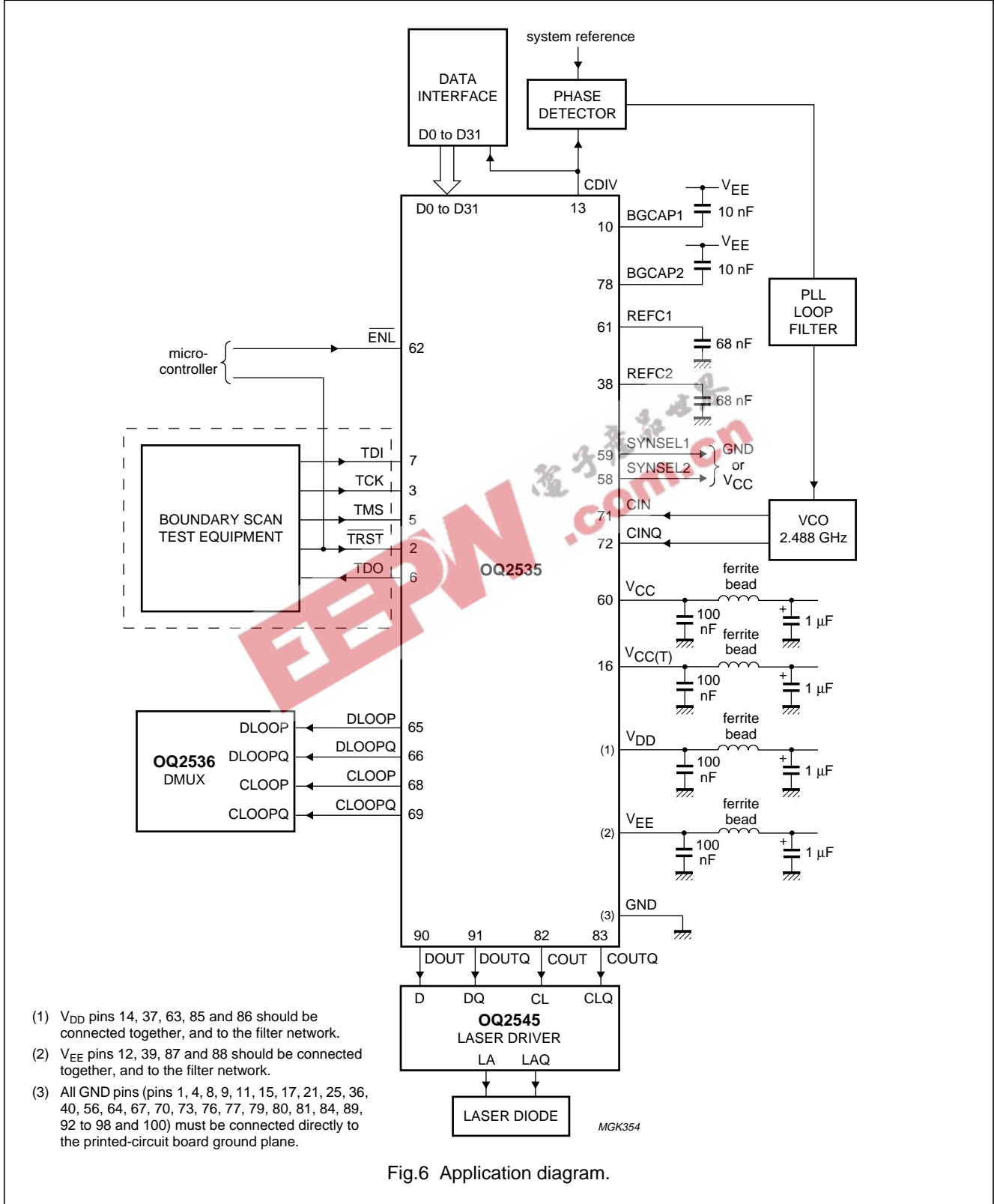


Fig.6 Application diagram.

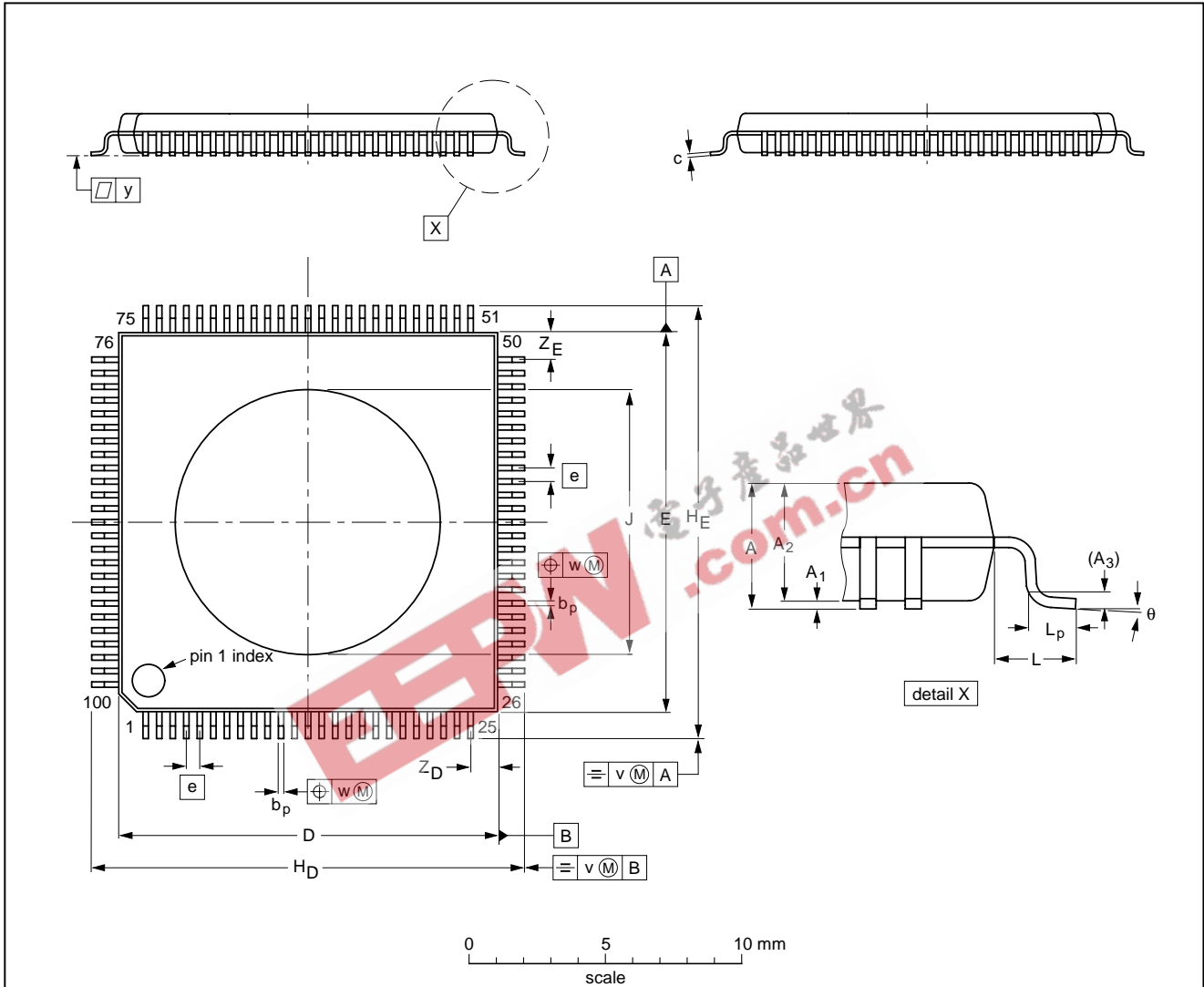
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PACKAGE OUTLINE

HLQFP100: plastic heat-dissipating low profile quad flat package;  
100 leads; body 14 x 14 x 1.4 mm

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DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>D</sub>	H <sub>E</sub>	J <sup>(2)</sup>	L	L <sub>p</sub>	v	w	y	Z <sub>D</sub> <sup>(1)</sup>	Z <sub>E</sub> <sup>(1)</sup>	θ
mm	1.6	0.20 0.05	1.5 1.3	0.25	0.28 0.16	0.18 0.12	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	10.15 9.15	1.0	0.75 0.45	0.2	0.12	0.1	1.15 0.85	1.15 0.85	7° 0°

Notes

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.
2. Heatsink intrusion 0.0127 maximum.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT470-1						97-01-13



## SDH/SONET STM16/OC48 multiplexer

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**SOLDERING****Introduction to soldering surface mount packages**

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "Data Handbook IC26; Integrated Circuit Packages" (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

**Reflow soldering**

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

**Wave soldering**

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

**Manual soldering**

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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## Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW <sup>(1)</sup>
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable <sup>(2)</sup>	suitable
PLCC <sup>(3)</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>(3)(4)</sup>	suitable
SSOP, TSSOP, VSO	not recommended <sup>(5)</sup>	suitable

## Notes

- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
- These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

## DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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# Philips Semiconductors – a worldwide company

**Argentina:** see South America

**Australia:** 3 Figtree Drive, HOMEBUSH, NSW 2140,  
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213,  
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,  
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

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**Bulgaria:** Philips Bulgaria Ltd., Energoproject, 15th floor,  
51 James Bourchier Blvd., 1407 SOFIA,  
Tel. +359 2 68 9211, Fax. +359 2 68 9102

**Canada:** PHILIPS SEMICONDUCTORS/COMPONENTS,  
Tel. +1 800 234 7381, Fax. +1 800 943 0087

**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre,  
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,  
Tel. +852 2319 7888, Fax. +852 2319 7700

**Colombia:** see South America

**Czech Republic:** see Austria

**Denmark:** Sydhavnsgade 23, 1780 COPENHAGEN V,  
Tel. +45 33 29 3333, Fax. +45 33 29 3905

**Finland:** Sinikalliontie 3, FIN-02630 ESPOO,  
Tel. +358 9 615 800, Fax. +358 9 6158 0920

**France:** 51 Rue Carnot, BP317, 92156 SURESNES Cedex,  
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG,  
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

**Hungary:** see Austria

**India:** Philips INDIA Ltd, Band Box Building, 2nd floor,  
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,  
Tel. +91 22 493 8541, Fax. +91 22 493 0966

**Indonesia:** PT Philips Development Corporation, Semiconductors Division,  
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,  
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

**Ireland:** Newstead, Clonskeagh, DUBLIN 14,  
Tel. +353 1 7640 000, Fax. +353 1 7640 200

**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,  
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

**Italy:** PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),  
Tel. +39 039 203 6838, Fax +39 039 203 6800

**Japan:** Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,  
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

**Korea:** Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,  
Tel. +82 2 709 1412, Fax. +82 2 709 1415

**Malaysia:** No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,  
Tel. +60 3 750 5214, Fax. +60 3 757 4880

**Mexico:** 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,  
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

**Middle East:** see Italy

**Netherlands:** Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,  
Tel. +31 40 27 82785, Fax. +31 40 27 88399

**New Zealand:** 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,  
Tel. +64 9 849 4160, Fax. +64 9 849 7811

**Norway:** Box 1, Manglerud 0612, OSLO,  
Tel. +47 22 74 8000, Fax. +47 22 74 8341

**Pakistan:** see Singapore

**Philippines:** Philips Semiconductors Philippines Inc.,  
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,  
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

**Poland:** Al.Jerozolimskie 195 B, 02-222 WARSAW,  
Tel. +48 22 5710 000, Fax. +48 22 5710 001

**Portugal:** see Spain

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**Russia:** Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,  
Tel. +7 095 755 6918, Fax. +7 095 755 6919

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**South Africa:** S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,  
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,  
Tel. +27 11 471 5401, Fax. +27 11 471 5398

**South America:** Al. Vicente Pinzon, 173, 6th floor,  
04547-130 SÃO PAULO, SP, Brazil,  
Tel. +55 11 821 2333, Fax. +55 11 821 2382

**Spain:** Balmes 22, 08007 BARCELONA,  
Tel. +34 93 301 6312, Fax. +34 93 301 4107

**Sweden:** Kottbygatan 7, Akalla, S-16485 STOCKHOLM,  
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**Switzerland:** Allmendstrasse 140, CH-8027 ZÜRICH,  
Tel. +41 1 488 2741 Fax. +41 1 488 3263

**Taiwan:** Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,  
TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

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209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,  
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**Turkey:** Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,  
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,  
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes,  
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

**United States:** 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,  
Tel. +1 800 234 7381, Fax. +1 800 943 0087

**Uruguay:** see South America

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**Yugoslavia:** PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,  
Tel. +381 11 62 5344, Fax.+381 11 63 5777

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