DATA SHEET

OQ8868
Digital Servo Integrated Circuit Silent (DSICS)

Product specification
Supersedes data of 1996 Apr 11
File under Integrated Circuits, IC01

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Philips Semiconductors

PHILIPS

Digital Servo Integrated Circuit Silent (DSICS) OQ8868

FEATURES

The DSICS realizes the following servo functions:

- Focus servo loop
- Radial servo loop
- Built-in access procedure
- Sledge motor servo loop
- Three line (TDA1301T-like; same on hardware level, coefficients differ) or I²C-bus serial interface with system controller.

Other features are:

- Single supply voltage (5 V)
- Flexible system oscillator
- Usable for single/double Foucault and astigmatic focus
- Wide range of adjustable servo characteristics possible
- Automatic focus start-up procedure and in-lock indication
- Fast focus restart procedure
- Sophisticated track loss detection mechanism
- Extended radial error signal
- Automatic initialization and jump procedure for radial servo
- Automatic radial error gain and offset control
- Sophisticated defect detector
- Shock detector
- Fast serial communication
- Low noise servo loops
- Automatic gain control for the complete focus and radial loop
- Fast track counting signal input
- Steered sledge jump
- Radial actuator damping.

Features that improve on its predecessor, the TDA1301T:

- Low noise in the focus loop
- Faster serial communication
- Improved jump performance.

Added features are:

- High level watchdogs
- Decoder (LO9585, LO9588 or HD60) communication support
- Application debugging support
- Pulsed sledge mode
- Auto gain control on radial and focus loop
- I²C-bus serial communication
- Externally available defect detector signals.

GENERAL DESCRIPTION

The Digital Servo Integrated Circuit Silent (DSICS) IC provides all servo functions except the spindle motor control in two-stage Compact Disc (CD) systems. It offers a high degree of integration, combined with the low additional cost of external components. The servo characteristics are widely adjustable by means of a three-wire serial interface, which offers great flexibility for the application of different CD mechanisms.

The servo chip accepts diode currents and drives various power stages. Proper functioning of the focus and radial AGCs requires a digital power stage (SZA1010). It can drive normal, CDM12-like, mechanisms.

It is the improved version of its predecessor, the DSIC2 (TDA1301).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OQ8868	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		4.5	–	5.5	V
V_{DDA}	analog supply voltage		4.5	–	5.5	V
I_{DDD}	digital supply current		–	17	–	mA
$I_{DD(q)}$	digital quiescent supply current		–	–	10	µA
I_{DDA}	analog supply current		–	5	–	mA
I_I	input current					
	for pins D1 to D4	note 1	–	–	12	µA
	for pins S1 and S2	note 2	–	–	6	µA
P_{tot}	total power dissipation		–	115	–	mW
T_{amb}	operating ambient temperature		–40	–	+85	°C

Notes

1. Maximum input range varies from 3.8 to 12 µA and varies with the reference current through XTLR.
2. Maximum input range varies from 1.9 to 6 µA and varies with the reference current through XTLR.

BLOCK DIAGRAM

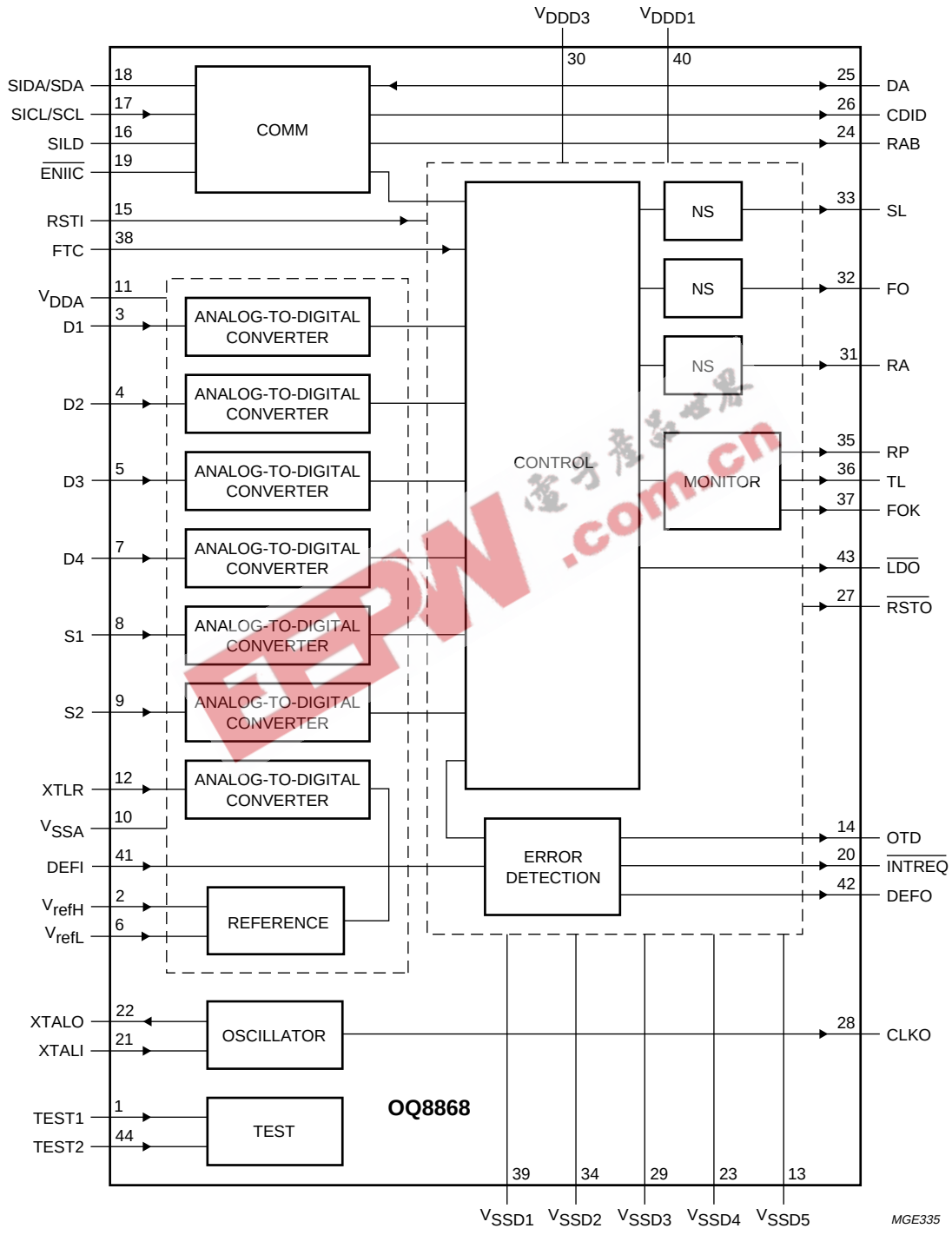


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TEST1	1	test input 1 (LOW for normal operation); internal pull-down
V_{refH}	2	high reference for A/D converter (input)
D1	3	unipolar current input (central diode signal input)
D2	4	unipolar current input (central diode signal input)
D3	5	unipolar current input (central diode signal input)
V_{refL}	6	low reference for A/D converter (input)
D4	7	unipolar current input (central diode signal input)
S1	8	unipolar current input (central diode signal input)
S2	9	unipolar current input (central diode signal input)
V_{SSA}	10	analog ground
V_{DDA}	11	analog supply voltage
XTLR	12	reference current input
V_{SSD5}	13	digital ground 5
OTD	14	off track detector (output)
RSTI	15	reset input (active HIGH)
SILD	16	serial host interface load
SICL/SCL	17	serial host interface clock /I^2C-bus clock (SCL)
SIDA/SDA	18	serial host interface data /I^2C-bus data (SDA)
$\overline{\text{ENIIC}}$	19	enable I^2C-bus serial format (active LOW)
$\overline{\text{INTREQ}}$	20	interrupt request output (active LOW)
XTALI	21	oscillator input
XTALO	22	oscillator output
V_{SSD4}	23	digital ground 4
RAB	24	serial decoder interface load (output)
DA	25	serial decoder interface data (input/output)
CDIC	26	serial decoder interface clock (output)
$\overline{\text{RSTO}}$	27	reset output (active LOW)
CLKO	28	clock buffer output
V_{SSD3}	29	digital ground 3
V_{DDD3}	30	digital supply voltage 3
RA	31	radial actuator output
FO	32	focus actuator output
SL	33	sledge output
V_{SSD2}	34	digital ground 2
RP	35	radial polarity signal
TL	36	track loss signal
FOK	37	focus OK output
FTC	38	fast track counting input (internal pull-down)
V_{SSD1}	39	digital ground
V_{DDD1}	40	digital supply voltage 1

SYMBOL	PIN	DESCRIPTION
DEFI	41	defect detector input (connected to DEFO)
DEFO	42	defect detector output
$\overline{LDO}$	43	laser drive on output (open drain, active LOW)
TEST2	44	test input 2 (low for normal operation)

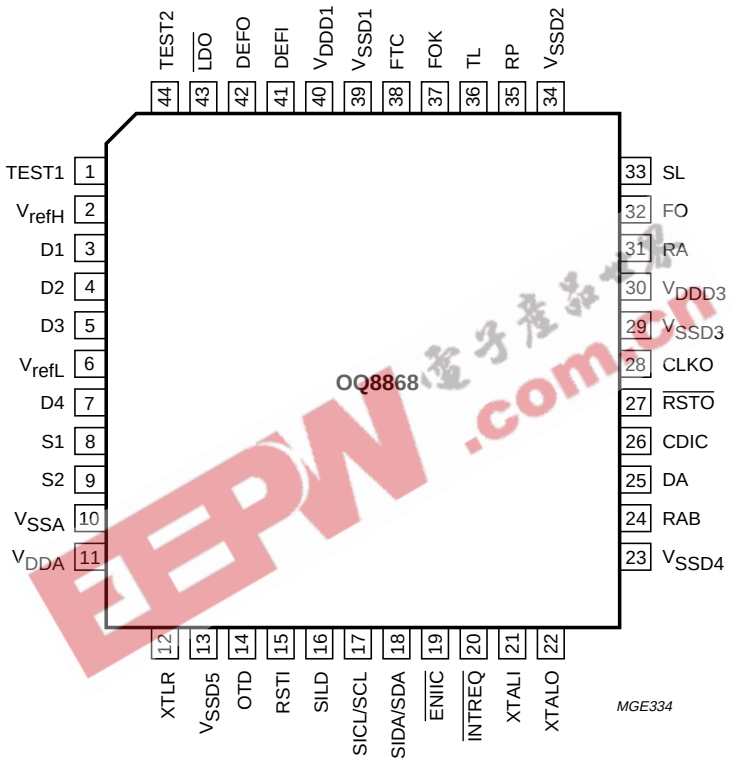


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Servo input circuits

This IC has been designed for Compact Disc drives for audio and data applications and uses diode currents as input signals.

The analog signals from the diode pre-processor are converted into a digital representation using analog-to-digital (A/D) converters.

Signal conditioning

The digital codes retrieved from the A/D converters are connected to a logic circuit, to obtain the various control signals. The signals from the central aperture detectors are processed in such a way that the following normalized focus error signal is generated:

$$FE_n = \frac{D1 - D2}{D1 + D2} - \frac{D3 - D4}{D3 + D4}$$

where the detector set-up is assumed as shown in Fig.3.

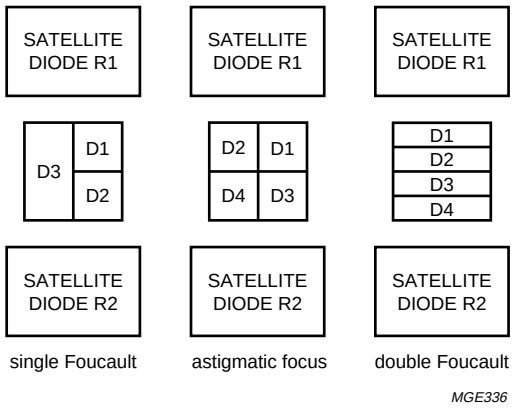


Fig.3 Detector arrangement.

For the single Foucault focusing method, the DSICS signal conditioning can be switched under software control so that the signal processing is as follows:

$$FE_n = 2 \times \frac{D1 - D2}{D1 + D2}$$

The FE_n thus obtained is further processed by a Proportional Integral and Differential (PID) filter section. A focus OK (FOK) flag is generated by means of the central aperture signal and an adjustable reference level. This signal is used to provide extra protection for the TL generation, and also for the focus start-up procedure and the drop-out detection.

The radial or tracking error signal is generated by means of the satellite detector signals S1and S2. The radial error signal can be formulated as follows:

$RE_s = (S1 - S2) \times RE\_gain + (S1 + S2) - RE\_offset$

where the index ‘s’ indicates the automatic scaling operation that is performed on the radial error signal. This scaling is necessary to avoid non-optimum dynamic range usage in the digital representation and reduces radial bandwidth spread. Furthermore, the radial error signal will be made free from offset during start-up of the disc.

The four signals from the central aperture detectors, together with the satellite detector signals, generate a track position indication (TPI) signal. This can be formulated as follows:

$TPI = sign[(D1 + D2 + D3 + D4) - (S1 + S2) \times Sum\_gain]$

where the weighting factor Sum_gain is generated internally in the DSICS during initialization.

Servo output circuits

The Off Track Detection (OTD) signal indicates an off track situation. The polarity of this signal is programmable. During active radial tracking, OTD is realized by continuously monitoring the off track counter value. The off track flag becomes valid whenever the off track counter value is not equal to zero. Depending on the type of extended S-curve, the off track counter is reset after ¾ extend or at the original track in the 2¼ track extend mode.

The control signals for the different actuators (FO, RA and SL) are 1-bit noise-shaped digital outputs at 1.0584 MHz (DSD mode). At 2.1168 MHz, noise-shaped signals can also be selected.

An analog representation of the output signals can be achieved by connecting a first-order low-pass filter to the outputs.

Focus control

The DSICS digital controller includes the following focus servo functions:

1. Focus start-up
2. Focus position control loop
3. Dropout detection
4. Focus loss detection and fast restart
5. Focus loop gain switching
6. Focus automatic gain control loop.

Focus start-up

Five initially-loaded coefficients influence the start-up behaviour of the focus controller. The automatically generated triangle voltage can be influenced by three parameters for the height (ramp_height) and DC-offset (ramp_offset) of the triangle and its steepness (ramp_inc).

For protection against false focus point detections, two parameters are available, these being an absolute level on the CA signal (CA_start) and a level on the FE_n signal (FE_start).

When this CA level is reached, the FOK signal becomes true. If this FOK signal is true and the level on the FE_n signal is reached, the focus PID is enabled to switch on when the next zero crossing is detected in the FE_n signal.

Focus position control loop

The focus control loop contains a digital PID controller, which has five parameters available to the user. These coefficients influence the integrating (foc_int), proportional (foc_prop) and differentiating (foc_pole_lead) action of this PID and a digital low-pass filter (foc_pole_noise) following the PID. The fifth coefficient (foc_gain) influences the loop gain.

Dropout detection

This detector can be influenced by one parameter (CA_drop). The FOK signal will become false and the PID integrator will hold if the CA signal drops below this programmable absolute CA level. When the FOK signal becomes false, it is assumed initially that this is caused by a black dot.

Focus loss detection and fast restart

Whenever FOK is false for longer than approximately 3 ms, it is assumed that the focus point is lost. A fast restart procedure is initiated, which is capable of restarting the focus loop within 200 to 300 ms, depending on the microprocessor-programmed coefficients.

Focus loop gain switching

The gain of the focus control loop (foc_gain) can be multiplied by a factor of 2 or divided by 2 during normal operation. The integrator value of the PID is corrected accordingly. The differentiating (foc_pole_lead) action of the PID can be switched at the same time when gain switching is performed.

Focus automatic gain control loop

The loop gain of the focus control loop can be corrected automatically to eliminate tolerances in the focus loop. This gain control injects a signal into the loop that is used to correct the loop gain. Since this decreases the optimum performance, the gain control should only be activated briefly, e.g. when starting a new disc.

Radial control

The DSICS digital controller includes the following radial servo functions:

1. Level initialization
2. Sledge home
3. Tracking control
4. Access
5. Radial automatic gain control loop.

Level initialization

During start-up, an automatic adjustment procedure is activated, to set the values of the radial error gain (RE_gain), offset (RE_offset) and satellite sum signal gain (Sum_gain) for TPI level generation. The initialization procedure runs in a radial open loop situation and is ≤300 ms. This start-up time period may coincide with the last part of the turntable motor start-up time period.

Automatic gain adjustment: As a result of this initialization, the amplitude of the RE signal is adjusted within ±10% around the nominal RE amplitude.

Offset adjustment: The additional offset in RE due to the limited accuracy of the start-up procedure is less than ±50 nm.

TPI level generation: The accuracy of the initialization procedure is such that the duty cycle range of TPI becomes 0.4 < duty cycle < 0.6. Duty cycle definition: TPI-HIGH/TPI-period).

Sledge home

The sledge moves to a reference position (end_stop_switch) at the inner side of the disc with user-defined voltage.

TRACKING CONTROL

The actuator is controlled using a PID loop filter with user-defined coefficients and gain. For stable operation between the tracks, the S-curve is extended over ±¾ track.

Upon a request from the microprocessor, S-curve extension over ±2¼ tracks is used, automatically changing to access control when exceeding those 2¼ tracks.

Both modes of S-curve extension make use of a track-count mechanism, as described in section “Off track counting”. In this mode, track counting results in automatic ‘return to zero track’, to avoid major music rhythm disturbances in the audio output for improved shock resistance. The sledge is continuously controlled using the filtered value of the integrator contents of the actuator, or upon request by the microprocessor. The microprocessor can read out this integrator value and provides the sledge with step pulses to reduce power consumption. Filter coefficients of the continuous sledge control can be preset by the user.

ACCESS

The access procedure is divided into two different modes, depending on the requested jump size (see Table 1).

The access procedure makes use of a track counting mechanism (see section “Off track counting”), a velocity signal based upon the number of tracks passed within a fixed time interval, a velocity setpoint calculated from the number of tracks to go and a user-programmable parameter indicating the maximum sledge performance.

If the number of tracks to go is larger than break_dist, then the Sledge jump mode is activated; otherwise, the actuator jump is performed. The requested jump size, together with the required sledge braking distance at maximum access speed, defines the value break_dist.

During the actuator jump mode, velocity control with a PI controller is used for the actuator. The sledge is then continuously controlled using the filtered value of the integrator contents of the actuator. All filter parameters (for actuator and sledge) are user-programmable.

In the sledge jump mode, maximum power (user-programmable) is applied to the sledge in the correct direction, while the actuator becomes idle; the contents of the actuator integrator leaks to zero just after the sledge jump mode is initiated.

Table 1 Access modes

ACCESS TYPE	JUMP SIZE	ACCESS SPEED
Actuator jump	1 – break_distance(1)	decreasing velocity
Sledge jump	break distance(1) – 32768	maximum power to sledge(1)

Note

1. Can be preset by the microcontroller.

RADIAL AUTOMATIC GAIN CONTROL LOOP

The loop gain of the radial control loop can be corrected automatically to eliminate tolerances in the radial loop. This gain control injects a signal into the loop, which is used to correct the loop gain. Since this decreases the optimum performance, the gain control should only be activated briefly (e.g. when starting a new disc).

This gain control differs from the 'level initialization' previously mentioned. This level initialization should be performed first. The disadvantage of the level initialization without the gain control is that only tolerances from the front-end are reduced.

Off track counting

TPI is a flag that is used to indicate whether the spot is positioned on the track, with a margin of ±¼ of the track-pitch. In combination with the RP-flag (radial polarity; pin 35) the relative spot position over the tracks can be determined.

These signals are affected by some uncertainties, caused by:

- Disc defects, such as scratches and fingerprints
- The high-frequency (HF) information on the disc, which is seen as noise by the detector signals.

In order to determine the spot position with sufficient accuracy, extra conditions are necessary to generate a TL signal as well as an off track counter value. These extra conditions influence the maximum speed and this implies that one of the three following counting states is selected internally:

- **Protected state:** used in normal play situations. In this state, a good protection against false detection caused by disc defects is important.
- **Slow counting state:** used in low velocity track jump situations. In this state, a fast response is important, rather than the protection against disc defects. (If the phase relationship between TL and RP of a ½π rad is affected too much, the direction can no longer be determined accurately.
- **Fast counting state:** used in high velocity track jump situations. The highest obtainable velocity is the most important feature in this state, in which counting on internally generated signals or on the Fast Track Count (FTC) input signal is possible.

Defect detection

Because of the possible defects previously mentioned (fingerprints, etc.), a defect detection circuit is incorporated into the DSICS. Whenever this circuit detects a defect, it will hold all radial and focus controls. This circuit improves the playability of the application (black dot performance, etc.) and is programmable, to optimize it for specific disc defects. The actions of this circuit can be monitored on the DEFO pin (active HIGH).

An external defect detection circuit can be added by removing the connection between DEFO and DEFI (normal operation) and connecting the external circuitry.

These signals are affected by some uncertainties caused by:

- Disc defects, such as scratches and fingerprints
- The HF information on the disc, which is seen as noise by the detector signals.

Off track detection

During active radial tracking, off track detection is realized by continuously monitoring the off track counter value. The off track detector (OTD) flag becomes valid whenever the off track counter value is not equal to zero. Depending on the type of extended S-curve, the off track counter is reset after ¾ extend or at the original track in the 2¼ track extend mode.

Serial host Interface

To control DSICS operation, a serial interface is implemented. This serial interface allows communication with a microcontroller via a 3-line or 2-line serial bus. In the 2 line, I²C-bus mode, it consists of:

- Clock line SCL (SICL/SCL pin)
- Data line SDA (SIDA/SDA pin).

In the 3-line, TDA1301T-like mode, it consists of:

- Clock line SICL (SICL/SCL pin)
- Data line SIDA (SIDA/SDA pin)
- Control line SILD.

The SICL line is controlled by the microcontroller and can be completely asynchronous from the DSICS oscillator frequency. The SILD line is used for read/write control and end-of-byte signalling.

The communication is bi-directional and processes 8-bit words (byte, MSB first). The data present on SIDA is clocked with the positive edge of SICL. A single information exchange consists of one command byte and up to seven data bytes.

The first byte defines the command, and is always input to the DSICS. This byte defines whether data has to be written to or read from the DSICS. If data has to be written to the DSICS, this byte also specifies the number of data bytes. The number of bytes read from the DSICS can vary from 0 to 128 and only depends on how many the microcontroller wants to read.

Serial decoder interface

The DSICS is able to control the decoder (SAA7345) through a second serial interface. If this connection is made, high-level features such as auto start-up and interrupt on subcode discontinuity can be used. In this case, the microcontroller has to communicate through the DSICS to the decoder.

The interface to the decoder is a 3-line serial bus comprising the following signals:

- Clock line (CDIC)
- Data line (DA)
- Control line (RAB).

The serial bus is fully controlled by the DSICS, although it can be disabled by the microcontroller.

Clock generation

The DSICS should run internally with a clock of 8.4672 MHz. The circuit that generates the clock has three modes: the oscillator frequency divided by 2, 3 or 4 (software controlled). Therefore, it is possible to connect a crystal or a resonator with a frequency of 8.4672, 11.2896 or 16.9344 MHz. For the best performance, use of the 16.9344 MHz input frequency is recommended for 8× applications. For higher speeds the next clock frequencies are recommended:

- 22.0147 MHz for 10 × CD-ROM data rate (8 × clock frequency +30%)
- 25.4016 MHz for 12 × CD-ROM data rate (8 × clock frequency +50%)
- 33.8688 MHz for 16 × CD-ROM data rate, including DVD (8 × clock frequency +100%)

These frequencies are derived from the currently popular decoder IC frequencies. It is also possible to drive the clock circuit with a TTL compatible external clock signal. The clock buffer output (CLKO) can supply the system clock or half the system clock (also switchable under software control via the serial bus) to be used as clock generator for other ICs. The oscillator circuit is optimized for low power dissipation, thus for applications beyond 8× the clock signal must be supplied external at pin XTALI.

Reset

Reset is controlled by means of the RSTI pin (active HIGH). This circuit ensures correct initialization of the digital circuit and the output stages. The minimum reset time is 250 ns. The inverse synchronized reset signal is available on the output pin $\overline{\text{RSTO}}$. This signal can be used to reset the decoder and disable the SZA1010 (digital output stages) during a reset.

Laser drive on

The $\overline{\text{LDO}}$ pin is used to switch the laser drive off and on. It is an open drain output. When the laser is on, the output has a high impedance. This pin is automatically driven when the focus control loop is switched on.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage	0	6.5	V
V_{DDA}	analog supply voltage	0	6.5	V
ΔV_{SS}	ground supply voltage difference between V_{SSA} and V_{SSD}	–5	+5	mV
P_{diss}	power dissipation	–	200	mW
T_{stg}	storage temperature	55	150	°C
T_{amb}	operating ambient temperature	–40	+85	°C
V_{esd}	electrostatic handling	–2000	+2000	V

HANDLING

Electrostatic handling in accordance with *"UZW-BO/FQ-0604"*.

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611E"*.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	80	K/W

CHARACTERISTICS

V_{DDD} = 5 V; V_{DDA} = 5 V; V_{SSD} = V_{SSA} = 0 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDD}	digital supply voltage		4.5	–	5.5	V
V_{DDA}	analog supply voltage		4.5	–	5.5	V
I_{DDD}	digital supply current		–	17	–	mA
I_{DDA}	analog supply current		–	–	9.0	mA
$I_{DD(q)}$	digital quiescent supply current		–	–	10	µA
P_{tot}	total power dissipation		–	115	–	mW
T_{amb}	operating ambient temperature		–40	–	+85	°C
Analog part						
DSICS ANALOG FRONT-END SPECIFICATION						
V_{DDA}	analog supply voltage		4.5	–	5.5	V
I_{DDA}	analog supply current		–	5	–	mA
I_{ref}	reference input current (XTLR)		1.935	–	6	µA
R_{ext}	external resistor		200	–	620	kΩ
V_i	voltage on current input (XTLR)		–	1.2	–	V
I_I	input current					
	for pins D1 to D4	note 1	3.871	–	12	µA
	for pinsS1 and S2	note 1	1.935	–	6	µA
C_{ext}	external capacitors D1 to D4, S1, S2		100	220	400	pF
V_i	voltage on current inputs D1 to D4, S1, S2		–	Virtual V_{refL}	–	V
V_{refL}	LOW level reference voltage		0	0	0	V
V_{refH}	HIGH level reference voltage		0.5	–	2.5	V
(THD+N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB; note 2	–	–50	–45	dB
S/N	signal-to-noise ratio		–	55	–	dB
PSRR	power supply ripple rejection	at V_{DDA}; note 3	–	45	–	dB
G_{tol}	gain tolerance	note 4	±13	–	±18	%
ΔG	variance of gain between channels		–	–	2	%
α_{cs}	channel separation		–	60	–	dB
Digital part						
DIGITAL INPUTS, WITH INTERNAL PULL-DOWN RESISTOR: TEST1, TEST2 AND DEFI						
V_{IL}	LOW level input voltage	T_{amb} = –40 to +85 °C	–	–	$0.3V_{DDD}$	V
V_{IH}	HIGH level input voltage	T_{amb} = –40 to +85 °C	$0.7V_{DDD}$	–	–	V
R_{pd}	internal pull-down resistor to V_{SSD}		27	–	80	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DIGITAL INPUTS, WITH INTERNAL PULL-DOWN RESISTOR AND TTL COMPATIBLE: FTC						
V_{IL}	LOW level input voltage	T_{amb} = –40 to +85 °C	–	–	0.8	V
V_{IH}	HIGH level input voltage	T_{amb} = –40 to +85 °C	2.0	–	–	V
R_{pd}	internal pull-down resistor to V_{SSD}		27	–	80	kΩ
DIGITAL INPUTS: SILD, SICL AND $\overline{\text{ENIIC}}$						
V_{IL}	LOW level input voltage	T_{amb} = –40 to +85 °C	–	–	$0.3V_{DDD}$	V
V_{IH}	HIGH level input voltage	T_{amb} = –40 to +85 °C	$0.7V_{DDD}$	–	–	V
I_{LI}	input leakage current		–	–	1	µA
DIGITAL INPUTS WITH INTERNAL PULL-DOWN RESISTOR, HYSTERESIS AND TTL COMPATIBLE: RSTI						
V_{IL}	LOW level input voltage	T_{amb} = –40 to +85 °C	–	–	0.6	V
V_{IH}	HIGH level input voltage	T_{amb} = –40 to +85 °C	2.4	–	–	V
R_{pd}	internal pull-down resistor to V_{SSD}		27	–	80	kΩ
DIGITAL OUTPUTS: $\overline{\text{LDO}}$ (OPEN DRAIN)						
I_{OL}	LOW level output current	V_o = 0.4 V	–	4	–	mA
I_{OH}	HIGH level output current	open drain	–	0	–	mA
t_r	rise time		–	–	–	ns
t_f	fall time	note 5	–	27	–	ns
DIGITAL OUTPUTS: OTD, $\overline{\text{INTREQ}}$, RAB, CL, $\overline{\text{RSTO}}$, CLKO AND DEFO						
I_{OL}	LOW level output current	V_o = 0.4 V	–	4	–	mA
I_{OH}	HIGH level output current	$V_o = V_{DDD} – 0.4$ V	–	4	–	mA
t_r	rise time	note 5	–	23	–	ns
t_f	fall time	note 5	–	27	–	ns
DIGITAL OUTPUTS; 3-STATE: RA, FO, SL, RP, TL AND FOK						
I_{OL}	LOW level output current	V_o = 0.4 V	–	4	–	mA
I_{OH}	HIGH level output current	$V_o = V_{DDD} – 0.4$ V	–	4	–	mA
$\lvert I_{OZ} \rvert$	3-state leakage current	T_{amb} = –40 to +85 °C	–	–	5	µA
I	current	V_o = 0 to V_{DDD}	–	–	–	A
t_r	rise time	note 5	–	24	–	ns
t_f	fall time	note 5	–	28	–	ns
DIGITAL BIDIRECTIONAL: SIDA AND DA						
V_{IL}	LOW level input voltage	T_{amb} = –40 to +85 °C	–	–	0.8	V
V_{IH}	HIGH level input voltage	T_{amb} = –40 to +85 °C	2.0	–	–	V
I_{OL}	LOW level output current	V_o = 0.4 V	4	–	–	mA
I_{OH}	HIGH level output current	$V_o = V_{DDD} – 0.4$ V	4	–	–	mA
$\lvert I_{OZ} \rvert$	3-state leakage current	T_{amb} = –40 to +85 °C	–	–	5	µA
I	current	V_o = 0 to V_{DDD}	–	–	–	A
t_r	rise time	note 5	–	19	–	ns
t_f	fall time	note 5	–	33	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator						
f_{osc}	oscillator frequency	note 6	8	–	33.9	MHz
C_{in}	input capacitance		–	8.5	10	pF
C_{fb}	feedback capacitance		–	3	3.7	pF
C_{out}	output capacitance		–	2	3	pF
Slave clock mode						
V_{IL}	LOW level input voltage		–	–	0.5	V
V_{IH}	HIGH level input voltage		2.0	–	–	V
t_H	input HIGH time	relative to clock period	45	–	55	%

Notes

1. f_{sys} = 8.4672 MHz; V_{refL} = 0 V.
   a) For A/D converters D1 to D4: $I_{I(max)} = \frac{2.4}{R_{ext}} = \frac{2.4}{200\ k\Omega} = 12\ \mu A$
   b) For A/D converters S1 and S2: $I_{I(max)} = \frac{1.2}{R_{ext}} = \frac{\overline{1.2}}{200\ k\Omega} = 6\ \mu A$
2. Measuring bandwidth: 200 Hz to 20 kHz; f_{inADC} = 1 kHz.
3. f_{ripple} = 1 kHz; V_{ripple} = 0.5 V (p-p).
4. Gain tolerance is determined by the accuracy of external resistor R_{ext}.
5. At 10 to 90% levels with C_L = 50 pF; V_{DD} = 4.5 V; T_j = 85 °C.
6. The oscillator frequency specification is depending on the application speed (see Table 2).

Table 2 Oscillator frequencies; note 1

APPLICATION SPEED	TYPICAL OSCILLATOR FREQUENCY (MHz)	REMARK
8×	16.9344	
10×	22.0147	
12×	25.4016	
16×	33.8688	including DVD application

Note

1. Note that the internal clock frequency is recommended as half of the oscillator frequency and that the digital power consumption scales with this clock frequency. For applications beyond 8× the clock signal must be supplied externally via pin XTALI.

APPLICATION INFORMATION

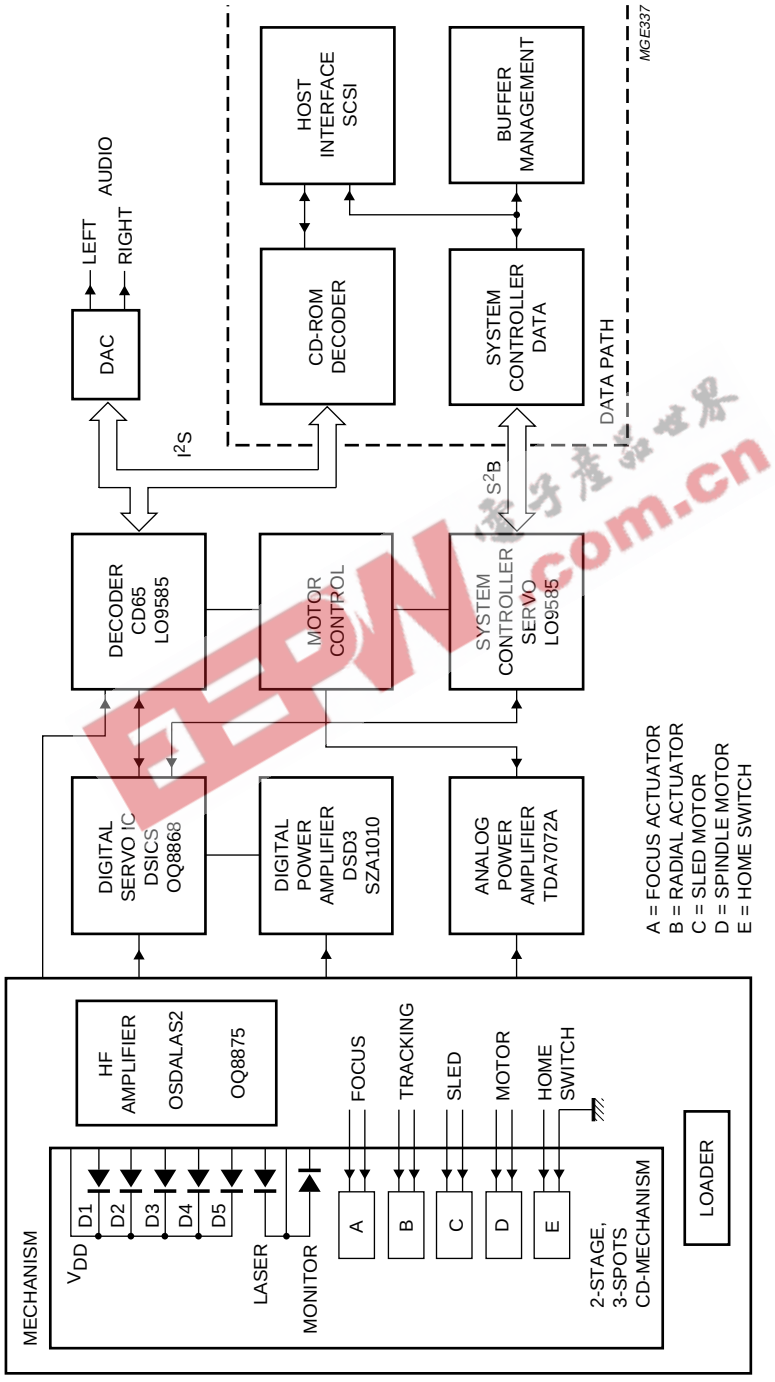
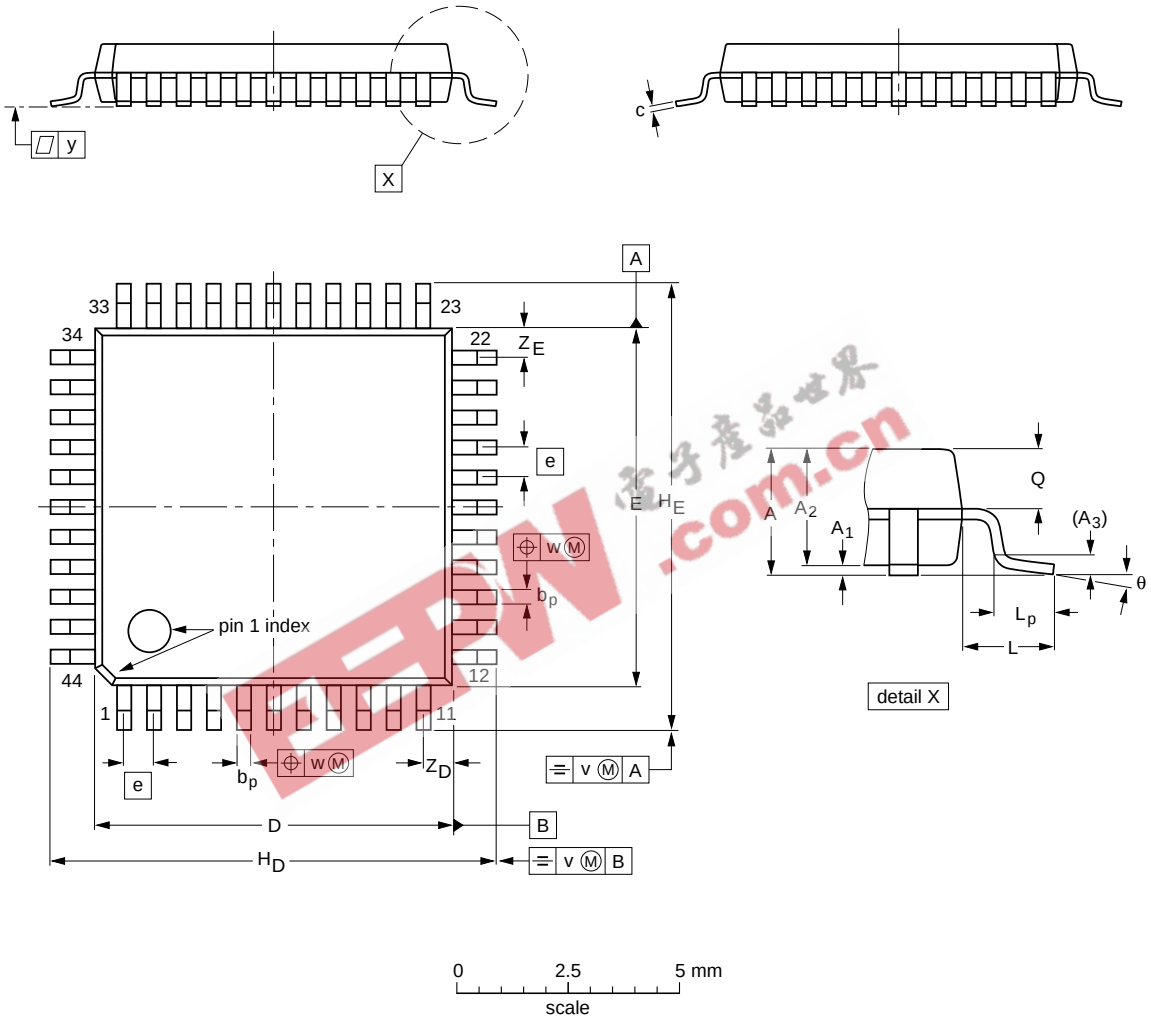


Fig.4 Application diagram.

PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.85 0.75	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~92-11-17~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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