Optoelectronics Division
TRW Electronic Components Group

Product Bulletin 5254
January 1985

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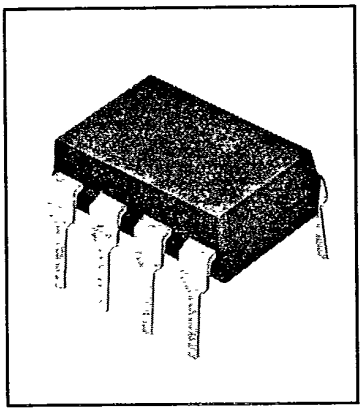
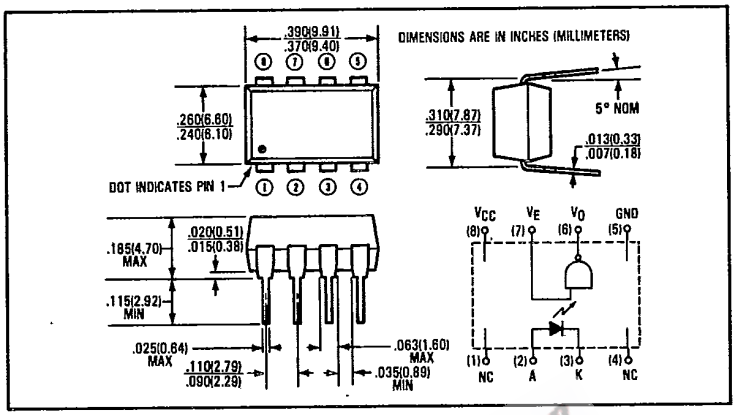
T-41-87

Optically Coupled Logic Gate
Types 6N137, OPI8137





Features
- LSTTL/TTL compatible
- Extremely high speed
- Low input current requirement
- High common mode rejection
- Guaranteed over temperature
- 3000 VDC isolation
- U.L. Recognized, File No. E58730

Description
The 6N137 and OPI8137 optocoupler combine a GaAsP photon emitting diode with a unique integrated detector. Photons are collected in the detector by a photodiode and amplified by a high gain linear amplifier that drives a Schottky clamped open collector output transistor. The circuit is temperature, current and voltage compensated.

The unique design produces maximum DC and AC circuit isolation between input and output while providing LSTTL/TTL circuit compatibility. Isolator parameters are guaranteed from 0°C to 70°C, so that a minimum input current of 5 mA will sink an eight gate fan-out (13 mA) at the output with 5 volt V_{CC} applied to the detector. Isolation and coupling are achieved with typical propagation delays of 45 ns for the 6N137 and 90 ns for the OPI8137. The enable input provides gating of the detector with input sinking and sourcing requirements compatible with LSTTL/TTL interfacing and a typical propagation delay of 25 ns.

Absolute Maximum Ratings* (No derating required up to 70°C)

Storage Temperature	−55°C to +125°C
Operating Temperature	0°C to +70°C
Lead Solder Temperature (1/16 inch [1.6 mm] from case for 10 seconds)	260°C
Peak Forward Input Currrent (≤ 1 msec duration)	40 mA
Average Forward Input Current	20 mA
Reverse Input Voltage	5.0 V
Enable Input Voltage (not to exceed V_{CC} by more than 500 mV)	5.5 V
Supply Voltage – V_{CC} (1 minute maximum)	7.0 V
Output Current – I_O	50 mA
Output Collector Power Dissipation	85 mW
Output Voltage – V_O	7.0 V

* JEDEC Registered Data

Applications
The device is designed for use in high speed digital interfacing applications where common mode signals must be rejected. Elimination of ground loops can be accomplished in system interfaces such as between a computer and a peripheral memory, printer, controller, etc.

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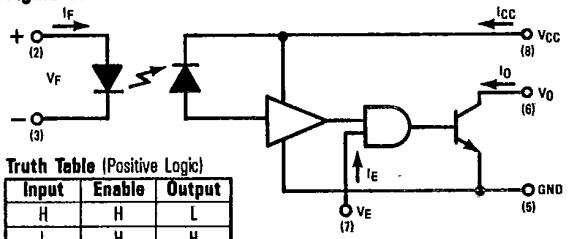
Figure 1. Schematic



Truth Table (Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H

Note:
A .01 to 0.1 μF bypass capacitor must be connected between pins 8 and 5.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
I_{FL}	Input Current, Low Level Each Channel	0	250	μA
I_{FH}	Input Current, High Level Each Channel	6.3**	15.0	mA
V_{EH}	High Level Enable Voltage	2.0	V_{CC}	V
V_{EL}	Low Level Enable Voltage (Output High)	0	0.80	V
V_{CC}	Supply Voltage, Output	4.5	5.5	V
N	Fan Out (TTL Load)		8	
T_A	Operating Temperature	0	70	°C

Electrical Characteristics Over recommended temperature (T_A = 0°C to 70°C), unless otherwise noted

Symbol	Parameter	Min.	Typ.***	Max.	Units	Test Conditions	Figure
I_{OH}*	High Level Output Current		2.0	250	μA	V_{CC} = 5.5 V, V_O = 5.5 V, I_F = 250 μA, V_E = 2.0 V	6
V_{OL}*	Low Level Output Voltage		0.40	0.60	V	V_{CC} = 5.5 V, I_F = 5.0 mA, V_{EH} = 2.0 V, I_{OL} (Sinking) = 13.0 mA	2, 3
I_{EH}	High Level Enable Current		−0.80		mA	V_{CC} = 5.5 V, V_E = 2.0 V	
I_{EL}*	Low Level Enable Current		−1.20	−2.0	mA	V_{CC} = 5.5 V, V_E = 0.50 V	
I_{CCH}*	High Level Supply Current		7.0	15.0	mA	V_{CC} = 5.5 V, I_F = 0, V_E = 0.50 V	
I_{CCL}*	Low Level Supply Current		13.0	18.0	mA	V_{CC} = 5.5 V, I_F = 10.0 mA, V_E = 0.50 V	
I_{IO}*	Input-Output Insulation Leakage Current			1.00	μA	Relative Humidity = 45%, T_A = 25°C, t = 5.0 sec, V_{IO} = 3000 VDC	
R_{IO}	Input-Output Resistance		10^{12}		Ω	V_{IO} = 500 V, T_A = 25°C	
C_{IO}	Input-Output Capacitance		0.60		pF	f = 1.00 MHz, T_A = 25°C	
V_F*	Input Forward Voltage		1.50	1.75	V	I_F = 10.0 mA, T_A = 25°C	5
BV_R*	Input Reverse Breakdown Voltage	5.0			V	I_R = 10.0 μA, T_A = 25°C	
C_{IN}	Input Capacitance		60		pF	V_F = 0, f = 1.00 MHz	
CTR	Current Transfer Ratio		700		%	I_F = 5.0 mA, R_L = 100Ω	4

Switching Specifications (T_A = 25°C) V_{CC} = 5 V

t_{PLH}	Propagation Delay Time to High Output Level	6N137 *		45	75	ns	R_L = 350Ω, C_L = 15.0 pF, I_F = 7.5 mA	7, 8
		OPI8137		90	150	ns		
t_{PHL}	Propagation Delay Time to Low Output Level	6N137 *		45	75	ns	R_L = 350Ω, C_L = 15.0 pF, I_F = 7.5 mA	7, 8
		OPI8137		90	150	ns		
t_r, t_f	Output Rise-Fall Time (10-90%)			20, 30		ns	R_L = 350Ω, C_L = 15.0 pF, I_F = 7.5 mA	
t_{ELH}	Propagation Delay Time of Enable from V_{EH} to V_{EL}			40		ns	R_L = 350Ω, C_L = 15.0 pF, I_F = 7.5 mA, V_{EH} = 3.0 V, V_{EL} = 0.50 V	10
t_{EHL}	Propagation Delay Time of Enable from V_{EL} to V_{EH}			25		ns	R_L = 350Ω, C_L = 15.0 pF, I_F = 7.5 mA, V_{EH} = 3.0 V, V_{EL} = 0.50 V	10
CM_H	Common Mode Transient Immunity at Logic High Output			50		V/μs	V_{CM} = 10.0 V, R_L = 350Ω, $V_{O(min)}$ = 2.0 V, I_F = 0 mA (See Note 1)	12
CM_L	Common Mode Transient Immunity at Logic Low Output			−150		V/μs	V_{CM} = 10.0 V, R_L = 350Ω, $V_{O(max)}$ = 0.80 V, I_F = 5.0 mA (See Note 2)	12

* JEDEC Registered Data. ** Permits 20% CTR degradation. *** All typicals at T_A = 25°C and V_{CC} = 5.0 V, unless otherwise noted.

Notes:
1. CM_H is the maximum allowable dv/dt on the leading edge of a common mode pulse to assure that the output will not switch from high to low.
2. CM_L is the maximum negative dv/dt allowable on the trailing edge of a common mode pulse to assure that the output will not switch from low to high.

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Operating Procedures and Definitions

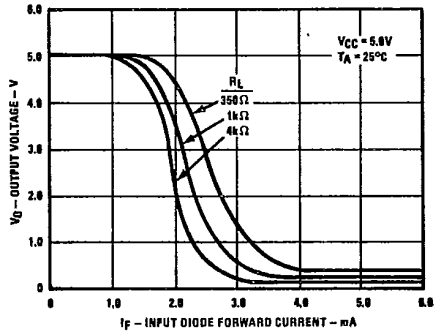
Logic Convention. The 6N137 is defined in terms of positive logic.

Bypassing. A ceramic capacitor (.01 to 0.1 μF) should be connected from pin 8 to pin 5 (Figure 9) to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching properties. The total lead length between capacitor and coupler should not exceed 20 mm.

Polarities. All voltages are referenced to network ground (pin 5). Current flowing toward a terminal is considered positive.

Enable Input. No external pull-up required for a logic (1), i.e., can be open circuit.

Figure 2. Input-Output Characteristics



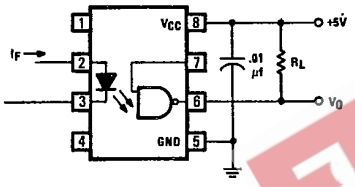


Figure 3. Output Voltage, V_{OL} vs Temperature and Fan-Out

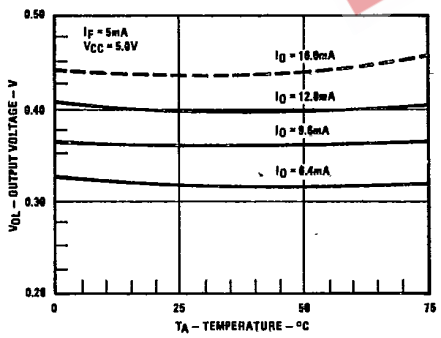
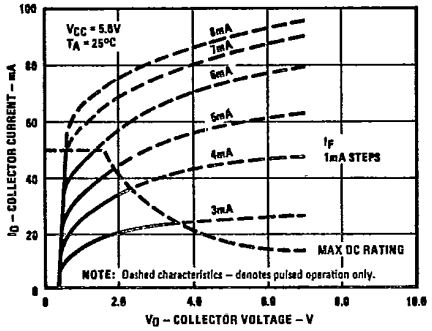


Figure 4. Optocoupler Collector Characteristics



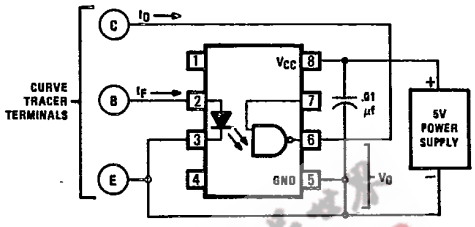


Figure 5. Input Diode Forward Characteristic

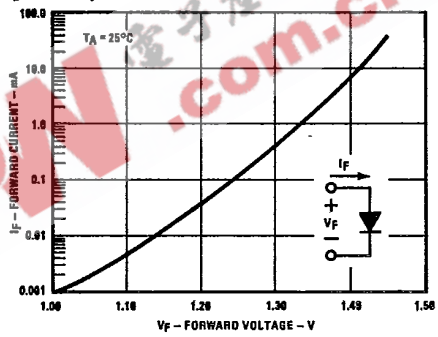


Figure 6. Output Current, I_{OH} vs Temperature (I_F=250 μA)

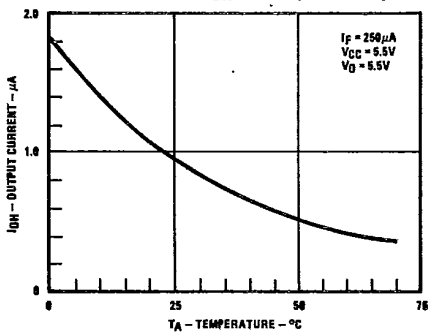


Figure 7. Test Circuit for T_{PHL} and T_{PLH} (6N137 Only)

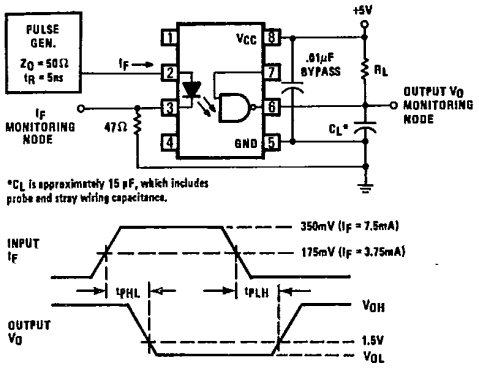


Figure 8. Propagation Delay, t_{PHL} and t_{PLH} vs Pulse Input Current, I_{FH}

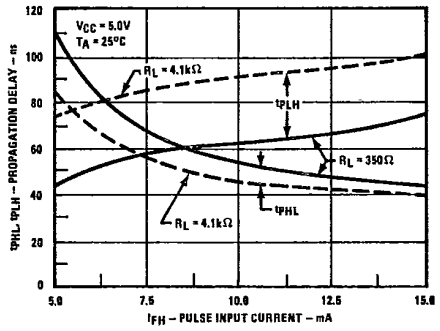


Figure 9. Recommended Printed Circuit Board Layout

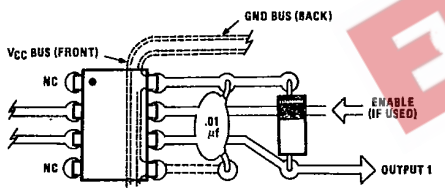


Figure 10. Test Circuit for T_{ELH} and T_{EHL}

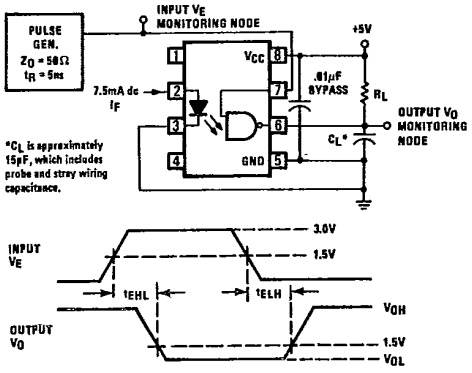


Figure 11. Response Delay Between TTL Gates

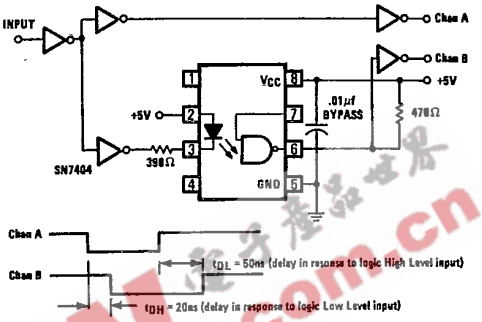
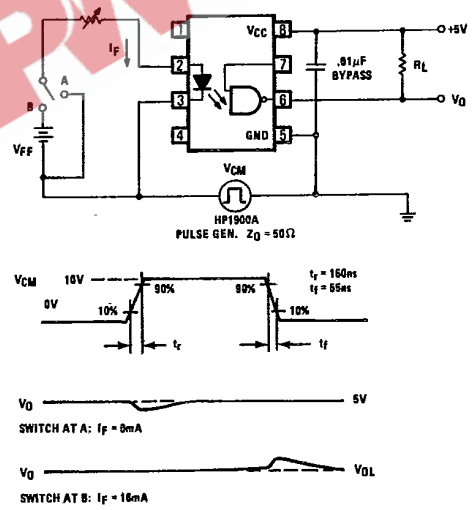


Figure 12. Test Circuit for Transient Immunity and Typical Waveforms



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