

OPA177

Precision OPERATIONAL AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 25 μ V max
- LOW DRIFT: 0.3 μ V/ $^{\circ}$ C
- HIGH OPEN-LOOP GAIN: 130dB min
- LOW QUIESCENT CURRENT: 1.5mA typ
- REPLACES INDUSTRY-STANDARD OP AMPS: OP-07, OP-77, OP-177, AD707, ETC.

APPLICATIONS

- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER

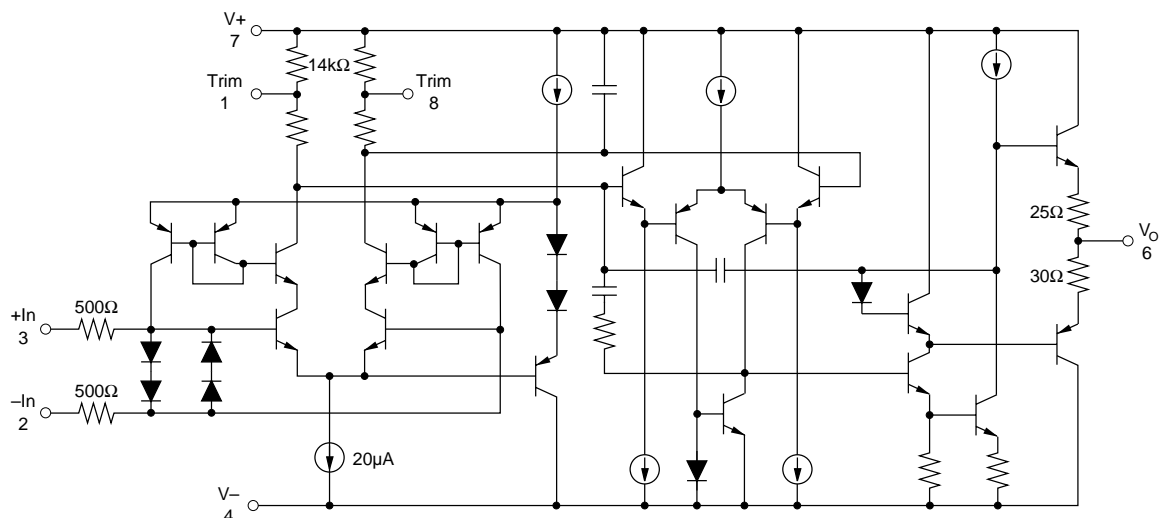
DESCRIPTION

The OPA177 precision bipolar op amp feature very low offset voltage and drift. Laser-trimmed offset, drift and input bias current virtually eliminate the need for costly external trimming. The high performance and low cost make them ideally suited to a wide range of precision instrumentation.

The low quiescent current of the OPA177 dramatically reduce warm-up drift and errors due to thermo-

electric effects in input interconnections. It provides an effective alternative to chopper-stabilized amplifiers. The low noise of the OPA177 maintains accuracy.

OPA177 performance gradeouts are available. Packaging options include 8-pin plastic DIP and SO-8 surface-mount packages.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: <http://www.burr-brown.com/> • FAXline: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

OPA177 SPECIFICATIONS

At $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	CONDITION	OPA177F			OPA177G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage Long-Term Input Offset ⁽¹⁾ Voltage Stability Offset Adjustment Range Power Supply Rejection Ratio	$R_P = 20k\Omega$ $V_S = \pm 3V$ to $\pm 18V$		10 0.3	25		20 0.4	60	μV $\mu V/Mo$ mV dB
INPUT BIAS CURRENT Input Offset Current Input Bias Current			0.3 0.5	1.5 ± 2		* *	2.8 ± 2.8	nA nA
NOISE Input Noise Voltage Input Noise Current	1Hz to 100Hz ⁽²⁾ 1Hz to 100Hz		85 4.5	150		* *	*	nVrms pArms
INPUT IMPEDANCE Input Resistance	Differential Mode ⁽³⁾ Common-Mode	26	45 200		18.5	* *		M Ω G Ω
INPUT VOLTAGE RANGE Common-Mode Input Range ⁽⁴⁾ Common-Mode Rejection	$V_{CM} = \pm 13V$	± 13 130	± 14 140		* 115	* *		V dB
OPEN-LOOP GAIN Large Signal Voltage Gain	$R_L \geq 2k\Omega$ $V_O = \pm 10V$ ⁽⁵⁾	5110	12,000		2000	6000		V/mV
OUTPUT Output Voltage Swing Open-Loop Output Resistance	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	± 13.5 ± 12.5 ± 12	± 14 ± 13 ± 12.5 60		* * *	* * *		V V V Ω
FREQUENCY RESPONSE Slew Rate Closed-Loop Bandwidth	$R_L \geq 2k\Omega$ $G = +1$	0.1 0.4	0.3 0.6		* *	* *		V/ μs MHz
POWER SUPPLY Power Consumption Supply Current	$V_S = \pm 15V$, No Load $V_S = \pm 3V$, No Load $V_S = \pm 15V$, No Load		40 3.5 1.3	60 4.5 2		* * *	* * *	mW mW mA

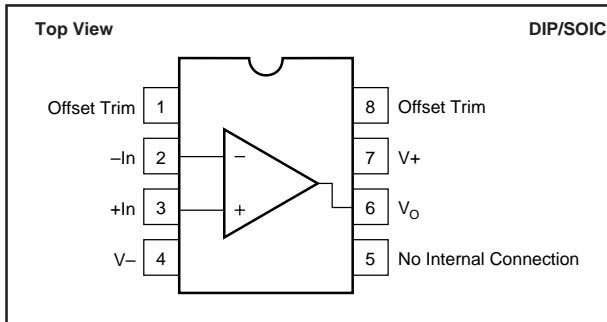
At $V_S = \pm 15V$, $-40^\circ C \leq T_A \leq +85^\circ C$, unless otherwise noted.

OFFSET VOLTAGE Input Offset Voltage Average Input Offset Voltage Drift Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$		15 0.1	40 0.3		20 0.7	100 1.2	μV $\mu V/^\circ C$ dB
INPUT BIAS CURRENT Input Offset Current Average Input Offset Current Drift ⁽⁶⁾ Input Bias Current Average Input Bias Current Drift ⁽⁶⁾			0.5 1.5	2.2 40		* *	4.5 85	nA pA/ $^\circ C$ nA pA/ $^\circ C$
INPUT VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection	$V_{CM} = \pm 13V$	± 13 120	± 13.5 140		* 110	* *		V dB
OPEN-LOOP GAIN Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	2000	6000		1000	4000		V/mV
OUTPUT Output Voltage Swing	$R_L \geq 2k\Omega$	± 12	± 13		* *	* *		V
POWER SUPPLY Power Consumption Supply Current	$V_S = \pm 15V$, No Load $V_S = \pm 15V$, No Load		60 2	75 25		* *	* *	mW mA

* Same as specification for product to left.

NOTES: (1) Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically less than $2\mu V$. (2) Sample tested. (3) Guaranteed by design. (4) Guaranteed by CMRR test condition. (5) To insure high open-loop gain throughout the $\pm 10V$ output range, A_{OL} is tested at $-10V \leq V_O \leq 0V$, $0V \leq V_O \leq +10V$, and $-10V \leq V_O \leq +10V$. (6) Guaranteed by end-point limits.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±22V
Differential Input Voltage	±30V
Input Voltage	±V _S
Output Short Circuit	Continuous
Operating Temperature:	
Plastic DIP (P), SO-8 (S)	-40°C to +85°C
θ _{JA} (PDIP)	100°C/W
θ _{JA} (SOIC)	160°C/W
Storage Temperature:	
Plastic DIP (P), SO-8 (S)	-65°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s) P packages	+300°C
(soldering, 3s) S package	+260°C

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	TEMPERATURE RANGE
OPA177FP	8-Pin Plastic DIP	006	-40°C to +85°C
OPA177GP	8-Pin Plastic DIP	006	-40°C to +85°C
OPA177GS	SO-8 Surface-Mount	182	-40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.



ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. ESD can cause damage ranging from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

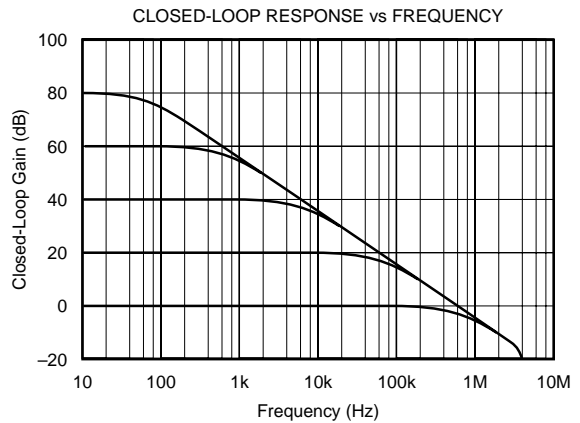
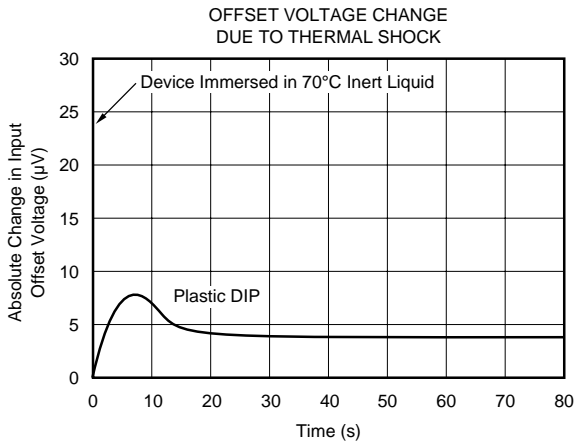
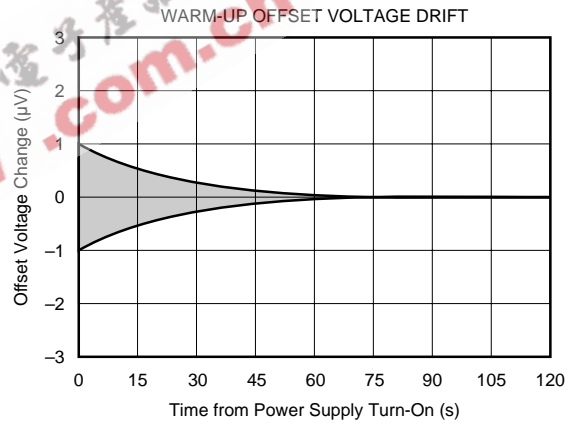
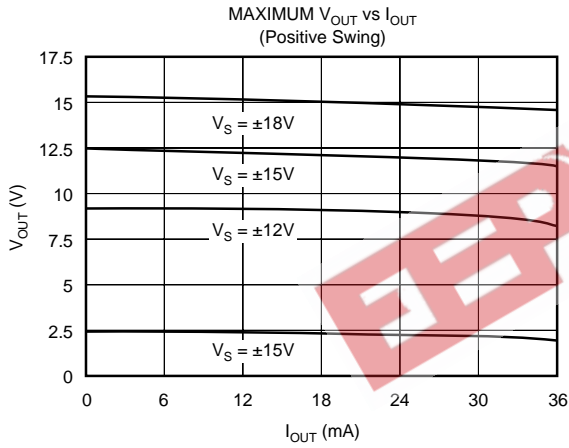
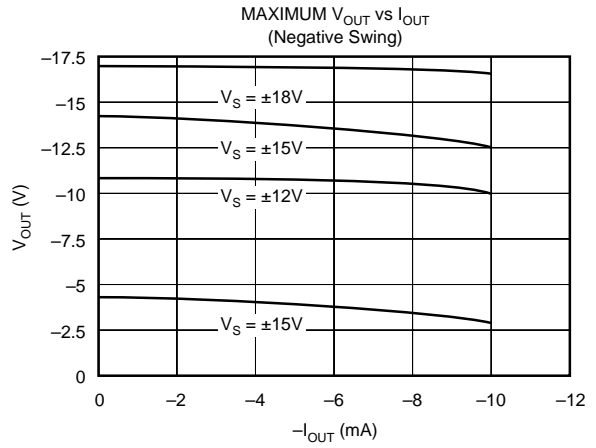
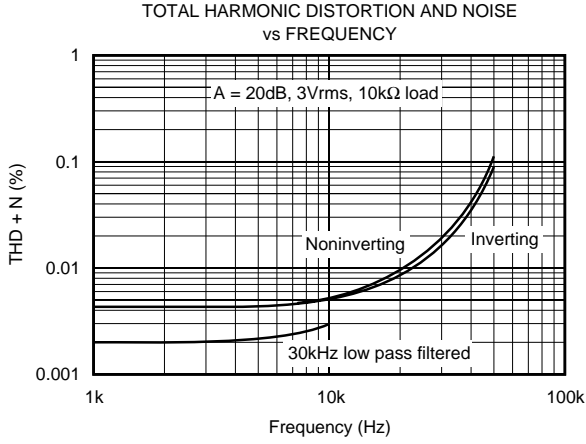
Burr-Brown's standard ESD test method consists of five 1000V positive and negative discharges (100pF in series with 1.5kΩ) applied to each pin.

Failure to observe proper handling procedures could result in small changes to the OPA177's input bias current.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

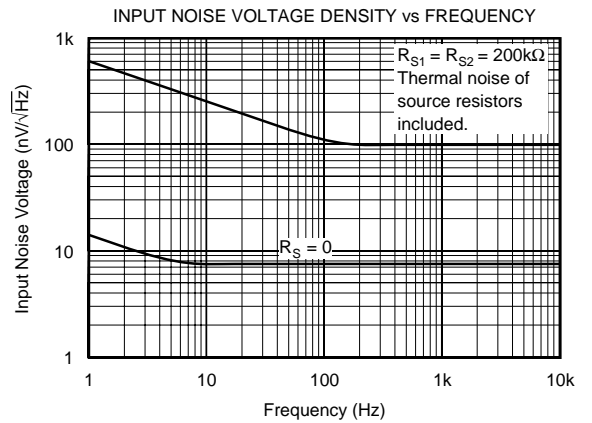
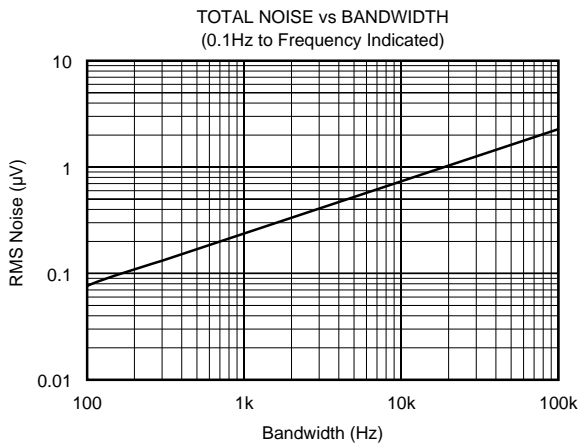
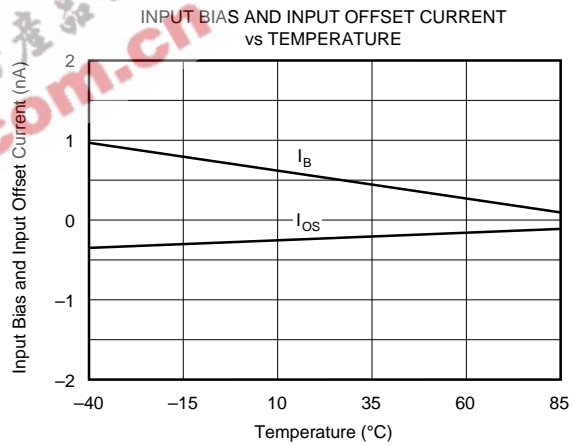
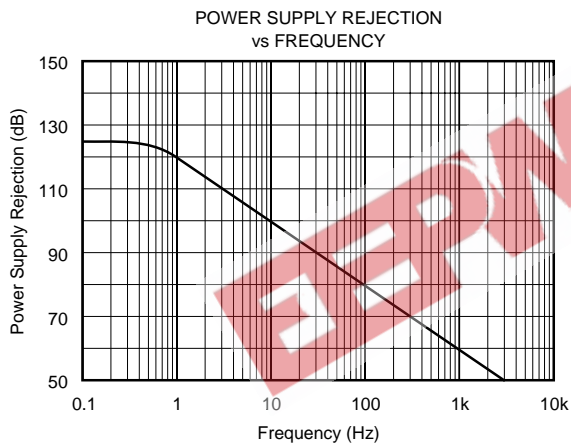
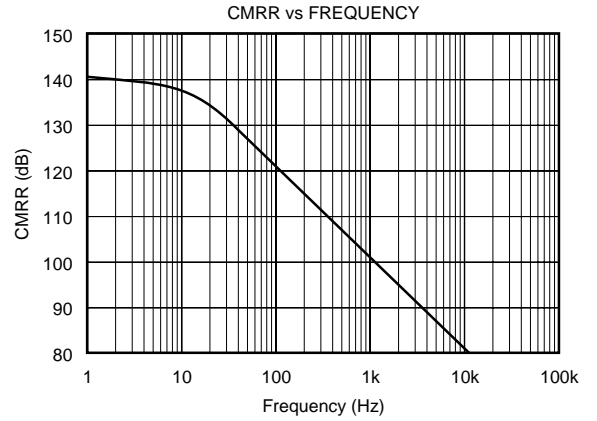
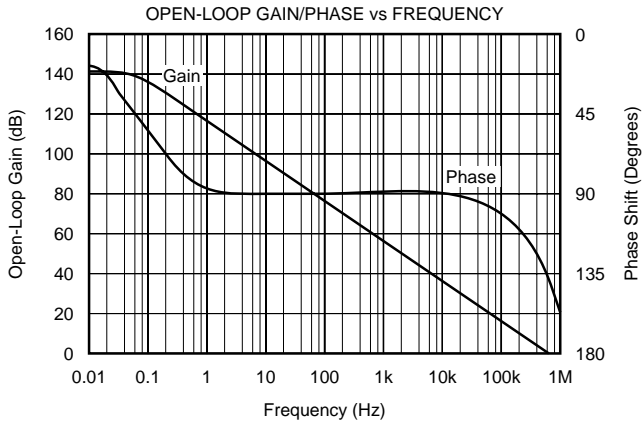
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



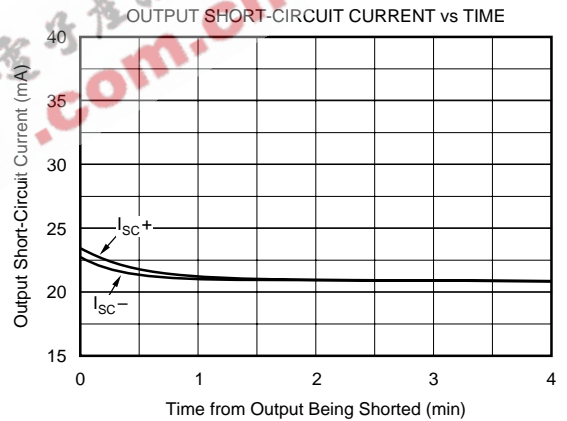
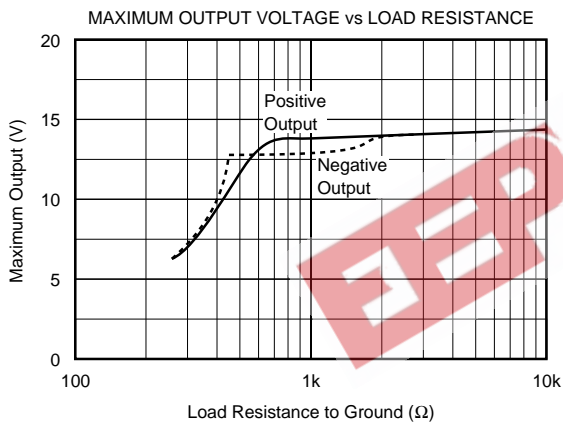
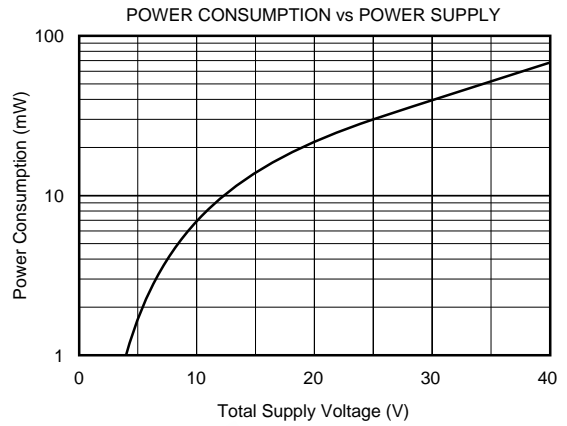
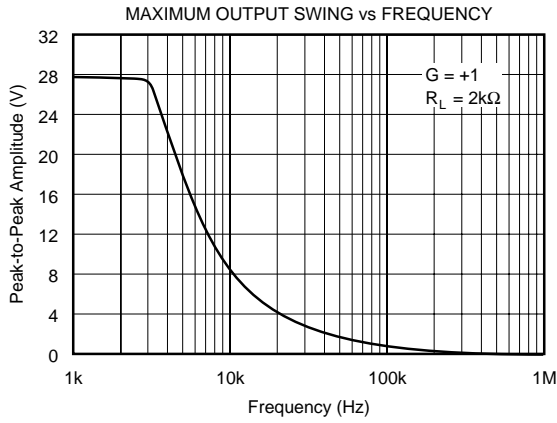
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



APPLICATIONS INFORMATION

The OPA177 is unity-gain stable, making it easy to use and free from oscillations in the widest range of circuitry. Applications with noisy or high impedance power supply lines may require decoupling capacitors close to the device pins. In most cases 0.1 μ F ceramic capacitors are adequate.

The OPA177 has very low offset voltage and drift. To achieve highest performance, circuit layout and mechanical conditions must be optimized. Offset voltage and drift can be degraded by small thermoelectric potentials at the op amp inputs. Connections of dissimilar metals will generate thermal potential which can mask the ultimate performance of the OPA177. These thermal potentials can be made to cancel by assuring that they are equal in both input terminals.

1. Keep connections made to the two input terminals close together.
2. Locate heat sources as far as possible from the critical input circuitry.
3. Shield the op amp and input circuitry from air currents such as cooling fans.

OFFSET VOLTAGE ADJUSTMENT

The OPA177 has been laser-trimmed for low offset voltage and drift so most circuits will not require external adjustment. Figure 1 shows the optional connection of an external potentiometer to adjust offset voltage. This adjustment should not be used to compensate for offsets created elsewhere in a system since this can introduce excessive temperature drift.

INPUT PROTECTION

The inputs of the OPA177 are protected with 500 Ω series input resistors and diode clamps as shown in the simplified circuit diagram. The inputs can withstand ± 30 V differential inputs without damage. The protection diodes will, of course, conduct current when the inputs are overdriven. This may disturb the slewing behavior of unity-gain follower applications, but will not damage the op amp.

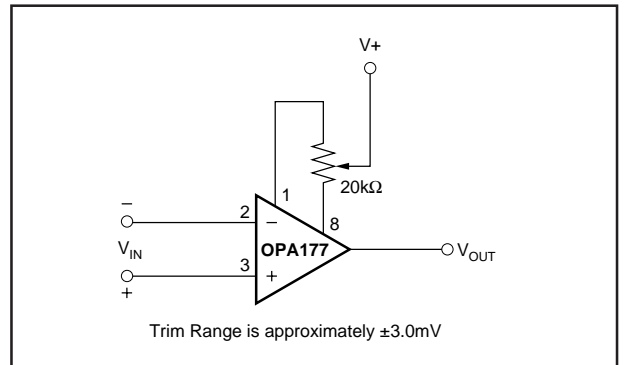


FIGURE 1. Optional Offset Nulling Circuit.

NOISE PERFORMANCE

The noise performance of the OPA177 is optimized for circuit impedances in the range of 2k Ω to 50k Ω . Total noise in an application is a combination of the op amp's input voltage noise and input bias current noise reacting with circuit impedances. For applications with higher source impedance, the OPA627 FET-input op amp will generally provide lower noise. For very low impedance applications, the OPA27 will provide lower noise.

INPUT BIAS CURRENT CANCELLATION

The input stage base current of the OPA177 is internally compensated with an equal and opposite cancellation current. The resulting input bias current is the difference between the input stage base current and the cancellation current. This residual input bias current can be positive or negative.

When the bias current is cancelled in this manner, the input bias current and input offset current are approximately the same magnitude. As a result, it is not necessary to balance the DC resistance seen at the two input terminals (Figure 2). A resistor added to balance the input resistances may actually increase offset and noise.

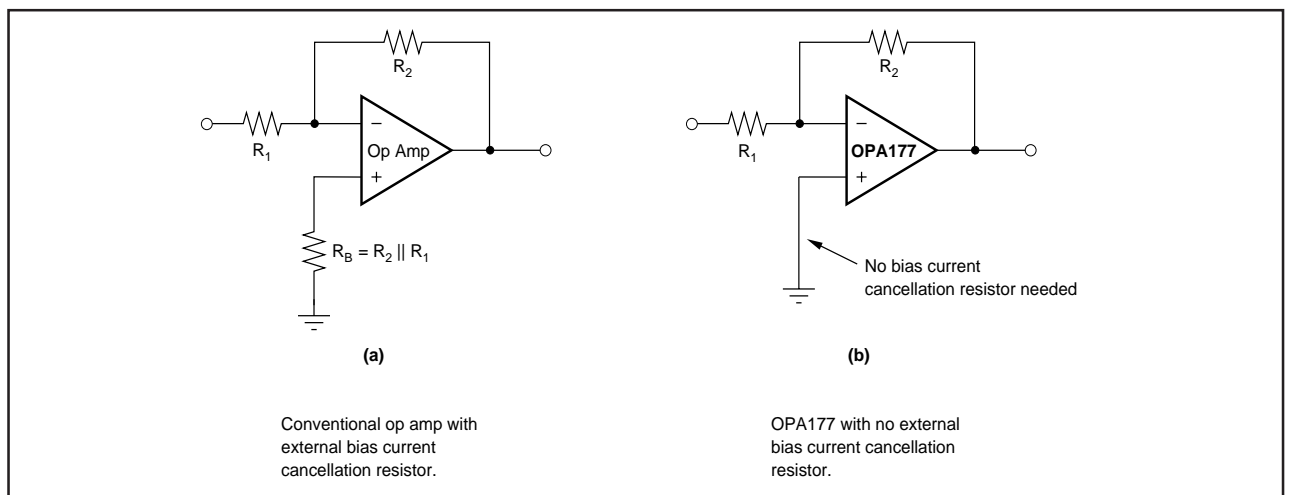


FIGURE 2. Input Bias Current Cancellation.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
OPA177FP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA177FPG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA177GP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA177GPG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA177GS	ACTIVE	SOIC	D	8	100	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA177GS/2K5	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA177GS/2K5E4	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA177GSE4	ACTIVE	SOIC	D	8	100	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265