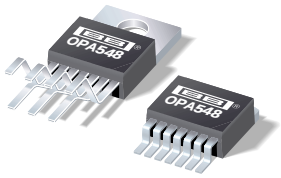
BURR - BROWN®




# OPA548

www.burr-brown.com/databook/OPA548.html

# High-Voltage, High-Current OPERATIONAL AMPLIFIER

## FEATURES

- WIDE SUPPLY RANGE
  Single Supply: +8V to +60V
  Dual Supply: ±4V to ±30V
- HIGH OUTPUT CURRENT:
  3A Continuous
  5A Peak
- WIDE OUTPUT VOLTAGE SWING
- FULLY PROTECTED:
  Thermal Shutdown
  Adjustable Current Limit
- OUTPUT DISABLE CONTROL
- THERMAL SHUTDOWN INDICATOR
- HIGH SLEW RATE: 10V/µs
- LOW QUIESCENT CURRENT
- PACKAGES:
  7-Lead TO-220
  7-Lead DDPAK Surface-Mount

## APPLICATIONS

- VALVE, ACTUATOR DRIVER
- SYNCHRO, SERVO DRIVER
- POWER SUPPLIES
- TEST EQUIPMENT
- TRANSDUCER EXCITATION
- AUDIO AMPLIFIER

## DESCRIPTION

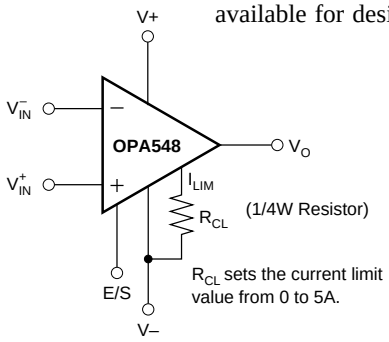
The OPA548 is a low cost, high-voltage/high-current operational amplifier ideal for driving a wide variety of loads. A laser-trimmed monolithic integrated circuit provides excellent low-level signal accuracy and high output voltage and current.

The OPA548 operates from either single or dual supplies for design flexibility. In single supply operation, the input common-mode range extends below ground.

The OPA548 is internally protected against overtemperature conditions and current overloads. In addition, the OPA548 was designed to provide an accurate, user-selected current limit. Unlike other designs which use a "power" resistor in series with the output current path, the OPA548 senses the load indirectly. This allows the current limit to be adjusted from 0 to 5A with a resistor/potentiometer or controlled digitally with a voltage-out or current-out DAC.

The Enable/Status (E/S) pin provides two functions. An input on the pin not only disables the output stage to effectively disconnect the load but also reduces the quiescent current to conserve power. The E/S pin output can be monitored to determine if the OPA548 is in thermal shutdown.

The OPA548 is available in an industry-standard 7-lead staggered TO-220 package and a 7-lead DDPAK surface-mount plastic power package. The copper tab allows easy mounting to a heat sink or circuit board for excellent thermal performance. It is specified for operation over the extended industrial temperature range, –40°C to +85°C. A SPICE macromodel is available for design analysis.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

©1997 Burr-Brown Corporation

Printed in U.S.A. October, 1997

# SPECIFICATIONS

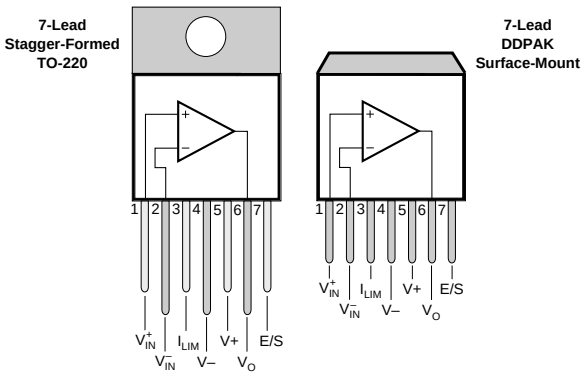
At $T_{CASE}$ = +25°C, $V_S$ = ±30V and E/S pin open, unless otherwise noted.

| PARAMETER | CONDITION | OPA548T, F MIN | OPA548T, F TYP | OPA548T, F MAX | UNITS |
|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0, $I_O$ = 0 | | ±2 | ±10 | mV |
| vs Temperature | $T_A$ = –40°C to +85°C | | ±30 | | µV/°C |
| vs Power Supply | $V_S$ = ±4V to ±30V | | 30 | 100 | µV/V |
| **INPUT BIAS CURRENT**(1) | | | | | |
| Input Bias Current(2) | $V_{CM}$ = 0V | | –100 | –500 | nA |
| vs Temperature | $T_A$ = –40°C to +85°C | | ±0.5 | | nA/°C |
| Input Offset Current | $V_{CM}$ = 0V | | ±5 | ±50 | nA |
| **NOISE** | | | | | |
| Input Voltage Noise Density, f = 1kHz | | | 90 | | nV/√Hz |
| Current Noise Density, f = 1kHz | | | 200 | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | |
| Common-Mode Voltage Range: Positive | Linear Operation | (V+) –3 | (V+) –2.3 | | V |
| Negative | Linear Operation | (V–) –0.1 | (V–) –0.2 | | V |
| Common-Mode Rejection | $V_{CM}$ = (V–) –0.1V to (V+) –3V | 80 | 95 | | dB |
| **INPUT IMPEDANCE** | | | | | |
| Differential | | | $10^7$ \|\| 6 | | Ω \|\| pF |
| Common-Mode | | | $10^9$ \|\| 4 | | Ω \|\| pF |
| **OPEN-LOOP GAIN** | | | | | |
| Open-Loop Voltage Gain | $V_O$ = ±25V, $R_L$ = 1kΩ | 90 | 98 | | dB |
| | $V_O$ = ±25V, $R_L$ = 8Ω | | 90 | | dB |
| **FREQUENCY RESPONSE** | | | | | |
| Gain-Bandwidth Product | $R_L$ = 8Ω | | 1 | | MHz |
| Slew Rate | G = 1, 50Vp-p, $R_L$ = 8Ω | | 10 | | V/µs |
| Full Power Bandwidth | | | See Typical Curve | | kHz |
| Settling Time: ±0.1% | G = –10, 50V Step | | 15 | | µs |
| Total Harmonic Distortion + Noise, f = 1kHz | $R_L$ = 8Ω, G = +3, Power = 10W | | 0.02(3) | | % |
| **OUTPUT** | | | | | |
| Voltage Output, Positive | $I_O$ = 3A | (V+) –4.1 | (V+) –3.7 | | V |
| Negative | $I_O$ = –3A | (V–) +3.7 | (V–) +3.3 | | V |
| Positive | $I_O$ = 0.6A | (V+) –2.4 | (V+) –2.1 | | V |
| Negative | $I_O$ = –0.6A | (V–) +1.3 | (V–) +1.0 | | V |
| Maximum Continuous Current Output: dc | | ±3 | | | A |
| ac | | 3 | | | Arms |
| Leakage Current, Output Disabled, dc | | | See Typical Curve | | |
| Output Current Limit | | | | | |
| Current Limit Range | | | 0 to ±5 | | A |
| Current Limit Equation | | | $I_{LIM}$ = (15000)(4.75)/(13750Ω + $R_{CL}$) | | A |
| Current Limit Tolerance(1) | $R_{CL}$ = 14.8kΩ ($I_{LIM}$ = ±2.5A), $R_L$ = 8Ω | | ±100 | ±250 | mA |
| Capacitive Load Drive | | | See Typical Curve(4) | | |
| **OUTPUT ENABLE /STATUS (E/S) PIN** | | | | | |
| Shutdown Input Mode | | | | | |
| $V_{E/S}$ High (output enabled) | E/S Pin Open or Forced High | (V–) +2.4 | | | V |
| $V_{E/S}$ Low (output disabled) | E/S Pin Forced Low | | | (V–) +0.8 | V |
| $I_{E/S}$ High (output enabled) | E/S Pin High | | –65 | | µA |
| $I_{E/S}$ Low (output disabled) | E/S Pin Low | | –70 | | µA |
| Output Disable Time | | | 1 | | µs |
| Output Enable Time | | | 3 | | µs |
| Thermal Shutdown Status Output | | | | | |
| Normal Operation | Sourcing 20µA | (V–) +2.4 | (V–) +3.5 | | V |
| Thermally Shutdown | Sinking 5µA, $T_J$ > 160°C | | (V–) +0.35 | (V–) +0.8 | V |
| Junction Temperature, Shutdown | | | +160 | | °C |
| Reset from Shutdown | | | +140 | | °C |
| **POWER SUPPLY** | | | | | |
| Specified Voltage | | | ±30 | | V |
| Operating Voltage Range | | ±4 | | ±30 | V |
| Quiescent Current | $I_{LIM}$ Connected to V–, $I_O$ = 0 | | ±17 | ±20 | mA |
| Quiescent Current, Shutdown Mode | $I_{LIM}$ Connected to V–, $I_O$ = 0 | | ±6 | | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specified Range | | –40 | | +85 | °C |
| Operating Range | | –40 | | +125 | °C |
| Storage Range | | –55 | | +125 | °C |
| Thermal Resistance, $\theta_{JC}$ | | | | | |
| 7-Lead DDPAK, 7-Lead TO-220 | f > 50Hz | | 2 | | °C/W |
| 7-Lead DDPAK, 7-Lead TO-220 | dc | | 2.5 | | °C/W |
| Thermal Resistance, $\theta_{JA}$ | | | | | |
| 7-Lead DDPAK, 7-Lead TO-220 | No Heat Sink | | 65 | | °C/W |

NOTES: (1) High-speed test at $T_J$ = +25°C. (2) Positive conventional current flows into the input terminals. (3) See "Total Harmonic Distortion+Noise vs Frequency" in the Typical Performance Curves section for additional power levels. (4) See "Small-Signal Overshoot vs Load Capacitance" in the Typical Performance Curves section.

## CONNECTION DIAGRAMS

**Top Front View**




NOTE: Tabs are electrically connected to V– supply.

## ABSOLUTE MAXIMUM RATINGS(1)

| | |
|---|---|
| Output Current | See SOA Curve |
| Supply Voltage, V+ to V– | 60V |
| Input Voltage | (V–)–0.5V to (V+)+0.5V |
| Input Shutdown Voltage | V+ |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –55°C to +125°C |
| Junction Temperature | 150°C |
| Lead Temperature (soldering 10s)(2) | 300°C |

NOTE: (1) Stresses above these ratings may cause permanent damage. (2) Vapor-phase or IR reflow techniques are recommended for soldering the OPA548F surface mount package. Wave soldering is not recommended due to excessive thermal shock and "shadowing" of nearby devices.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| OPA548T | 7-Lead Stagger-Formed TO-220 | 327 | –40°C to +85°C |
| OPA548F(2) | 7-Lead DDPAK Surface-Mount | 328 | –40°C to +85°C |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Available on Tape and Reel.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

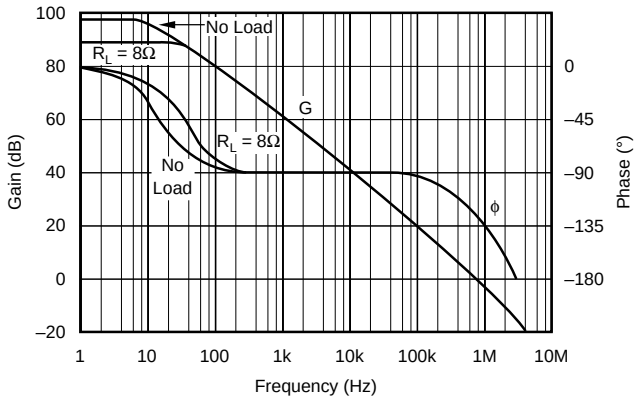
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

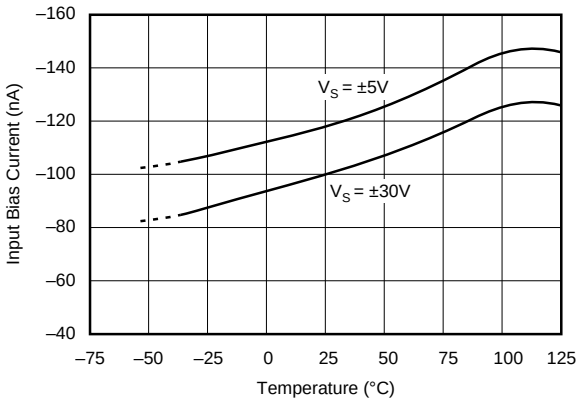
# TYPICAL PERFORMANCE CURVES

At $T_{CASE}$ = +25°C, $V_S$ = ±30V and E/S pin open, unless otherwise noted.

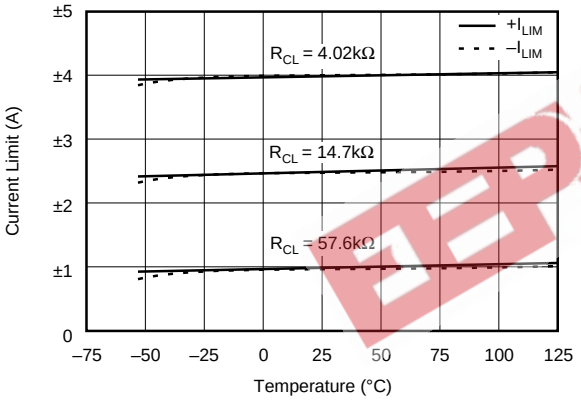
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



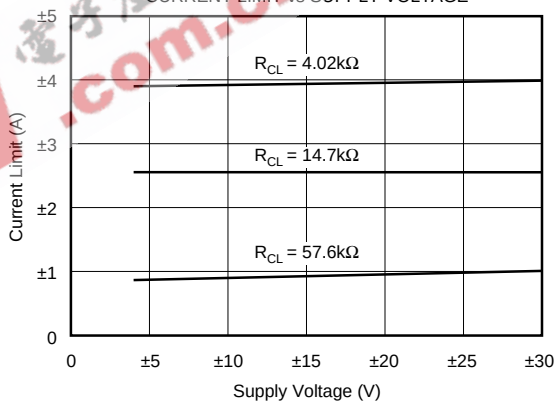

INPUT BIAS CURRENT vs TEMPERATURE



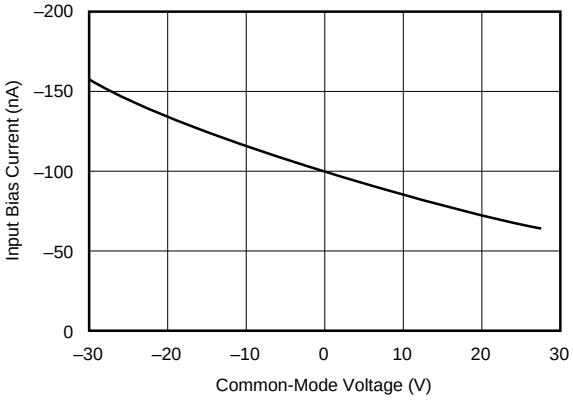

CURRENT LIMIT vs TEMPERATURE



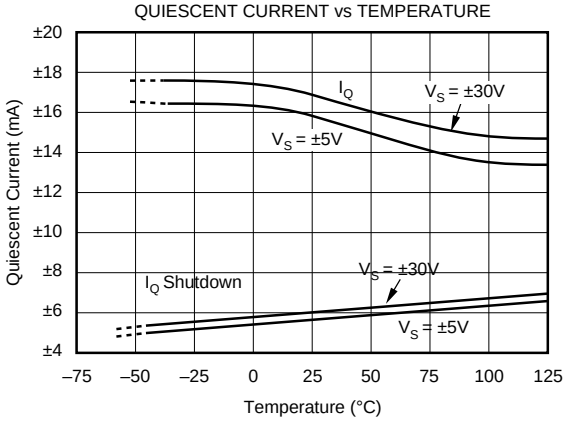

CURRENT LIMIT vs SUPPLY VOLTAGE




INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE




QUIESCENT CURRENT vs TEMPERATURE

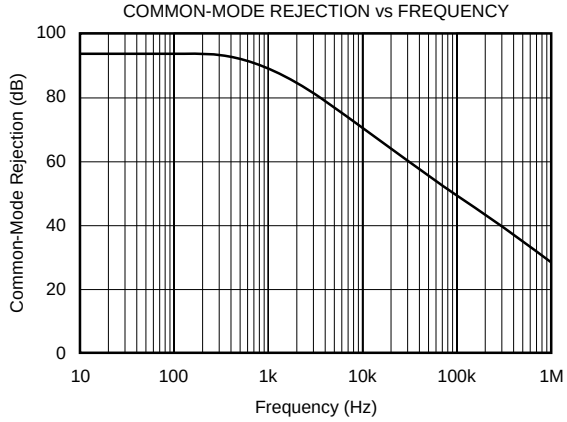



EEPW .com.cn

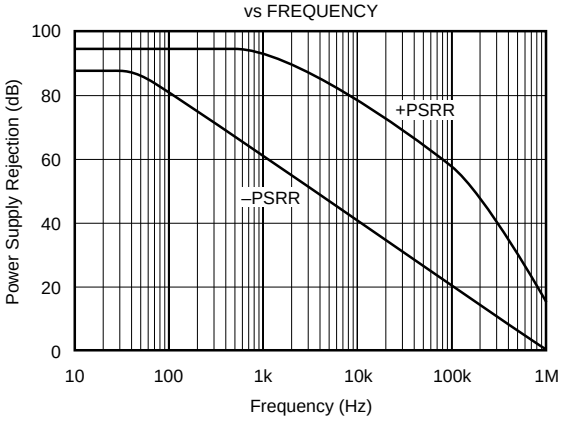
# TYPICAL PERFORMANCE CURVES (CONT)

At $T_{CASE}$ = +25°C, $V_S$ = ±30V and E/S pin open, unless otherwise noted.

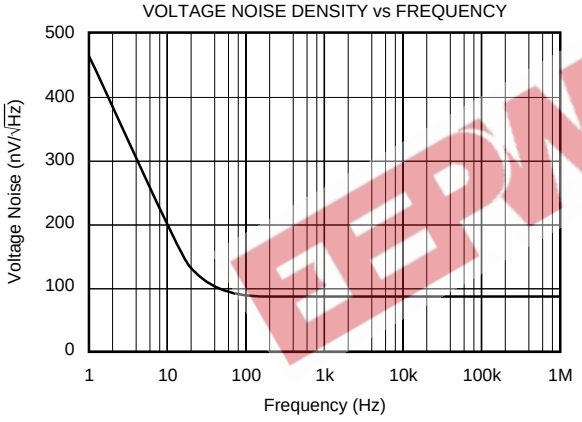
COMMON-MODE REJECTION vs FREQUENCY



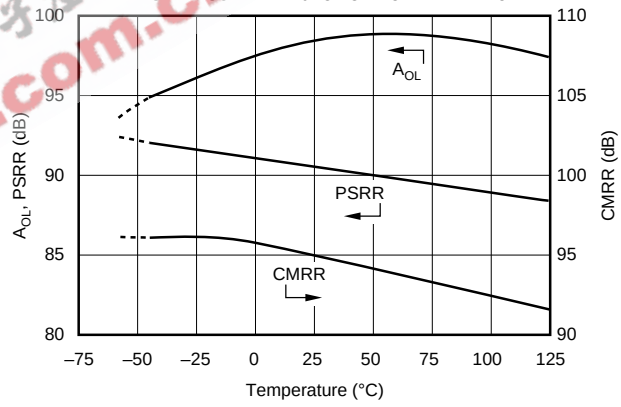

POWER SUPPLY REJECTION vs FREQUENCY



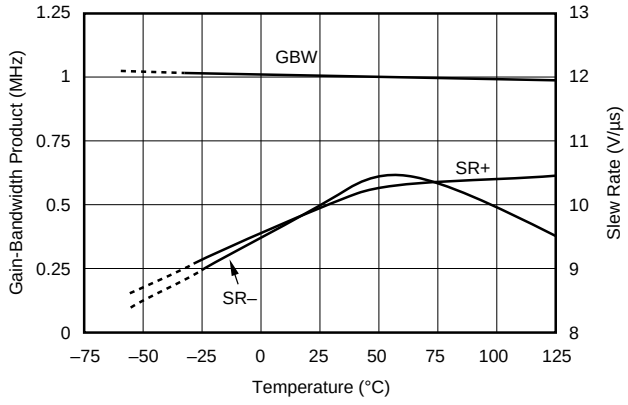

VOLTAGE NOISE DENSITY vs FREQUENCY



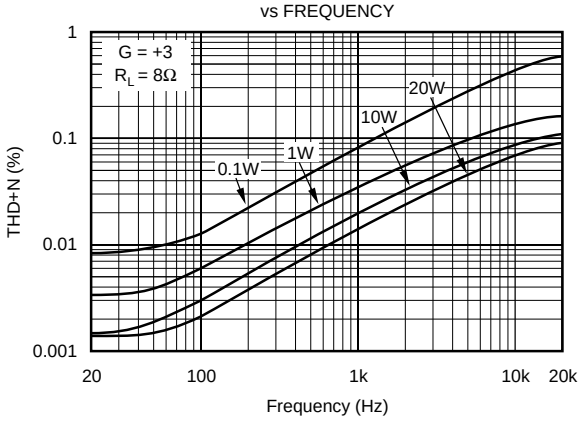

OPEN-LOOP GAIN, COMMON-MODE REJECTION, AND POWER SUPPLY REJECTION vs TEMPERATURE




GAIN-BANDWIDTH PRODUCT AND SLEW RATE vs TEMPERATURE




TOTAL HARMONIC DISTORTION+NOISE vs FREQUENCY

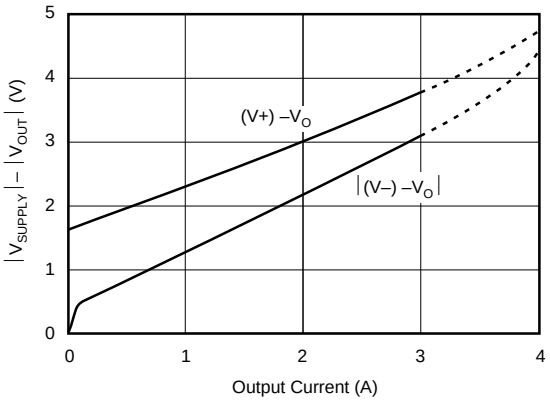



EEPW .com.cn

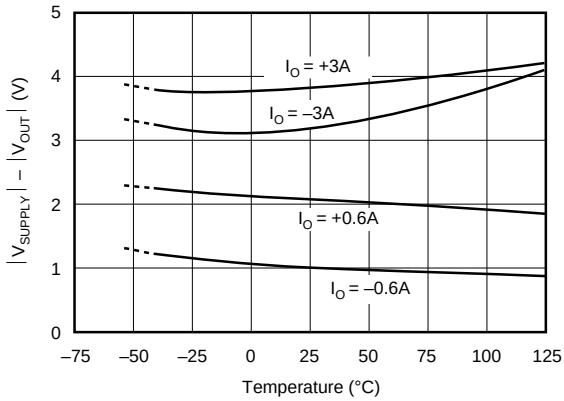
# TYPICAL PERFORMANCE CURVES (CONT)

At $T_{CASE}$ = +25°C, $V_S$ = ±30V and E/S pin open, unless otherwise noted.

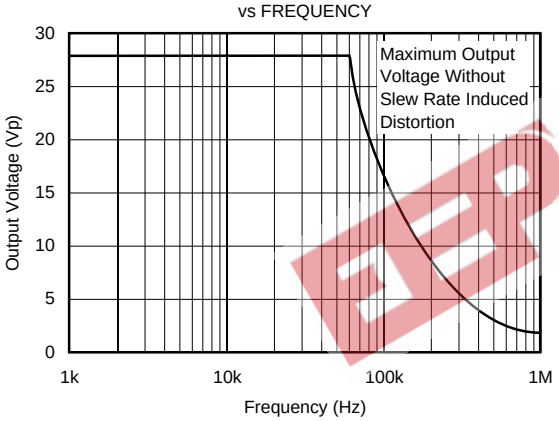
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



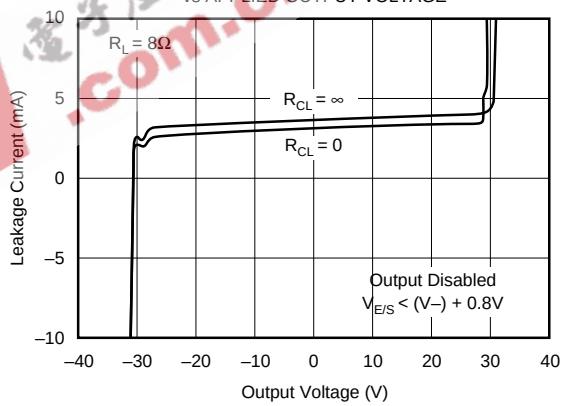

OUTPUT VOLTAGE SWING vs TEMPERATURE



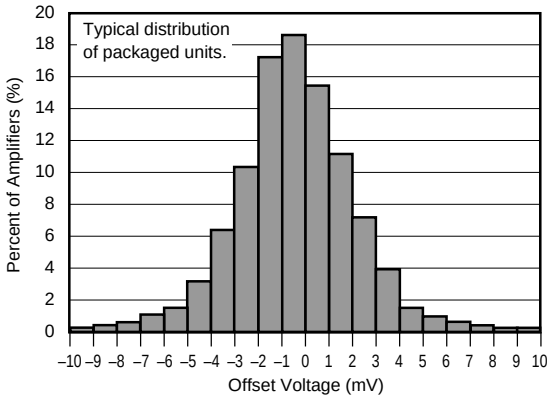

MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY



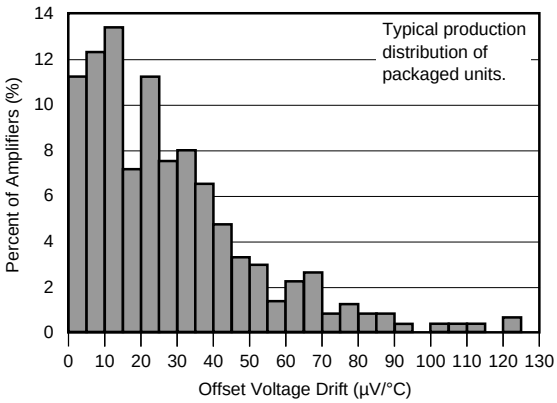

OUTPUT LEAKAGE CURRENT vs APPLIED OUTPUT VOLTAGE




OFFSET VOLTAGE PRODUCTION DISTRIBUTION



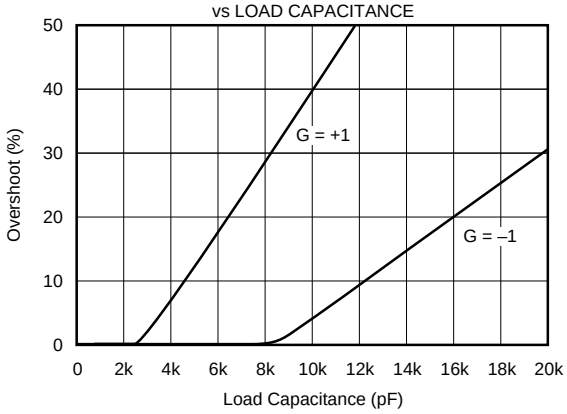

OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



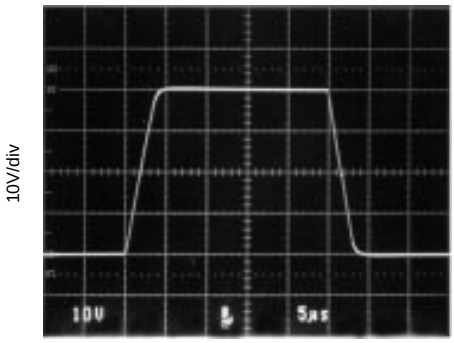
# TYPICAL PERFORMANCE CURVES (CONT)

At $T_{CASE}$ = +25°C, $V_S$ = ±30V and E/S pin open, unless otherwise noted.

SMALL-SIGNAL OVERSHOOT
vs LOAD CAPACITANCE

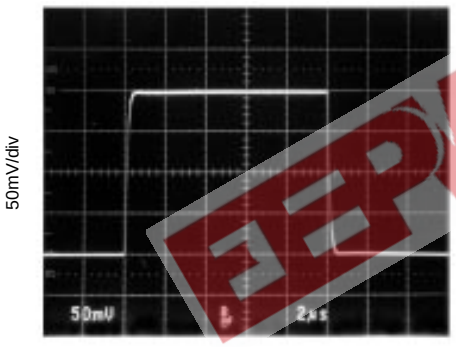



LARGE-SIGNAL STEP RESPONSE
G = 3, $C_L$ = 1000pF, $R_L$ = 8Ω



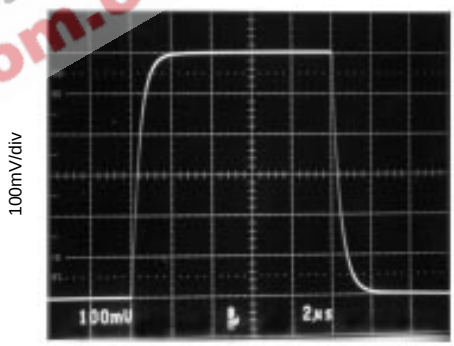

5µs/div

SMALL-SIGNAL STEP RESPONSE
G = 1, $C_L$ = 1000pF




2µs/div

SMALL-SIGNAL STEP RESPONSE
G = 3, $C_L$ = 1000pF




2µs/div

EEPW .com.cn

# APPLICATIONS INFORMATION

Figure 1 shows the OPA548 connected as a basic non-inverting amplifier. The OPA548 can be used in virtually any op amp configuration.

Power supply terminals should be bypassed with low series impedance capacitors. The technique shown, using a ceramic and tantalum type in parallel is recommended. In addition, we recommend a 0.01µF capacitor between V+ and V– as close to the OPA548 as possible. Power supply wiring should have low series impedance.

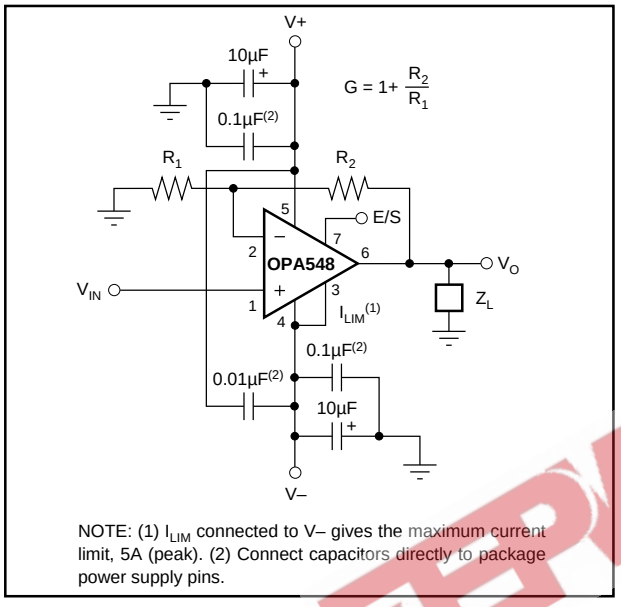



FIGURE 1. Basic Circuit Connections.

## POWER SUPPLIES

The OPA548 operates from single (+8V to +60V) or dual (±4V to ±30V) supplies with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the typical performance curves.

Some applications do not require equal positive and negative output voltage swing. Power supply voltages do not need to be equal. The OPA548 can operate with as little as 8V between the supplies and with up to 60V between the supplies. For example, the positive supply could be set to 55V with the negative supply at –5V, or vice-versa.

## ADJUSTABLE CURRENT LIMIT

The OPA548 features an accurate, user-selected current limit. Current limit is set from 0 to 5A by controlling the input to the $I_{LIM}$ pin. Unlike other designs which use a power resistor in series with the output current path, the OPA548 senses the load indirectly. This allows the current limit to be set with a 0 to 330µA control signal. In contrast, other designs require a limiting resistor to handle the full output current (5A in this case).

With the OPA548, the simplest method for adjusting the current limit uses a resistor or potentiometer connected between the $I_{LIM}$ pin and V– according to the equation:

$$R_{CL} = \frac{(15000)(4.75)}{I_{LIM}} - 13750\Omega$$

The low level control signal (0 to 330µA) also allows the current limit to be digitally controlled.

Figure 3 shows a simplified schematic of the internal circuitry used to set the current limit. Leaving the $I_{LIM}$ pin open programs the output current to zero, while connecting $I_{LIM}$ directly to V– programs the maximum output current limit, typically 5A.

## SAFE OPERATING AREA

Stress on the output transistors is determined both by the output current and by the output voltage across the conducting output transistor, $V_S - V_O$. The power dissipated by the output transistor is equal to the product of the output current and the voltage across the conducting transistor, $V_S - V_O$. The Safe Operating Area (SOA curve, Figure 2) shows the permissible range of voltage and current.

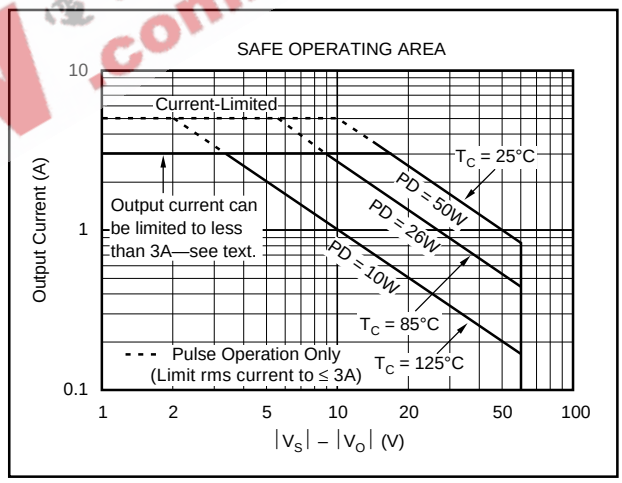
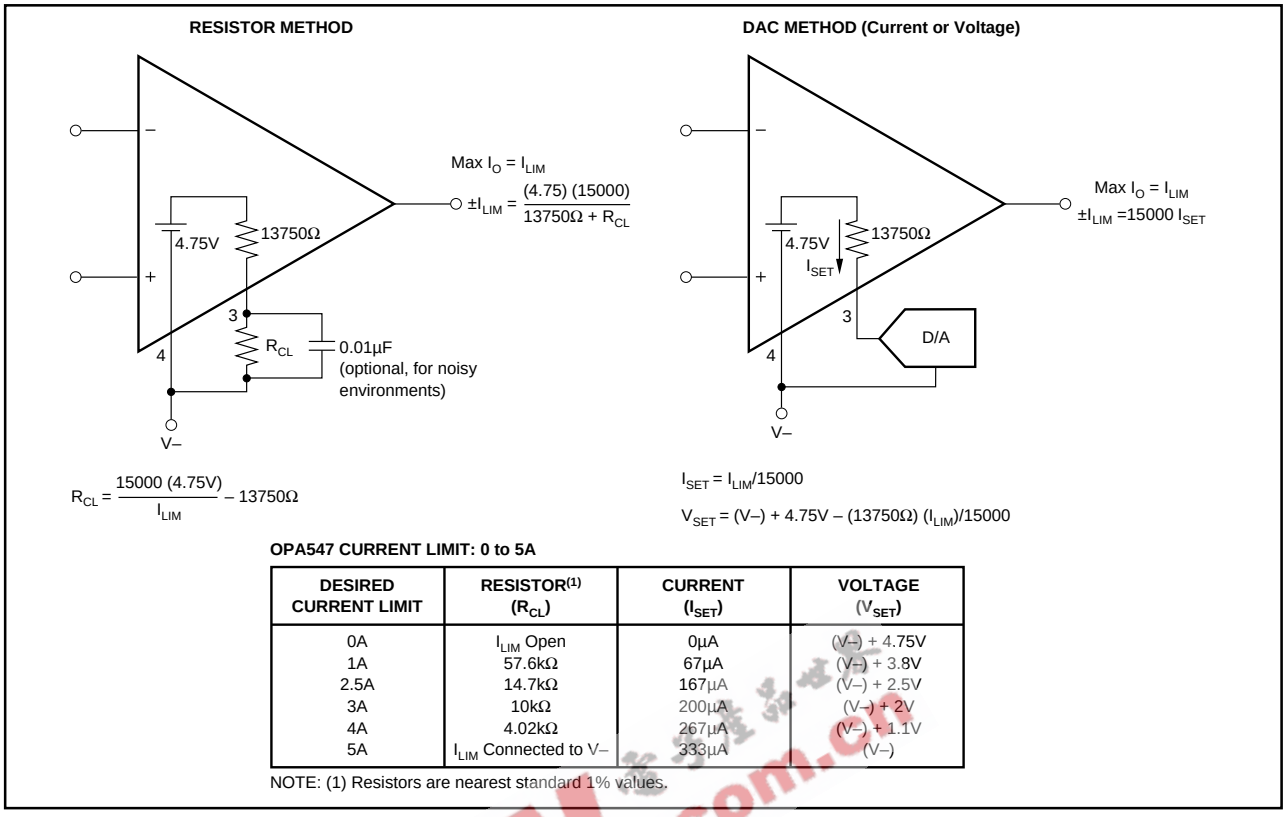



FIGURE 2. Safe Operating Area.

The safe output current decreases as $V_S - V_O$ increases. Output short-circuits are a very demanding case for SOA. A short-circuit to ground forces the full power supply voltage (V+ or V–) across the conducting transistor. Increasing the case temperature reduces the safe output current that can be tolerated without activating the thermal shutdown circuit of the OPA548. For further insight on SOA, consult Application Bulletin AB-039.

## AMPLIFIER MOUNTING

Figure 4 provides recommended solder footprints for both the TO-220 and DDPAK power packages. The tab of both packages is electrically connected to the negative supply, V–. It may be desirable to isolate the tab of TO-220 package from its

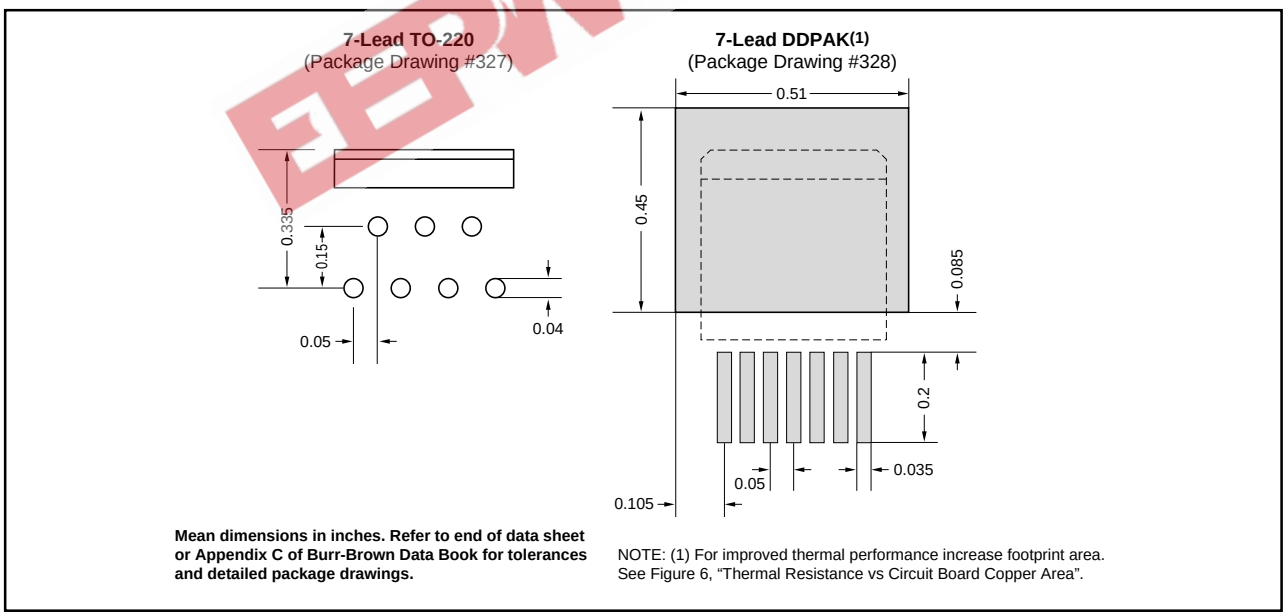



**OPA547 CURRENT LIMIT: 0 to 5A**

| DESIRED CURRENT LIMIT | RESISTOR(1) ($R_{CL}$) | CURRENT ($I_{SET}$) | VOLTAGE ($V_{SET}$) |
|---|---|---|---|
| 0A | $I_{LIM}$ Open | 0µA | (V–) + 4.75V |
| 1A | 57.6kΩ | 67µA | (V–) + 3.8V |
| 2.5A | 14.7kΩ | 167µA | (V–) + 2.5V |
| 3A | 10kΩ | 200µA | (V–) + 2V |
| 4A | 4.02kΩ | 267µA | (V–) + 1.1V |
| 5A | $I_{LIM}$ Connected to V– | 333µA | (V–) |

NOTE: (1) Resistors are nearest standard 1% values.

FIGURE 3. Adjustable Current Limit.




**Mean dimensions in inches. Refer to end of data sheet or Appendix C of Burr-Brown Data Book for tolerances and detailed package drawings.**

NOTE: (1) For improved thermal performance increase footprint area. See Figure 6, "Thermal Resistance vs Circuit Board Copper Area".

FIGURE 4. TO-220 and DDPAK Solder Footprints.

mounting surface with a mica (or other film) insulator (see Figure 5). For lowest overall thermal resistance it is best to isolate the entire heat sink/OPA548 structure from the mounting surface rather than to use an insulator between the semiconductor and heat sink.

For best thermal performance, the tab of the DDPAK surface-mount version should be soldered directly to a circuit board copper area. Increasing the copper area improves heat dissipation. Figure 6 shows typical thermal resistance from junction-to-ambient as a function of the copper area

## POWER DISSIPATION

Power dissipation depends on power supply, signal, and load conditions. For dc signals, power dissipation is equal to the product of output current times the voltage across the

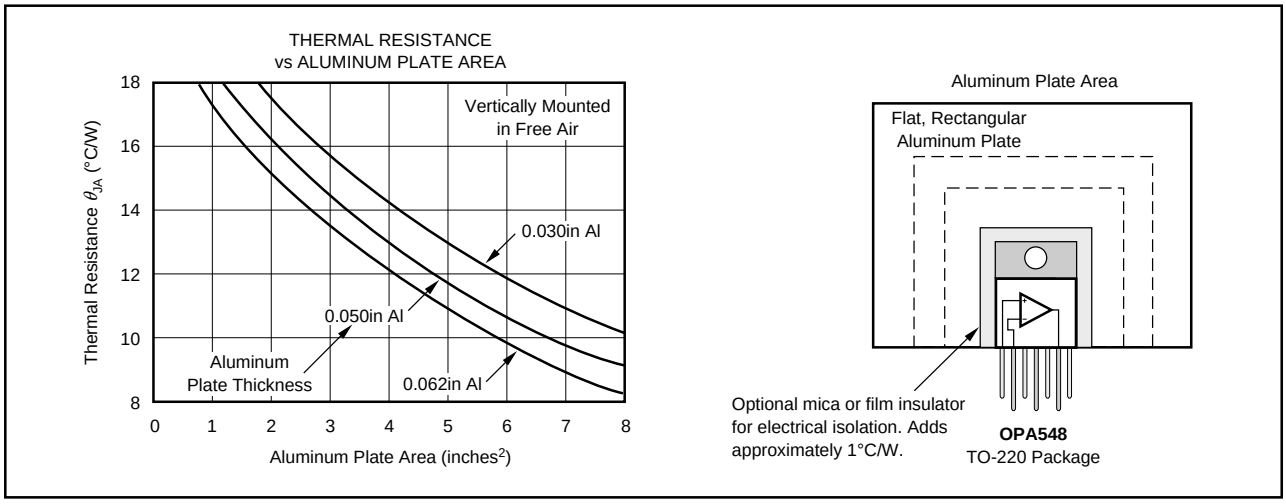



FIGURE 5. TO-220 Thermal Resistance vs Aluminum Plate Area.

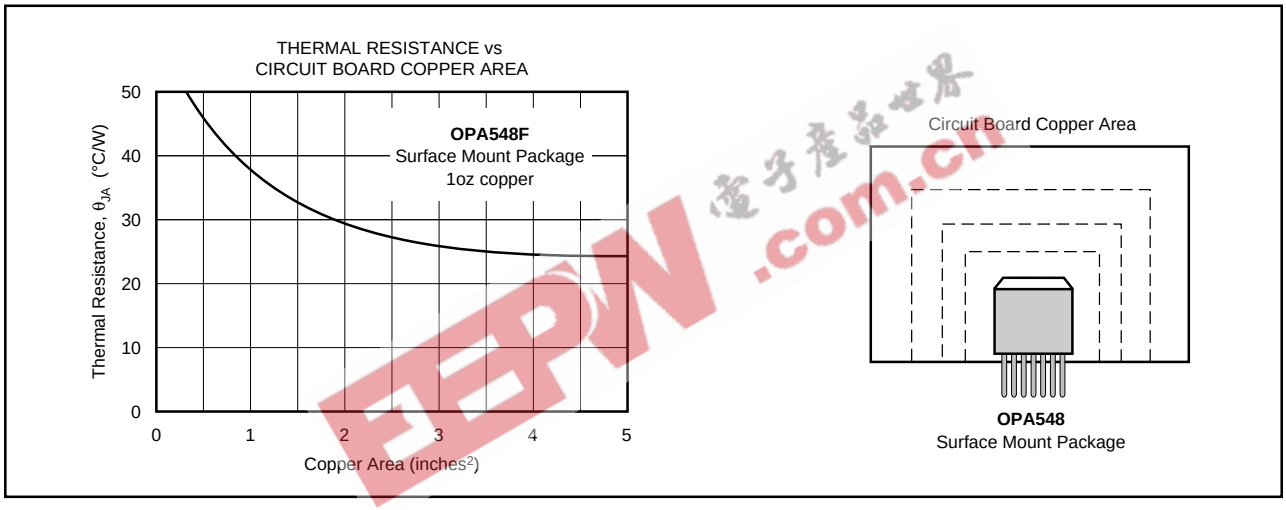



FIGURE 6. DDPAK Thermal Resistance vs Circuit Board Copper Area.

conducting output transistor. Power dissipation can be minimized by using the lowest possible power supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a dc output voltage of one-half the power supply voltage. Dissipation with ac signals is lower. Application Bulletin AB-039 explains how to calculate or measure power dissipation with unusual signals and loads.

## THERMAL PROTECTION

Power dissipated in the OPA548 will cause the junction temperature to rise. The OPA548 has thermal shutdown circuitry that protects the amplifier from damage. The thermal protection circuitry disables the output when the junction temperature reaches approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on load and signal conditions, the thermal protection circuit may cycle on and off. This limits the dissipation of the amplifier but may have an undesirable effect on the load.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to 125°C, maximum. To estimate the margin of safety in a complete design (including heat sink) increase the ambient temperature until the thermal protection is triggered. Use worst-case load and signal conditions. For good reliability, thermal protection should trigger more than 35°C above the maximum expected ambient condition of your application. This produces a junction temperature of 125°C at the maximum expected ambient condition.

The internal protection circuitry of the OPA548 was designed to protect against overload conditions. It was not intended to replace proper heat sinking. Continuously running the OPA548 into thermal shutdown will degrade reliability.

## HEAT SINKING

Most applications require a heat sink to assure that the maximum operating junction temperature (125°C) is not exceeded. In addition, the junction temperature should be kept as low as possible for increased reliability. Junction temperature can be determined according to the equation:

$$T_J = T_A + P_D\theta_{JA} \quad (1)$$

$$\text{where, } \theta_{JA} = \theta_{JC} + \theta_{CH} + \theta_{HA} \quad (2)$$

$T_J$ = Junction Temperature (°C)
$T_A$ = Ambient Temperature (°C)
$P_D$ = Power Dissipated (W)
$\theta_{JC}$ = Junction-to-Case Thermal Resistance (°C/W)
$\theta_{CH}$ = Case-to-Heat Sink Thermal Resistance (°C/W)
$\theta_{HA}$ = Heat Sink-to-Ambient Thermal Resistance (°C/W)
$\theta_{JA}$ = Junction-to-Air Thermal Resistance (°C/W)

Figure 7 shows maximum power dissipation versus ambient temperature with and without the use of a heat sink. Using a heat sink significantly increases the maximum power dissipation at a given ambient temperature as shown.

The difficulty in selecting the heat sink required lies in determining the power dissipated by the OPA548. For dc output into a purely resistive load, power dissipation is simply the load current times the voltage developed across the conducting output transistor, $P_D = I_L(V_S–V_O)$. Other loads are not as simple. Consult Application Bulletin AB-039 for further insight on calculating power dissipation. Once power dissipation for an application is known, the proper heat sink can be selected.

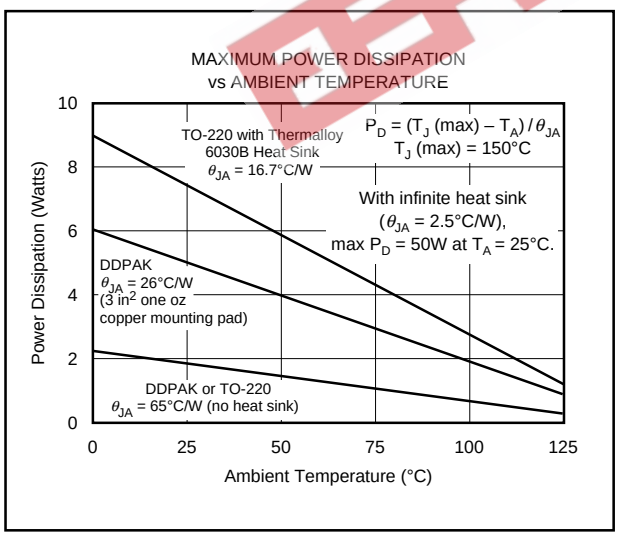



FIGURE 7. Maximum Power Dissipation vs Ambient Temperature.

### Heat Sink Selection Example

A TO-220 package is dissipating 5 Watts. The maximum expected ambient temperature is 40°C. Find the proper heat sink to keep the junction temperature below 125°C (150°C minus 25°C safety margin).

Combining equations (1) and (2) gives:

$$T_J = T_A + P_D(\theta_{JC} + \theta_{CH} + \theta_{HA}) \quad (3)$$

$T_J$, $T_A$, and $P_D$ are given. $\theta_{JC}$ is provided in the specification table, 2.5°C/W (dc). $\theta_{CH}$ can be obtained from the heat sink manufacturer. Its value depends on heat sink size, area, and material used. Semiconductor package type, mounting screw torque, insulating material used (if any), and thermal joint compound used (if any) also affect $\theta_{CH}$. A typical $\theta_{CH}$ for a TO-220 mounted package is 1°C/W. Now we can solve for $\theta_{HA}$:

$$\theta_{HA} = \frac{T_J - T_A}{P_D} - (\theta_{JC} + \theta_{CH})$$

$$\theta_{HA} = \frac{125°C - 40°C}{5W} - (2.5°C/W + 1°C/W) = 13.5°C/W$$

To maintain junction temperature below 125°C, the heat sink selected must have a $\theta_{HA}$ less than 14°C/W. In other words, the heat sink temperature rise above ambient must be less than 67.5°C (13.5°C/W x 5W). For example, at 5 Watts Thermalloy model number 6030B has a heat sink temperature rise of 66°C above ambient ($\theta_{HA}$ = 66°C/5W = 13.2°C/W), which is below the 67.5°C required in this example. Figure 7 shows power dissipation versus ambient temperature for a TO-220 package with a 6030B heat sink.

Another variable to consider is natural convection vs forced convection air flow. Forced-air cooling by a small fan can lower $\theta_{CA}$ ($\theta_{CH} + \theta_{HA}$) dramatically. Heat sink manufactures provide thermal data for both of these cases. For additional information on determining heat sink requirements, consult Application Bulletin AB-038.

As mentioned earlier, once a heat sink has been selected the complete design should be tested under worst-case load and signal conditions to ensure proper thermal protection.

## ENABLE/STATUS (E/S) PIN

The Enable/Status Pin provides two functions: forcing this pin low disables the output stage, or, E/S can be monitored to determine if the OPA548 is in thermal shutdown. One or both of these functions can be utilized on the same device using single or dual supplies. For normal operation (output enabled), the E/S pin can be left open or pulled high (at least 2.4V above the negative rail). A small value capacitor connected between the E/S pin and V– may be required for noisy applications.

### Output Disable

A unique feature of the OPA548 is its output disable capability. This function not only conserves power during idle periods (quiescent current drops to approximately 6mA) but also allows multiplexing in low frequency (f<20kHz), multichannel applications. Signals greater than 20kHz may cause leakage current to increase in devices that are shutdown. Figure 18 shows the two OPA548s in a switched amplifier configuration. The on/off state of the two amplifiers is controlled by the voltage on the E/S pin.

To disable the output, the E/S pin is pulled low, no greater than 0.8V above the negative rail. Typically the output is shutdown in 1µs. Figure 8 provides an example of how to implement this function using a single supply. Figure 9 gives a circuit for dual supply applications. To return the output to an enabled state, the E/S pin should be disconnected (open) or pulled to at least (V–) + 2.4V. It should be noted that pulling the E/S pin high (output enabled) does not disable internal thermal shutdown.

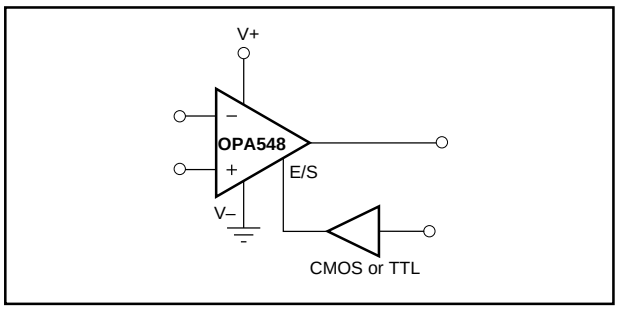



FIGURE 8. Output Disable with a Single Supply.

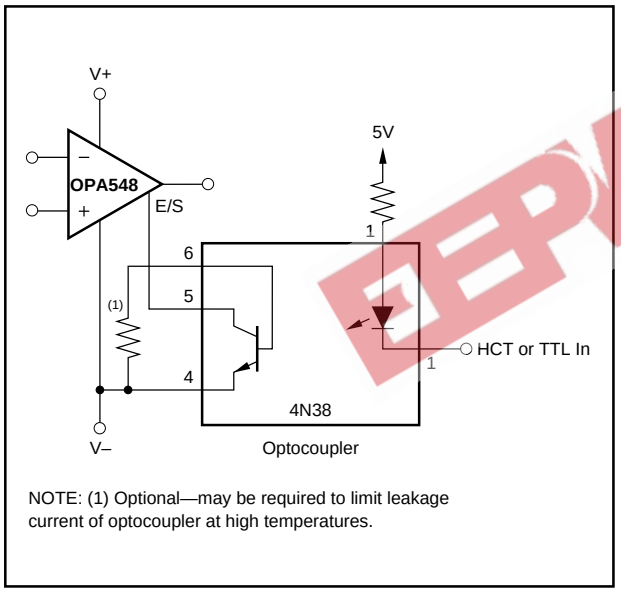



FIGURE 9. Output Disable with Dual Supplies.

### Thermal Shutdown Status

Internal thermal shutdown circuitry shuts down the output when the die temperature reaches approximately 160°C, resetting when the die has cooled to 140°C. The E/S pin can be monitored to determine if shutdown has occurred. During normal operation the voltage on the E/S pin is typically 3.5V above the negative rail. Once shutdown has occurred this voltage drops to approximately 350mV above the negative rail.

Figure 10 gives an example of monitoring shutdown in a single supply application. Figure 11 provides a circuit for dual supplies. External logic circuitry or an LED could be used to indicate if the output has been thermally shutdown, see Figure 16.

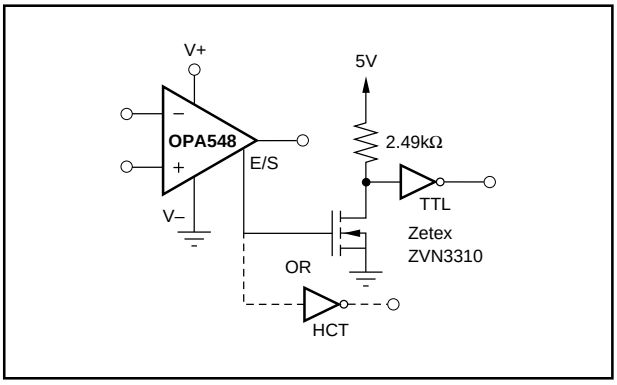



FIGURE 10. Thermal Shutdown Status with a Single Supply.

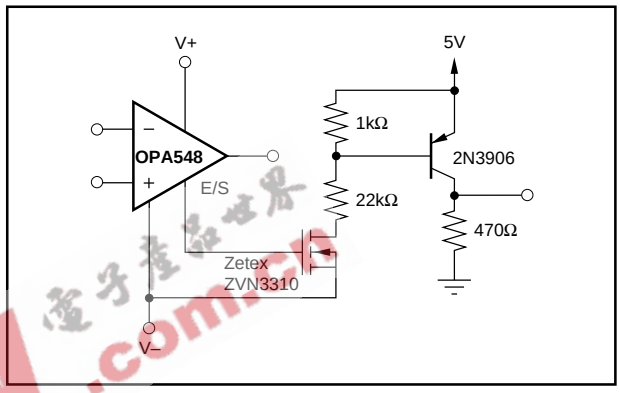



FIGURE 11. Thermal Shutdown Status with Dual Supplies.

### Output Disable and Thermal Shutdown Status

As mentioned earlier, the OPA548's output can be disabled and the disable status can be monitored simultaneously. Figures 12 and 13 provide examples interfacing to the E/S pin while using a single supply and dual supplies, respectively.

## OUTPUT STAGE COMPENSATION

The complex load impedances common in power op amp applications can cause output stage instability. For normal operation output compensation circuitry is typically not required. However, if the OPA548 is intended to be driven into current limit, an R/C network may be required. Figure 14 shows an output series R/C compensation (snubber) network which generally provides excellent stability.

A snubber circuit may also enhance stability when driving large capacitive loads (>1000pF) or inductive loads (motors, loads separated from the amplifier by long cables). Typically 3Ω to 10Ω in series with 0.01µF to 0.1µF is adequate. Some variations in circuit value may be required with certain loads.

## OUTPUT PROTECTION

Reactive and EMF-generating loads can return load current to the amplifier, causing the output voltage to exceed the power supply voltage. This damaging condition can

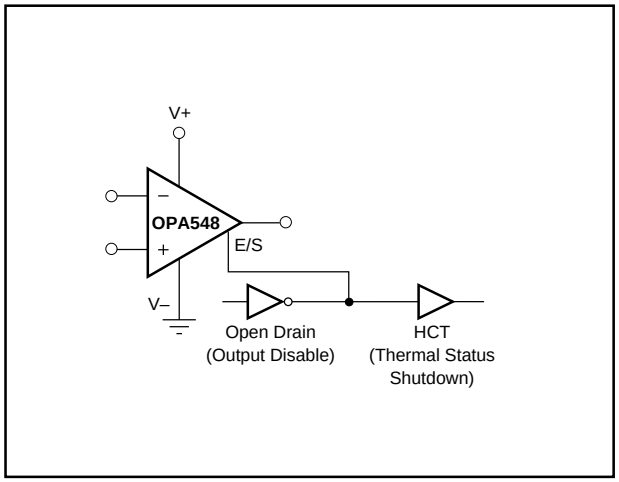



FIGURE 12. Output Disable and Thermal Shutdown Status with a Single Supply.

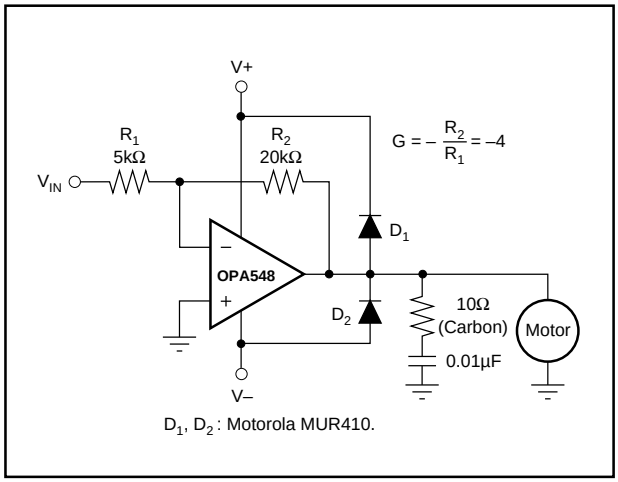



FIGURE 14. Motor Drive Circuit.

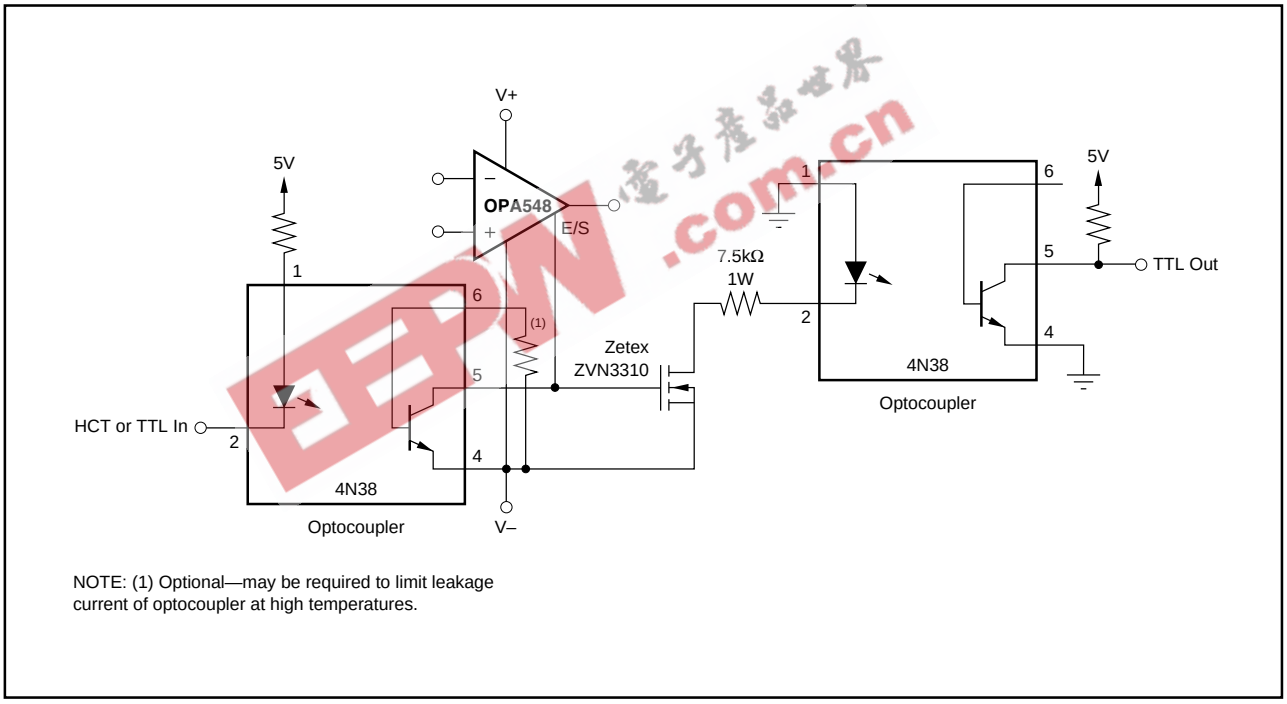



FIGURE 13. Output Disable and Thermal Shutdown Status with Dual Supplies.

be avoided with clamp diodes from the output terminal to the power supplies as shown in Figure 14. Schottky rectifier diodes with a 5A or greater continuous rating are recommended.

## VOLTAGE SOURCE APPLICATION

Figure 15 illustrates how to use the OPA548 to provide an accurate voltage source with only three external resistors. First, the current limit resistor, $R_{CL}$, is chosen according to the desired output current. The resulting voltage at the $I_{LIM}$ pin is constant and stable over temperature. This voltage, $V_{CL}$, is connected to the noninverting input of the op amp and used as a voltage reference, thus eliminating the need for an external reference. The feedback resistors are selected to gain $V_{CL}$ to the desired output voltage level.

## PROGRAMMABLE POWER SUPPLY

A programmable source/sink power supply can easily be built using the OPA548. Both the output voltage and output current are user-controlled. Figure 16 shows a circuit using potentiometers to adjust the output voltage and current while Figure 17 uses digital-to-analog converters. An LED tied to the E/S pin through a logic gate indicates if the OPA548 is in thermal shutdown.

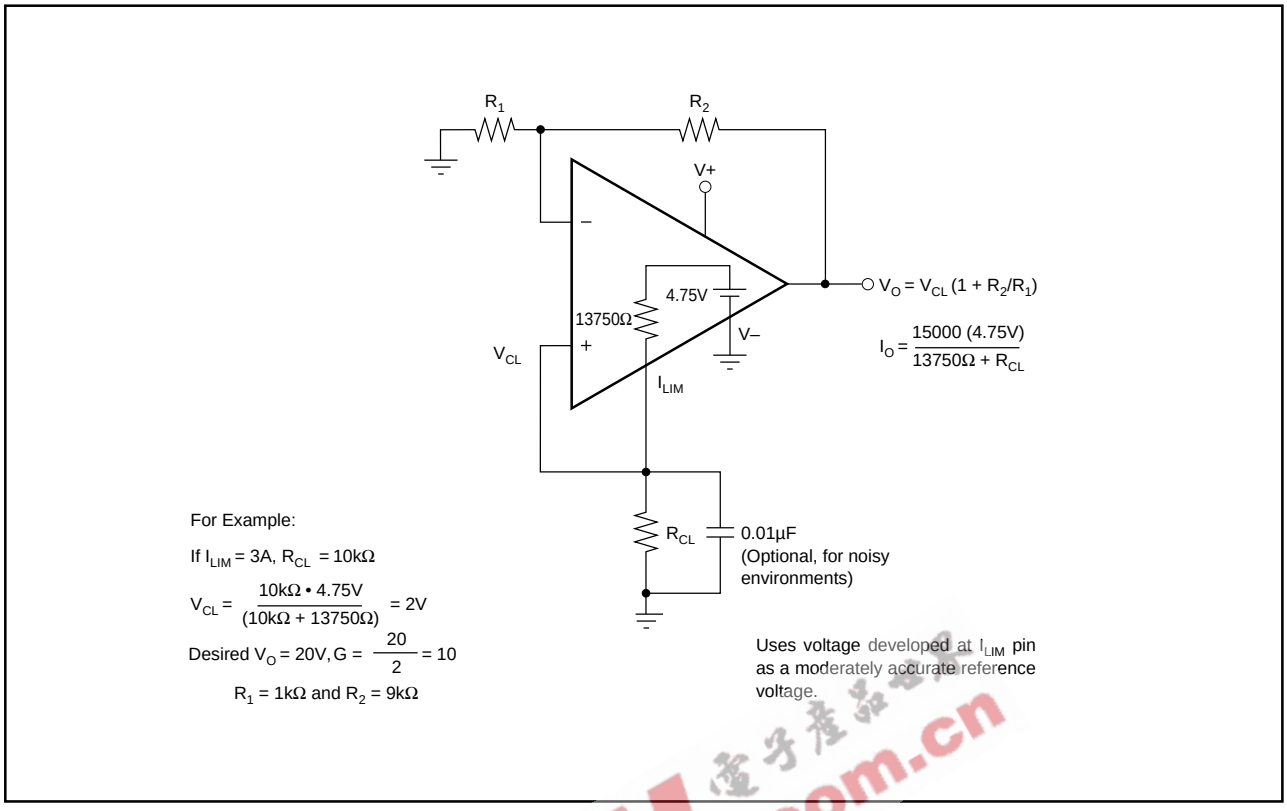



FIGURE 15. Voltage Source.

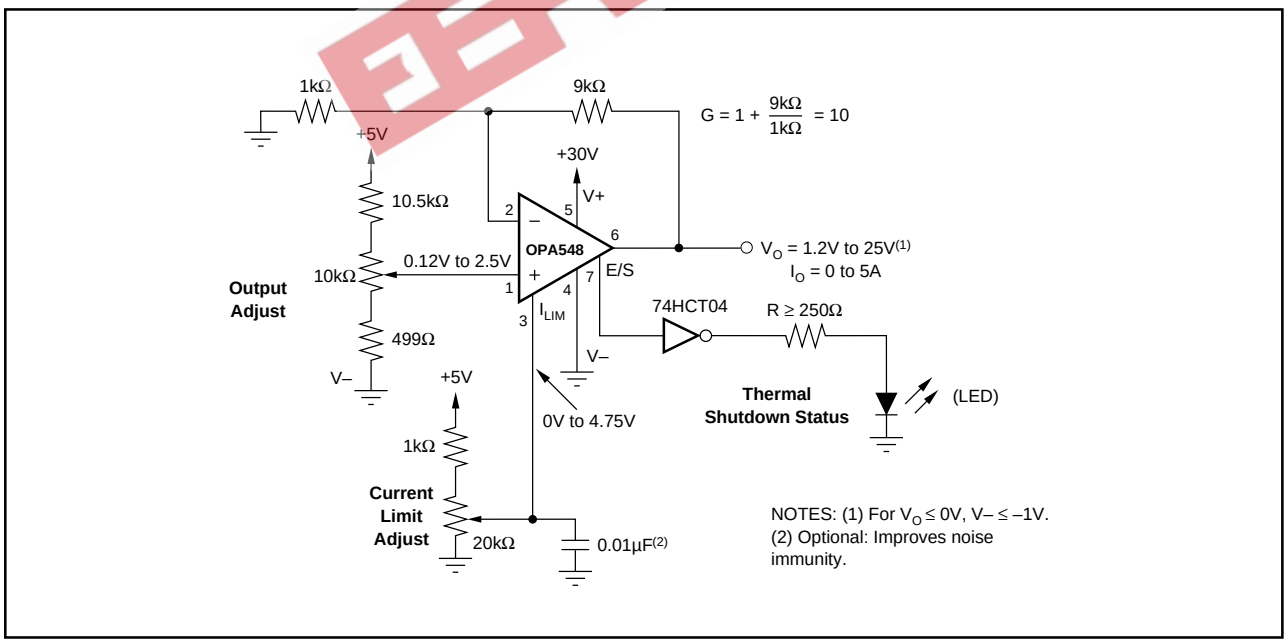



FIGURE 16. Resistor-Controlled Programmable Power Supply.

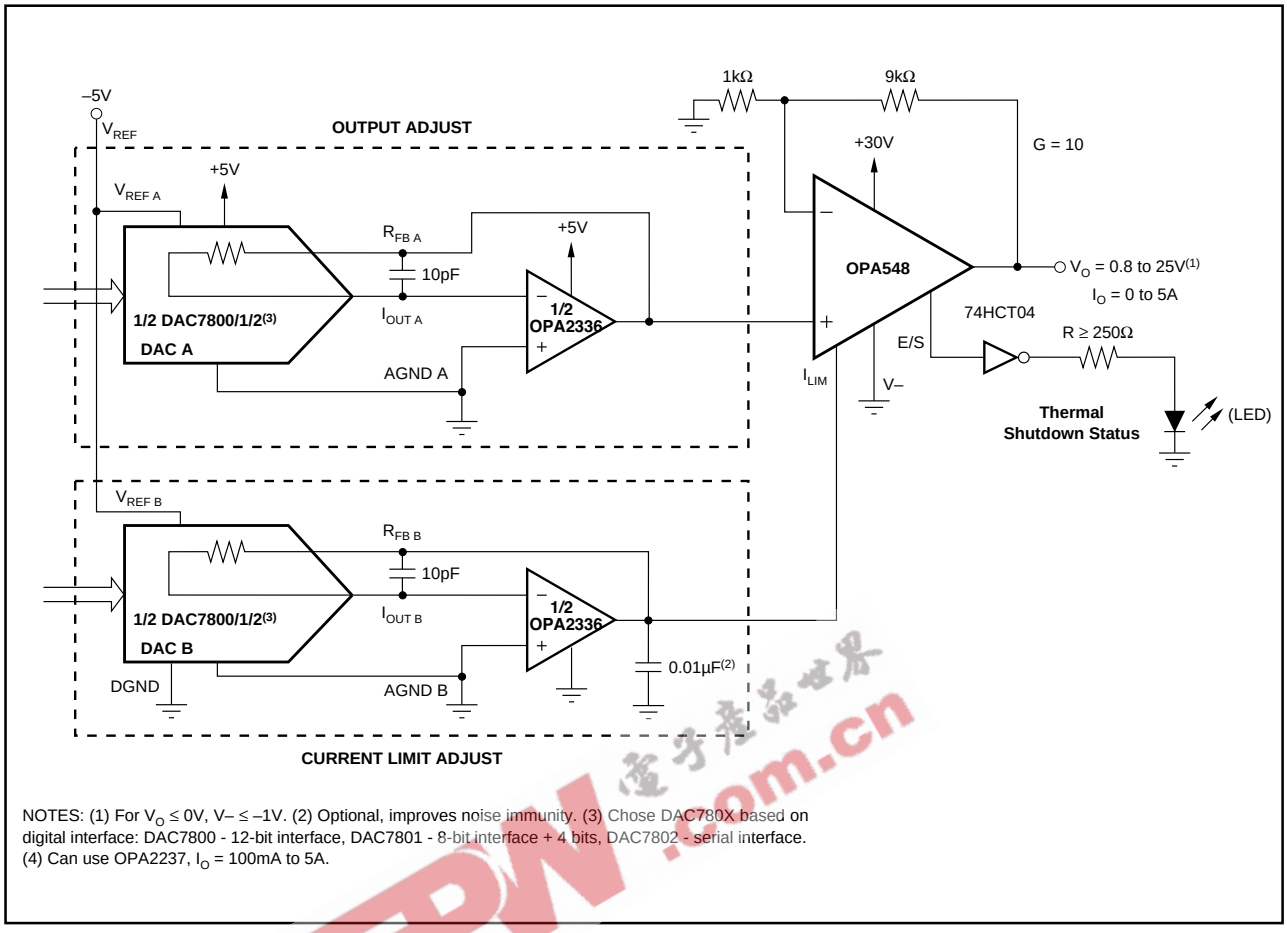



FIGURE 17. Digitally-Controlled Programmable Power Supply.

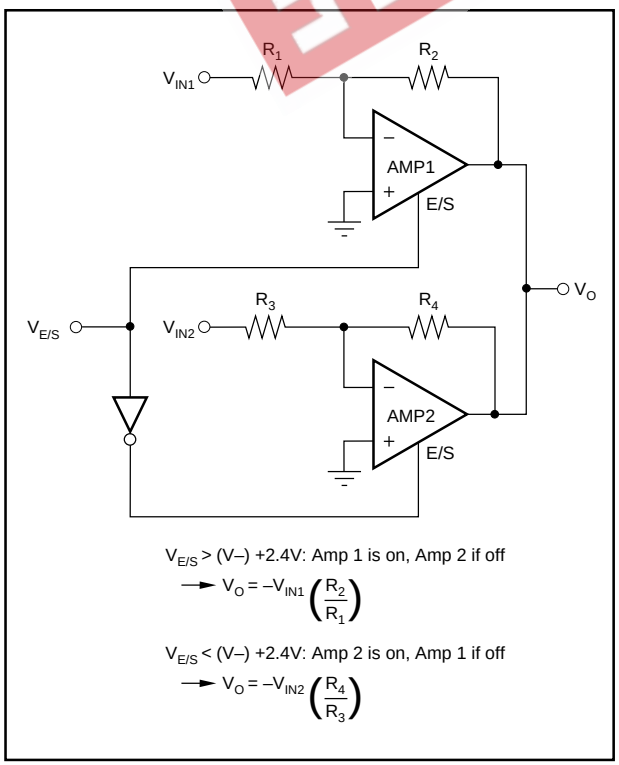



FIGURE 18. Switched Amplifier.

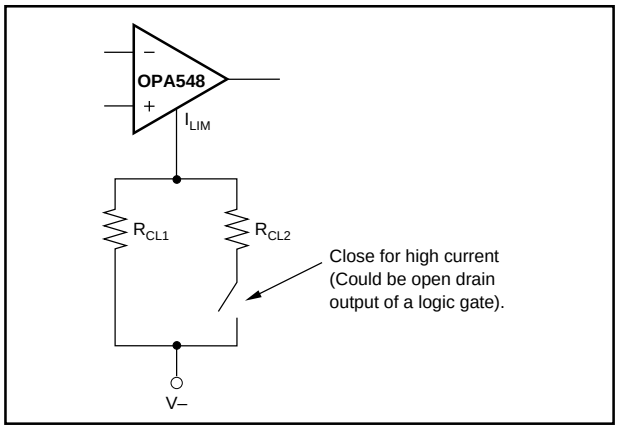



FIGURE 19. Multiple Current Limit Values.

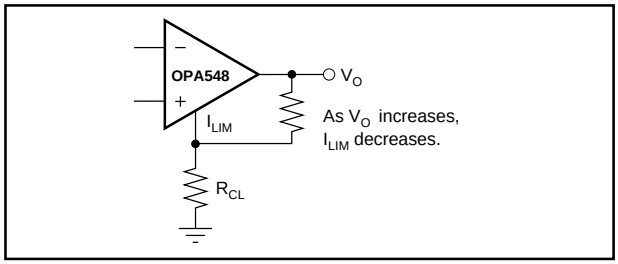
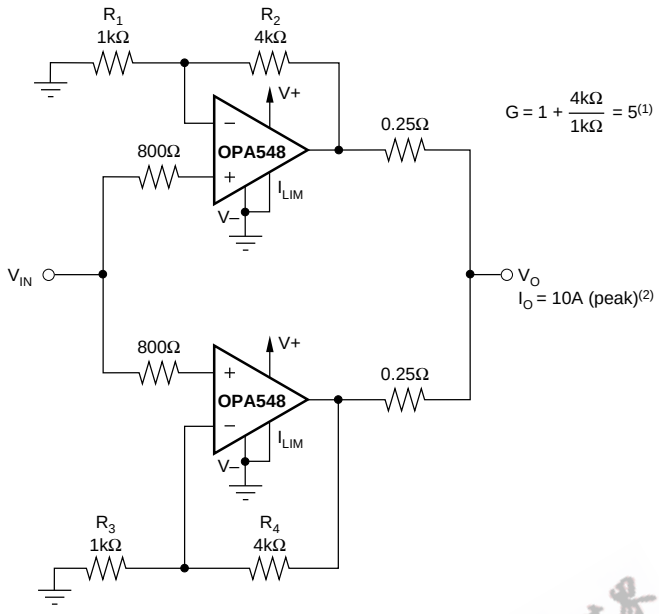



FIGURE 20. Single Quadrant V • I Limiting.




NOTES: (1) Works well for G < 10. Input offset causes output current to flow between amplifiers with G > 10. Gains (resistor ratios) of the two amplifiers should be carefully matched to ensure equal current sharing. (2) As configured ($I_{LIM}$ connected to V–) output current limit is set to 10A (peak). Each amplifier is limited to 5A (peak). Other current limit values may be obtained, see Figure 3, “Adjustable Current Limit”.

FIGURE 21. Parallel Output for Increased Output Current.

EEPW .com.cn