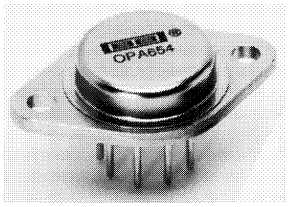
BURR-BROWN®



OPA654

Wide Bandwidth, High Output Current *Difet* ® OPERATIONAL AMPLIFIER

FEATURES

- HIGH SLEW RATE: 750V/µs
- HIGH OUTPUT CURRENT: 200mA
- WIDE GAIN-BANDWIDTH: 700MHz
- FAST SETTLING: 150ns to 0.1%
- FET INPUT: I_B = 50pA max

APPLICATIONS

- LINE DRIVERS
- PIN DRIVERS
- HIGH-SPEED DATA ACQUISITION
- WAVEFORM GENERATORS

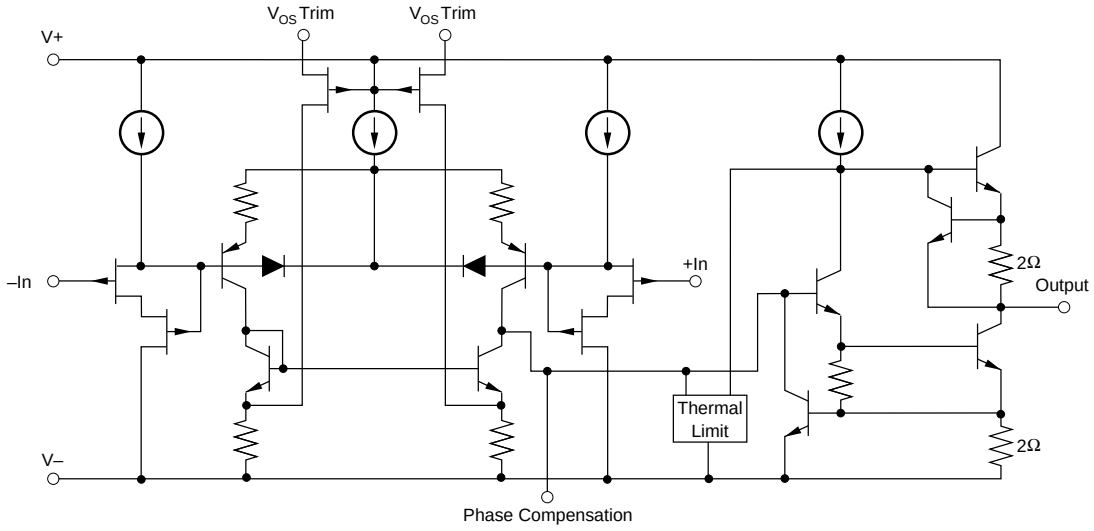
DESCRIPTION

The OPA654 is a high-speed monolithic operational amplifier featuring 200mA output current. Fabricated using Burr-Brown's Complementary-Bipolar, ***Difet*** process, it provides an excellent combination of high speed and high output current.

The OPA654 is versatile, operating from power supplies ranging from ±5V to ±18V. It can deliver up to ±10V signals into a 50Ω load at slew rates of 750V/µs. Its speed and output current make it useful for line driver and automatic test applications.

The OPA654 is externally compensated, allowing open-loop gain and phase characteristics to be optimized for the desired closed-loop gain, load and dynamic characteristics.

The OPA654 is available in an 8-pin metal TO-3 package that provides excellent thermal characteristics and is specified for the industrial temperature range.



Difet ®, Burr-Brown Corp.

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PDS-1098B
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SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_S = ±15V unless otherwise noted.

PARAMETER	CONDITION	OPA654AM MIN	OPA654AM TYP	OPA654AM MAX	UNITS
FREQUENCY RESPONSE					
Gain-Bandwidth Product [2]			See Typical Curve		
Slew Rate [2,3]	G = –1, 20V Step		750		V/µs
Settling Time [2] 0.01%	G = –1, 10V Step		240		ns
0.1%	G = –1, 10V Step		150		ns
1%	G = –1, 10V Step		85		ns
OFFSET VOLTAGE					
Input Offset Voltage			±0.1	±3	mV
Average Drift			±40		µV/°C
Power Supply Rejection	V_S = ±5 to ±15V	72	82		dB
INPUT BIAS CURRENT[1]					
Input Bias Current	V_{CM} = 0V		3	50	pA
Input Offset Current	V_{CM} = 0V		2	25	pA
NOISE					
Input Voltage Noise					
Noise Density,	f = 10Hz		115		nV/√Hz
	f = 100Hz		37		nV/√Hz
	f = 1kHz		19		nV/√Hz
	f = 10kHz		14		nV/√Hz
Voltage Noise,	f_B = 10Hz to 1MHz		85		µVp-p
Input Bias Current Noise					
Current Noise Density, f = 0.1Hz to 20kHz			1		fA/√Hz
INPUT VOLTAGE RANGE					
Common-Mode Input Range		±12	±13		V
Common-Mode Rejection	V_{CM} = ±10V	70	76		dB
INPUT IMPEDANCE					
Differential			10^{12} || 2.5		Ω || pF
Common-Mode			10^{12} || 3.2		Ω || pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain	V_O = ±10V, R_L = 1kΩ		94		dB
	V_O = ±10V, R_L = 50Ω	80	82		dB
OUTPUT					
Voltage Output	R_L = 50Ω	±11	±12.3		V
Current Output	V_O = ±10V		200		mA
Short Circuit Current			325		mA
Output Resistance, Open-Loop	DC		800		Ω
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±5		±18	V
Quiescent Current			±38	±43	mA
TEMPERATURE RANGE					
Specification		–25		+85	°C
Operating		–55		+125	°C
Storage		–55		+150	°C
Thermal Resistance, θ_{JC}			15		°C/W
θ_{JA}			45		°C/W

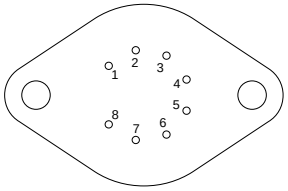
NOTES: (1) High-speed test at T_J = 25°C. (2) Varies with external phase compensation, C_1. See typical curves for performance with other gains and C_1. (3) Slew rate is rate of change from 10% to 90% of output voltage step.

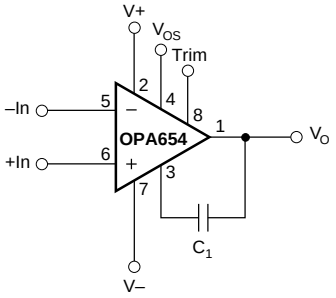
PIN CONFIGURATION

"M" TO-3 Metal Package

PIN LIST
1. V_O
2. V+
3. Compensation
4. V_{OS} Trim
5. –In
6. +In
7. V–
8. V_{OS} Trim

BOTTOM VIEW





Case is connected to IC substrate. Connect case to ground—see text.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±18V
Input Voltage	$\pm V_S$ ±1V
Output Short Circuit (to ground)	10s
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +150°C
Junction Temperature	+165°C
Lead Temperature (soldering, 10s)	+300°C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA654AM	8-Pin Metal TO-3	030

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

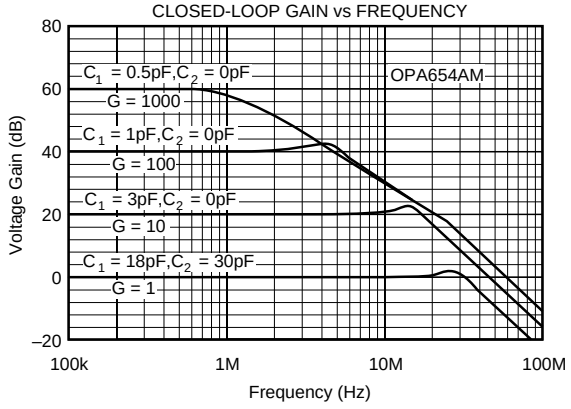
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA654AM	8-Pin Metal TO-3	–25°C to +85°C

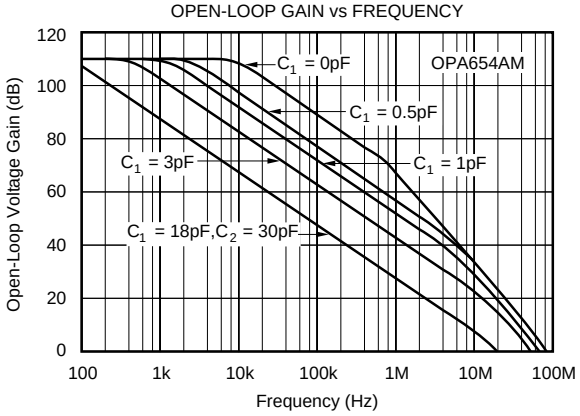
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

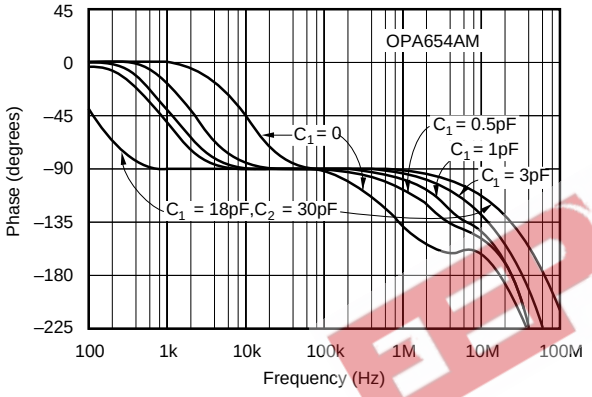
CLOSED-LOOP GAIN vs FREQUENCY



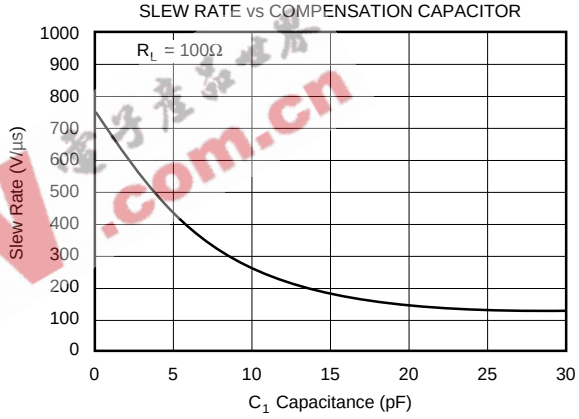
OPEN-LOOP GAIN vs FREQUENCY



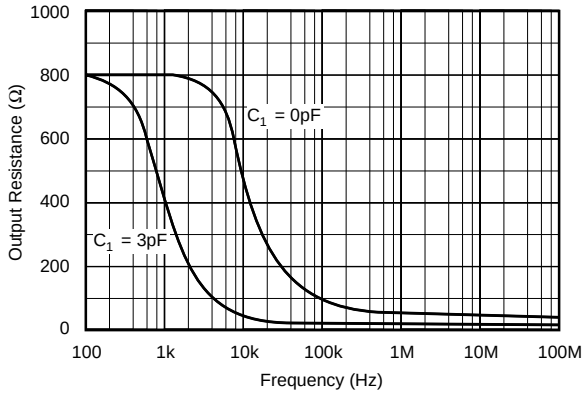
OPEN-LOOP PHASE vs FREQUENCY



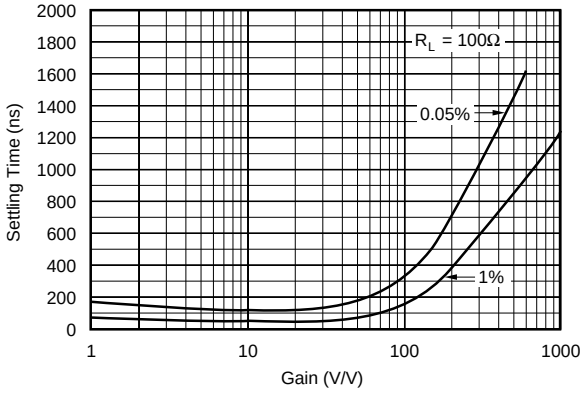
SLEW RATE vs COMPENSATION CAPACITOR



OPEN-LOOP OUTPUT RESISTANCE vs FREQUENCY



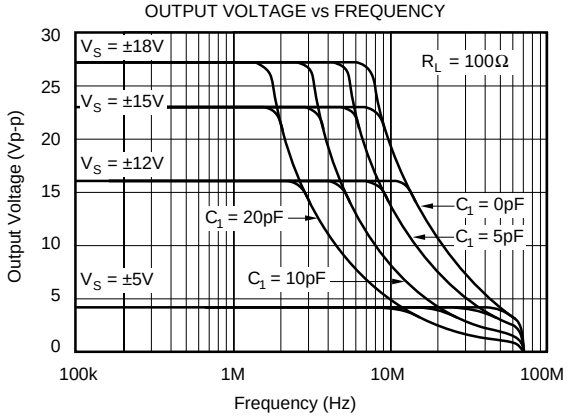
SETTLING TIME vs CLOSED-LOOP GAIN



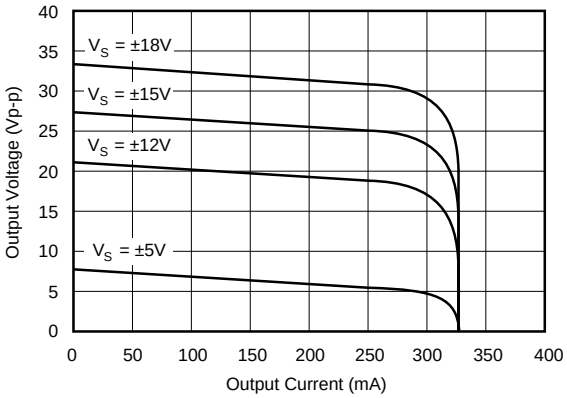
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

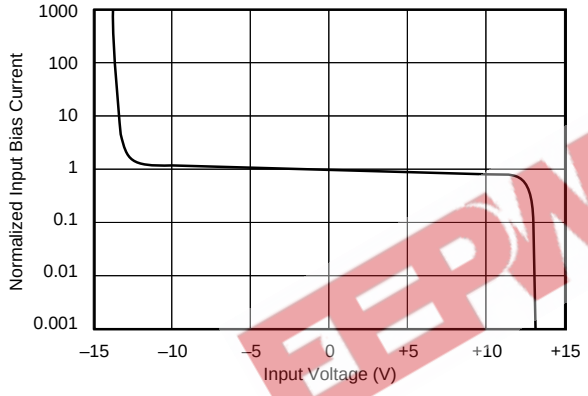
OUTPUT VOLTAGE vs FREQUENCY



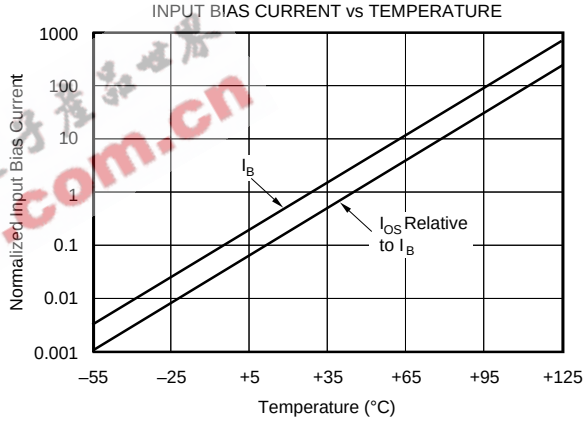
OUTPUT VOLTAGE vs OUTPUT CURRENT



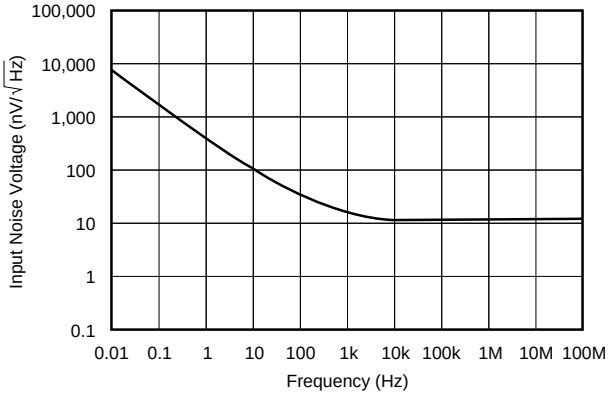
INPUT BIAS CURRENT



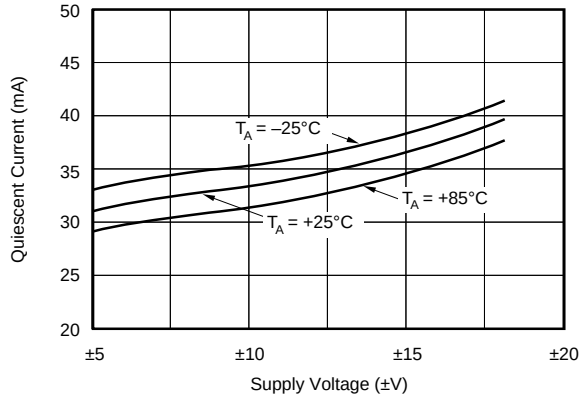
INPUT BIAS CURRENT vs TEMPERATURE



INPUT VOLTAGE NOISE SPECTRAL DENSITY

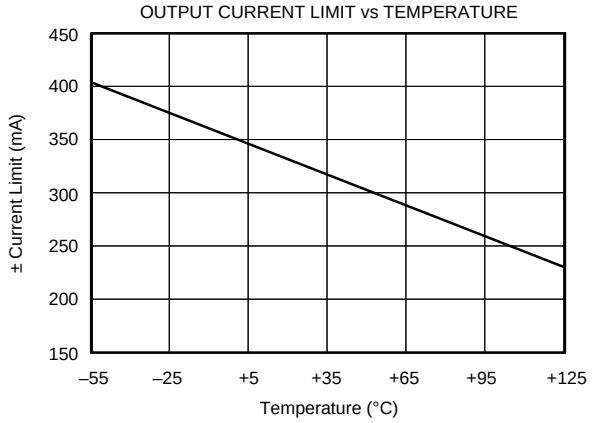


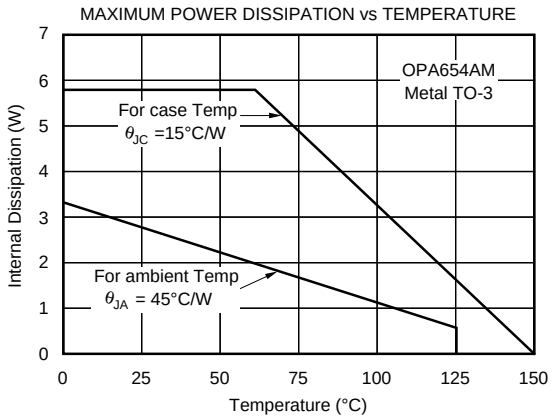
QUIESCENT CURRENT vs POWER SUPPLY VOLTAGE



TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.





CIRCUIT LAYOUT

With any wide-bandwidth circuitry, careful circuit layout will ensure best performance. Make short, direct circuit interconnections and avoid stray wiring capacitance—especially at the inverting input pin. A component-side ground plane will help ensure low ground impedance. Do not place the ground plane under or near the inputs and feedback network.

Power supplies should be bypassed with good high-frequency capacitors positioned close to the op amp pins. In most cases, a 2.2µF solid tantalum capacitor for each power supply is adequate. The OPA654 can deliver load currents up to 200mA. Even if steady-state load currents are lower, signal transients may demand large current transients from the power supplies. It is the power supply bypass capacitors which must supply these current transients. Larger bypass capacitors such as 10µF solid tantalum capacitors may improve dynamic performance in these applications.

CASE CONNECTION

The case of the TO-3 metal package should be connected to ground. Failure to connect the case to ground will not damage the device but will degrade its AC performance. The case is internally connected to the substrate of the dielectrically isolated IC. This substrate is DC-neutral—it is not connected to the V– power supply as it would be with most analog ICs. In principle, it could be connected to any AC ground potential such as one of the power supplies, but DC ground is usually most convenient. Do not connect the case to DC potentials which exceed the power supply voltages, $\pm V_S$.

OFFSET ADJUSTMENT

Many applications require no external offset voltage adjustment. Figure 1a shows connection of an optional offset voltage trimming potentiometer. Use a small, non-inductive potentiometer with short connections to the trim pins. Avoid stray capacitance from the input or output nodes. The added resistors in Figure 1b help decouple the potentiometer from these sensitive nodes, making the type and location of the potentiometer less critical. This also reduces the trim range, providing more adjustment resolution. Do not use an offset voltage adjustment to correct for offsets produced in other circuitry since this can introduce large offset voltage drift.

COMPENSATION

The OPA654 uses external compensation capacitors. This tailors the open-loop response characteristics to the application. Its effect can be seen in the open-loop gain and phase curves.

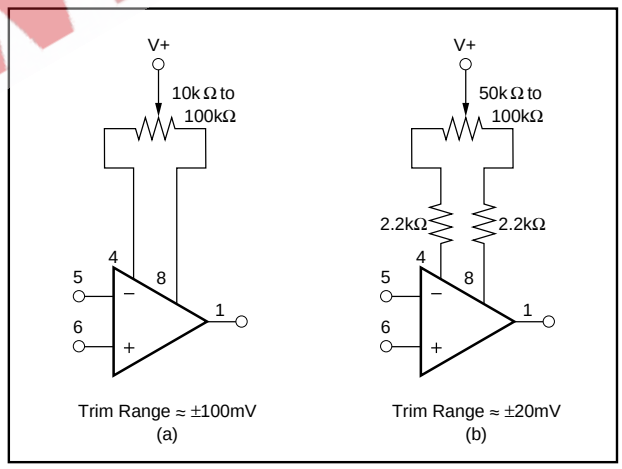
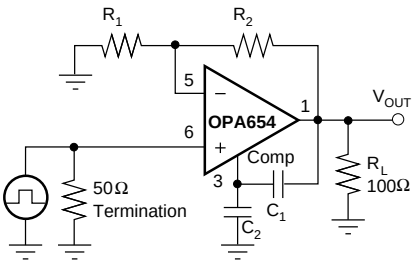
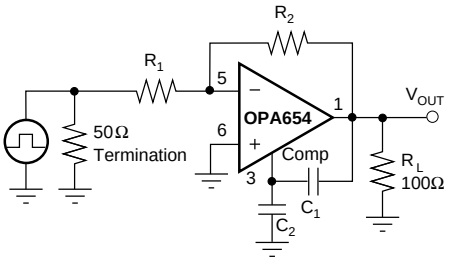


FIGURE 1. Optional Offset Voltage Trim Circuits.

Figures 2 shows typical capacitor values for various closed-loop gains. This chart should be considered a starting point for optimizing an application. Many variables including circuit layout, source and load characteristics, and desired dynamic behavior will affect the optimum capacitor values. Capacitive loads change op amp behavior and higher compensation capacitor values are generally required. Resistor R_S, shown in Figure 3, can improve the ability to drive a capacitive load. Typical values for R_S range from 5Ω to 50Ω, depending on the load and how much voltage drop can be tolerated.

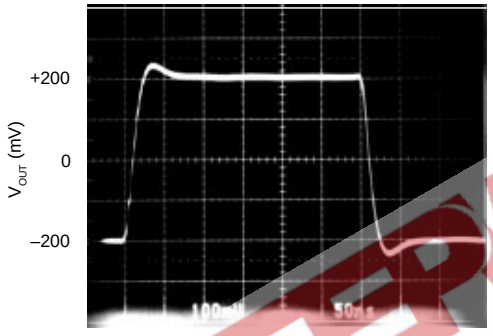




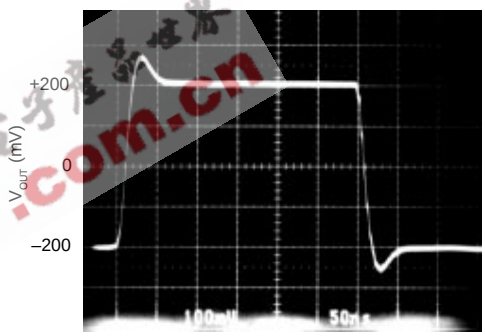
CLOSED-LOOP GAIN	C_1	C_2	R_1	R_2
+1000	0.5pF	0	10Ω	10kΩ
+100	1pF	0	100Ω	10kΩ
+10	3pF	0	100Ω	900Ω
+1	18pF	30pF	—	0

CLOSED-LOOP GAIN	C_1	C_2	R_1	R_2
–1000	0.5pF	0	10Ω	10kΩ
–100	1pF	0	100Ω	10kΩ
–10	3pF	0	100Ω	1kΩ
–1	18pF	20pF	1kΩ	1kΩ

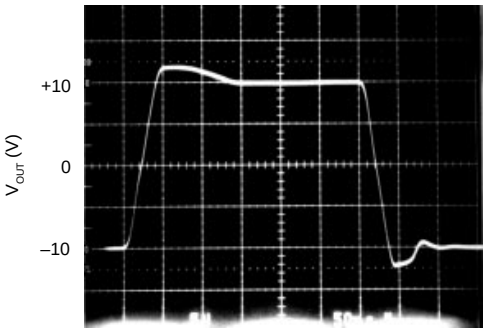
G = +10 SMALL-SIGNAL RESPONSE, R_L =100Ω



G = –10 SMALL-SIGNAL RESPONSE, R_L =100Ω



G = +10 LARGE-SIGNAL RESPONSE, R_L =100Ω



G = –10 LARGE-SIGNAL RESPONSE, R_L =100Ω

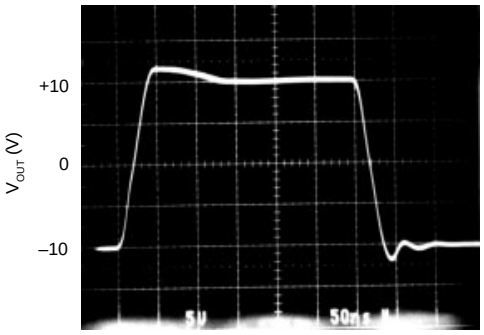


FIGURE 2. Basic Amplifier Circuits.

Figure 3 also demonstrates a compensation technique using an additional network, R_3-C_3. This allows use of a smaller value for C_1, producing a corresponding increase in slew rate. It reduces the high frequency loop gain by placing the op amp in a higher noise gain at high frequency. This technique improves large-signal response at the sacrifice of small-signal behavior. Settling time is increased and high frequency noise performance will be somewhat degraded.

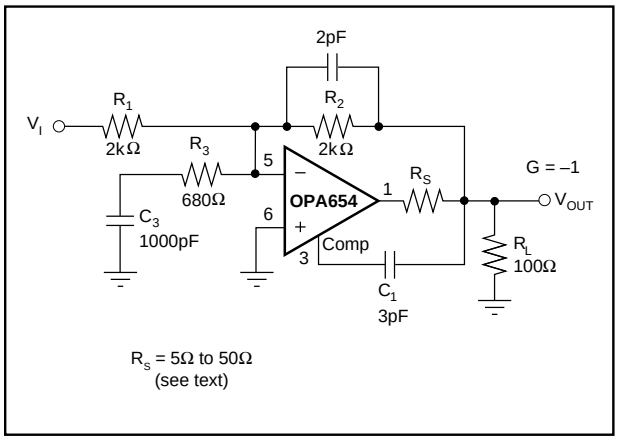


FIGURE 3. High Slew Rate Compensation Circuit.

Figure 4 shows an alternative compensation network for unity gain. This technique provides a small amount of positive feedback, reducing the net negative feedback factor. Large signal response and load driving capability is improved with this approach.

The compensation for a given application can be evaluated by observing amplifier pulse response. Both small-signal and large-signal response should be checked to assure that both are acceptable. Large overshoot or many cycles of ringing in the small-signal response is a sign of instability and the circuit may require further optimization. Good practice dictates a somewhat conservative approach to allow for device-to-device variation.

POWER DISSIPATION

Many applications do not require an external heat sink. However, with high ambient temperature or heavy load conditions, a heat sink may be required. The heat sink should be electrically connected to ground—see "Connections to Case". Operate within the power derating curve (Maximum Power Dissipation vs Temperature) shown in the typical performance curve section.

Exceeding the maximum die temperature of 165°C may activate the internal thermal limit circuitry, disabling the output stage. This thermal limit is set for a junction temperature of approximately 185°C.

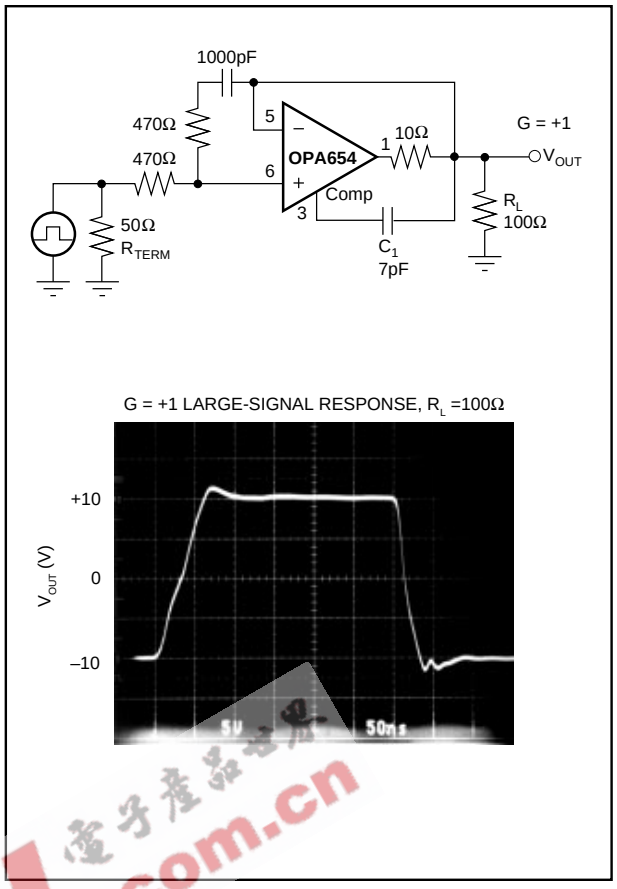


FIGURE 4. G = +1 Amplifier with Alternative Compensation.

The OPA654 may be operated at reduced power supply voltage, thus reducing internal power dissipation. This can eliminate the need for heat sinking in some applications.

OUTPUT CURRENT LIMIT

Output current is limited by internal circuitry to approximately 325mA at 25°C. The limit current decreases with increasing junction temperature as shown in the typical curves. The combination of current limit and thermal limit protects the device from short circuits to ground.

INPUT BIAS CURRENT

The OPA654 is fabricated with Burr-Brown's dielectrically isolated ***Difet*** process, giving it very low input bias current. Like other FET amplifiers, input bias current doubles for every 10°C increase in junction temperature. This increase can be minimized by providing a heat sink and, if possible, operating with reduced power supply voltage to minimize power dissipation.