



OPA177

Precision OPERATIONAL AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 25μV max
- LOW DRIFT: 0.3μV/°C
- HIGH OPEN-LOOP GAIN: 130dB min
- LOW QUIESCENT CURRENT: 1.5mA typ
- REPLACES INDUSTRY-STANDARD OP AMPS: OP-07, OP-77, OP-177, AD707, ETC.

APPLICATIONS

- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER

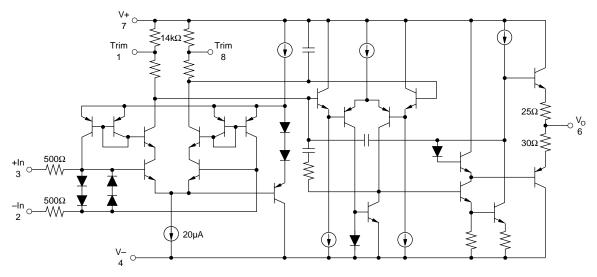
DESCRIPTION

The OPA177 precision bipolar op amp feature very low offset voltage and drift. Laser-trimmed offset, drift and input bias current virtually eliminate the need for costly external trimming. The high performance and low cost make them ideally suited to a wide range of precision instrumentation.

The low quiescent current of the OPA177 dramatically reduce warm-up drift and errors due to thermo-

electric effects in input interconnections. It provides an effective alternative to chopper-stabilized amplifiers. The low noise of the OPA177 maintains accuracy.

OPA177 performance gradeouts are available. Packaging options include 8-pin plastic DIP and SO-8 surface-mount packages.



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OPA177 SPECIFICATIONS

At $V_S = \pm 15V$, $T_A = +25$ °C, unless otherwise noted.

		OPA177F			OPA177G			
PARAMETER	CONDITION	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
OFFSET VOLTAGE Input Offset Voltage Long-Term Input Offset ⁽¹⁾ Voltage Stability Offset Adjustment Range	R _P = 20kΩ		10 0.3 ±3	25		20 0.4 *	60	μV μV/Mo mV
Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	115	125		110	120		dB
INPUT BIAS CURRENT Input Offset Current Input Bias Current			0.3 0.5	1.5 ±2		* *	2.8 ±2.8	nA nA
NOISE Input Noise Voltage Input Noise Current	1Hz to 100Hz ⁽²⁾ 1Hz to 100Hz		85 4.5	150		*	*	nVrms pArms
INPUT IMPEDANCE Input Resistance	Differential Mode ⁽³⁾ Common-Mode	26	45 200		18.5	*		ΜΩ GΩ
INPUT VOLTAGE RANGE Common-Mode Input Range ⁽⁴⁾ Common-Mode Rejection	$V_{CM} = \pm 13V$	±13 130	±14 140		* 115	*		V dB
OPEN-LOOP GAIN Large Signal Voltage Gain	$R_L \ge 2k\Omega$ $V_O = \pm 10V^{(5)}$	5110	12,000		2000	6000		V/mV
Output Voltage Swing Open-Loop Output Resistance	$R_L \ge 10k\Omega$ $R_L \ge 2k\Omega$ $R_L \ge 1k\Omega$	±13.5 ±12.5 ±12	±14 ±13 ±12.5	~苍	* *	* * * *		V V V Ω
FREQUENCY RESPONSE Slew Rate Closed-Loop Bandwidth	$R_L \ge 2k\Omega$ $G = +1$	0.1 0.4	0.3 0.6	COY	* *	*		V/μs MHz
POWER SUPPLY Power Consumption Supply Current	$V_S = \pm 15V$, No Load $V_S = \pm 3V$, No Load $V_S = \pm 15V$, No Load		40 3.5 1.3	60 4.5 2		* * *	* * *	mW mW mA

At $V_S = \pm 15 V$, $-40 ^{\circ} C \le T_A \le +85 ^{\circ} C$, unless otherwise noted.

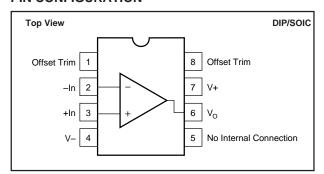
OFFSET VOLTAGE Input Offset Voltage Average Input Offset Voltage Drift Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	110	15 0.1 120	40 0.3	106	20 0.7 115	100 1.2	μV μV/°C dB
INPUT BIAS CURRENT Input Offset Current Average Input Offset Current Drift(6) Input Bias Current Average Input Bias Current Drift(6)			0.5 1.5 0.5 8	2.2 40 ±4 40		* * * 15	4.5 85 ±6 60	nA pA/°C nA pA/°C
INPUT VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection	V _{CM} = ±13V	±13 120	±13.5 140		* 110	*		V dB
OPEN-LOOP GAIN Large Signal Voltage Gain	$R_L \ge 2k\Omega, \ V_O = \pm 10V$	2000	6000		1000	4000		V/mV
OUTPUT Output Voltage Swing	$R_L \ge 2k\Omega$	±12	±13		*	*		V
POWER SUPPLY Power Consumption Supply Current	$V_S = \pm 15V$, No Load $V_S = \pm 15V$, No Load		60 2	75 25		*	*	mW mA

 $[\]ensuremath{\boldsymbol{\ast}}$ Same as specification for product to left.

NOTES: (1) Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically less than $2\mu V$. (2) Sample tested. (3) Guaranteed by design. (4) Guaranteed by CMRR test condition. (5) To insure high open-loop gain throughout the $\pm 10V$ output range, A_{OL} is tested at $-10V \le V_O \le 0V$, $0V \le V_O \le +10V$, and $-10V \le V_O \le +10V$. (6) Guaranteed by end-point limits.



PIN CONFIGURATION



PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	TEMPERATURE RANGE
OPA177FP	8-Pin Plastic DIP	006	-40°C to +85°C
OPA177GP	8-Pin Plastic DIP	006	-40°C to +85°C
OPA177GS	SO-8 Surface-Mount	182	-40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	
Differential Input Voltage	±30V
Input Voltage	±V _S
Output Short Circuit	Continuous
Operating Temperature:	
Plastic DIP (P), SO-8 (S)	40°C to +85°C
θ_{JA} (PDIP)	100°C/W
θ_{JA} (SOIC)	160°C/W
Storage Temperature:	
Plastic DIP (P), SO-8 (S)	65°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s) P packages	+300°C
(soldering, 3s) S package	+260°C



ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. ESD can cause damage ranging from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

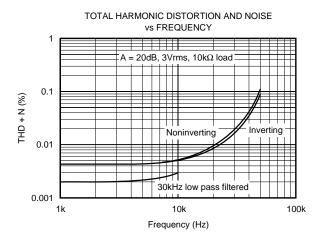
Burr-Brown's standard ESD test method consists of five 1000V positive and negative discharges (100pF in series with $1.5 \mathrm{k}\Omega$) applied to each pin.

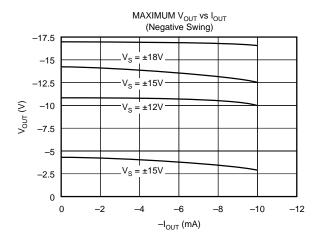
Failure to observe proper handling procedures could result in small changes to the OPA177's input bias current.

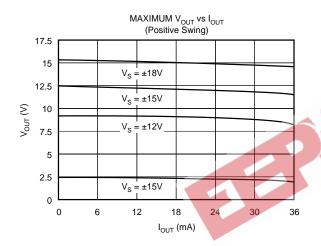
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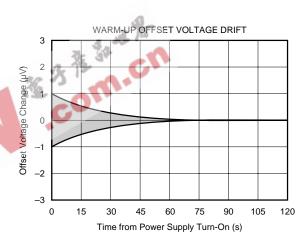
TYPICAL PERFORMANCE CURVES

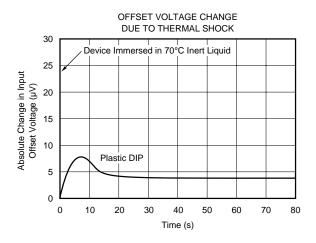
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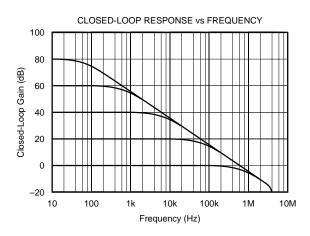








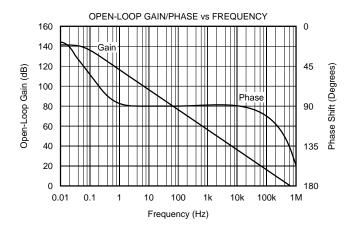


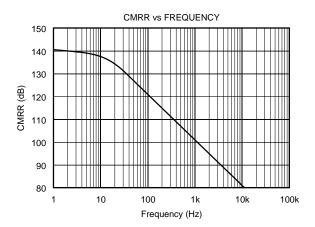


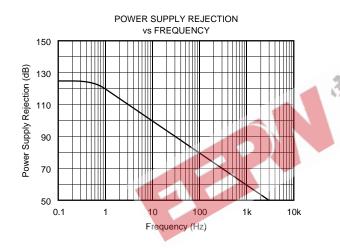


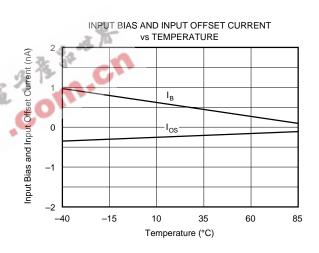
TYPICAL PERFORMANCE CURVES (CONT)

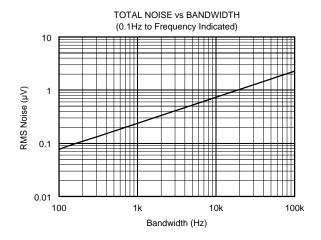
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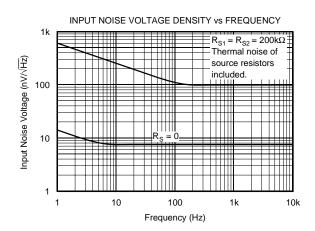






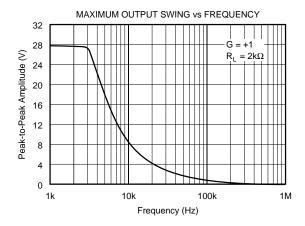


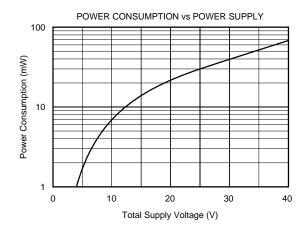


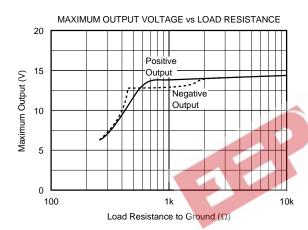


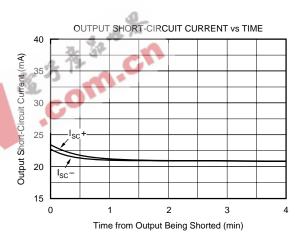
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25$ °C, $V_S = \pm 15$ V, unless otherwise noted.









APPLICATIONS INFORMATION

The OPA177 is unity-gain stable, making it easy to use and free from oscillations in the widest range of circuitry. Applications with noisy or high impedance power supply lines may require decoupling capacitors close to the device pins. In most cases 0.1µF ceramic capacitors are adequate.

The OPA177 has very low offset voltage and drift. To achieve highest performance, circuit layout and mechanical conditions must be optimized. Offset voltage and drift can be degraded by small thermoelectric potentials at the op amp inputs. Connections of dissimilar metals will generate thermal potential which can mask the ultimate performance of the OPA177. These thermal potentials can be made to cancel by assuring that they are equal in both input terminals.

- 1. Keep connections made to the two input terminals close together.
- 2. Locate heat sources as far as possible from the critical input circuitry.
- Shield the op amp and input circuitry from air currents such as cooling fans.

OFFSET VOLTAGE ADJUSTMENT

The OPA177 has been laser-trimmed for low offset voltage and drift so most circuits will not require external adjustment. Figure 1 shows the optional connection of an external potentiometer to adjust offset voltage. This adjustment should not be used to compensate for offsets created elsewhere in a system since this can introduce excessive temperature drift.

INPUT PROTECTION

The inputs of the OPA177 are protected with 500Ω series input resistors and diode clamps as shown in the simplified circuit diagram. The inputs can withstand $\pm 30 \text{V}$ differential inputs without damage. The protection diodes will, of course, conduct current when the inputs are overdriven. This may disturb the slewing behavior of unity-gain follower applications, but will not damage the op amp.

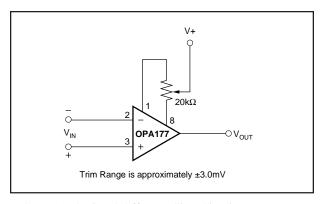


FIGURE 1. Optional Offset Nulling Circuit.

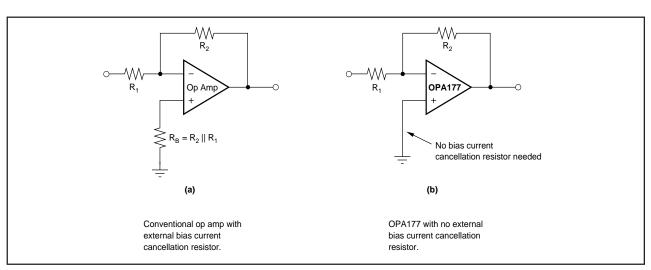
NOISE PERFORMANCE

The noise performance of the OPA177 is optimized for circuit impedances in the range of $2k\Omega$ to $50k\Omega.$ Total noise in an application is a combination of the op amp's input voltage noise and input bias current noise reacting with circuit impedances. For applications with higher source impedance, the OPA627 FET-input op amp will generally provide lower noise. For very low impedance applications, the OPA27 will provide lower noise.

INPUT BIAS CURRENT CANCELLATION

The input stage base current of the OPA177 is internally compensated with an equal and opposite cancellation current. The resulting input bias current is the difference between the input stage base current and the cancellation current. This residual input bias current can be positive or negative.

When the bias current is cancelled in this manner, the input bias current and input offset current are approximately the same magnitude. As a result, it is not necessary to balance the DC resistance seen at the two input terminals (Figure 2). A resistor added to balance the input resistances may actually increase offset and noise.



7

FIGURE 2. Input Bias Current Cancellation.

