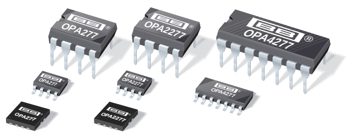
Burr-Brown Products
from Texas Instruments



OPA277
OPA2277
OPA4277

SBOS079A – MARCH 1999 – REVISED APRIL 2005

High Precision
OPERATIONAL AMPLIFIERS

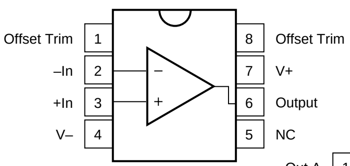
FEATURES

- ULTRA LOW OFFSET VOLTAGE: 10μV
- ULTRA LOW DRIFT: ±0.1μV/°C
- HIGH OPEN-LOOP GAIN: 134dB
- HIGH COMMON-MODE REJECTION: 140dB
- HIGH POWER SUPPLY REJECTION: 130dB
- LOW BIAS CURRENT: 1nA max
- WIDE SUPPLY RANGE: ±2V to ±18V
- LOW QUIESCENT CURRENT: 800μA/amplifier
- SINGLE, DUAL, AND QUAD VERSIONS
- REPLACES OP-07, OP-77, OP-177

APPLICATIONS

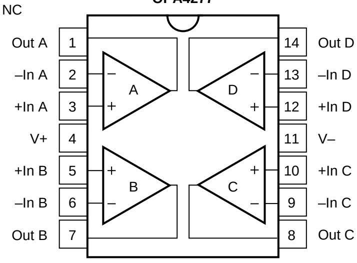
- TRANSDUCER AMPLIFIER
- BRIDGE AMPLIFIER
- TEMPERATURE MEASUREMENTS
- STRAIN GAGE AMPLIFIER
- PRECISION INTEGRATOR
- BATTERY POWERED INSTRUMENTS
- TEST EQUIPMENT

OPA277



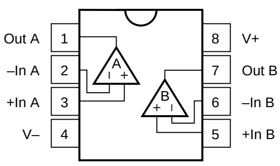
8-Pin DIP, SO-8

OPA4277



14-Pin DIP, SO-14

OPA2277



8-Pin DIP, SO-8

NC = No connection.

DESCRIPTION

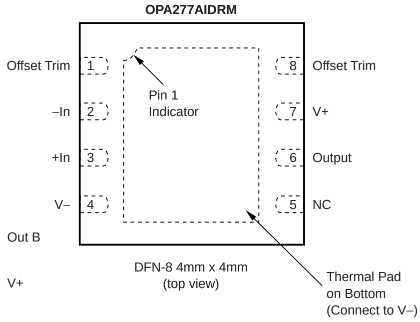
The OPA277 series precision op amps replace the industry standard OP-177. They offer improved noise, wider output voltage swing, and are twice as fast with half the quiescent current. Features include ultra low offset voltage and drift, low bias current, high common-mode rejection, and high power supply rejection. Single, dual, and quad versions have identical specifications for maximum design flexibility.

OPA277 series op amps operate from ±2V to ±18V supplies with excellent performance. Unlike most op amps which are specified at only one supply voltage, the OPA277 series is specified for real-world applications; a single limit applies over the ±5V to ±15V supply range. High performance is maintained as the amplifiers swing to their specified limits. Because the initial offset voltage (±20μV max) is so low, user adjustment is usually not required. However, the single version (OPA277) provides external trim pins for special applications.

OPA277 op amps are easy to use and free from phase inversion and overload problems found in some other op amps. They are stable in unity gain and provide excellent dynamic behavior over a wide range of load conditions. Dual and quad versions feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

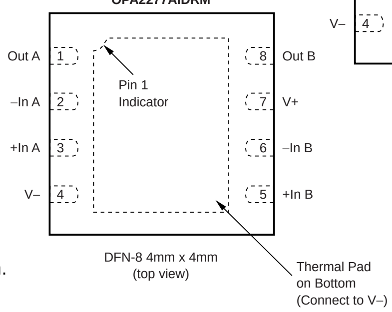
Single (OPA277) and dual (OPA2277) versions are available in DIP-8, SO-8, and DFN-8 (4mm x 4mm) packages. The quad (OPA4277) comes in DIP-14 and SO-14 surface-mount packages. All are fully specified from –40°C to +85°C and operate from –55°C to +125°C.

OPA277AIDRM



DFN-8 4mm x 4mm
(top view)

OPA2277AIDRM



DFN-8 4mm x 4mm
(top view)

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	36V
Input Voltage	(V–) –0.7V to (V+) +0.7V
Output Short-Circuit[2]	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C
ESD Rating (Human Body Model)	2000V
(Machine Model)	100V

NOTE: (1) Stresses above these rating may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Short-circuit to ground, one amplifier per package.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

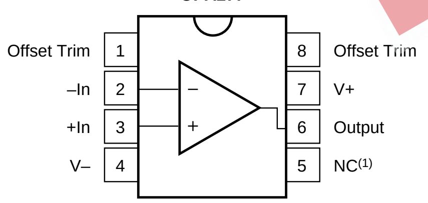
PACKAGE/ORDERING INFORMATION[1]

PRODUCT	OFFSET VOLTAGE max, µV	OFFSET VOLTAGE DRIFT max, µV/°C	PACKAGE-LEAD
Single			
OPA277PA	±50	±1	DIP-8
OPA277P	±20	±0.15	DIP-8
OPA277UA	±50	±1	SO-8 Surface Mount
OPA277U	±20	±0.15	SO-8 Surface Mount
OPA277AIDRM	±100	±1	DFN-8 (4mm x 4mm)
Dual			
OPA2277PA	±50	±1	DIP-8
OPA2277P	±25	±0.25	DIP-8
OPA2277UA	±50	±1	SO-8 Surface Mount
OPA2277U	±25	±0.25	SO-8 Surface Mount
OPA2277AIDRM	±100	±1	DFN-8 (4mm x 4mm)
Quad			
OPA4277PA	±50	±1	DIP-14
OPA4277UA	±50	±1	SO-14 Surface Mount

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet or visit the TI web site at www.ti.com.

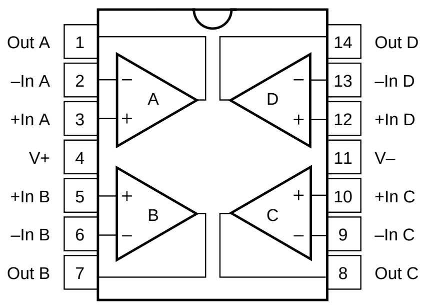
PIN DESCRIPTIONS

OPA277



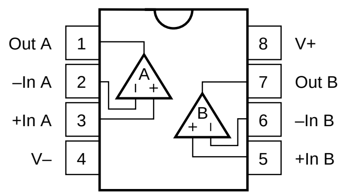
8-Pin DIP, SO-8

OPA4277



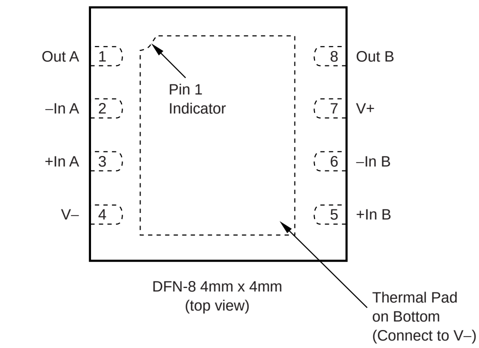
14-Pin DIP, SO-14

OPA2277

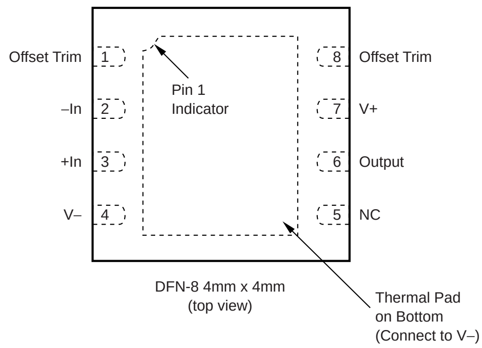


8-Pin DIP, SO-8

OPA2277AIDRM



OPA277AIDRM



NOTE: (1) NC = No connection.

ELECTRICAL CHARACTERISTICS: V_S = ±5V to V_S = ±15V

At T_A = +25°C, and R_L = 2kΩ, unless otherwise noted.
Boldface limits apply over the specified temperature range, –40°C to +85°C.

PARAMETER	CONDITION	OPA277P, U OPA2277P, U			OPA277PA, UA OPA2277PA, UA OPA4277PA, UA			OPA277AIDRM, OPA2277AIDRM			UNITS
		MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
OFFSET VOLTAGE											
Input Offset Voltage: V_{OS}											
OPA277P, U (high grade, single)			±10	±20							μV
OPA2277P, U (high grade, dual)			±10	±25							μV
All PA, UA, Versions						±20	±50				μV
AIDRM Versions									±35	±100	μV
Input Offset Voltage Over Temperature											
OPA277P, U (high grade, single)	**T_A = –40°C to +85°C**			**±30**							**μV**
OPA2277P, U (high grade, dual)	**T_A = –40°C to +85°C**			**±50**							**μV**
All PA, UA, Versions	**T_A = –40°C to +85°C**						**±100**				**μV**
AIDRM Versions	**T_A = –40°C to +85°C**									**±165**	**μV**
Input Offset Voltage Drift dV_{OS}/dT											
OPA277P, U (high grade, single)	**T_A = –40°C to +85°C**		**±0.1**	**±0.15**							**μV/°C**
OPA2277P, U (high grade, dual)	**T_A = –40°C to +85°C**		**±0.1**	**±0.25**							**μV/°C**
All PA, UA, AIDRM Versions	**T_A = –40°C to +85°C**					**±0.15**	**±1**		**±0.15**	**±1**	**μV/°C**
Input Offset Voltage: (all models)											
vs Time			0.2			*			*		μV/mo
vs Power Supply PSRR	V_S = ±2V to ±18V		±0.3	±0.5		*	±1		*	±1	μV/V
T_A = –40°C to +85°C	V_S = ±2V to ±18V			**±0.5**			**±1**			**±1**	μV/V
Channel Separation (dual, quad)	dc		0.1			*			*		μV/V
INPUT BIAS CURRENT											
Input Bias Current I_B			±0.5	±1		*	±2.8			±2.8	nA
T_A = –40°C to +85°C				**±2**			**±4**			**±4**	**nA**
Input Offset Current I_{OS}			±0.5	±1		*	±2.8			±2.8	nA
T_A = –40°C to +85°C				**±2**			**±4**			**±4**	**nA**
NOISE											
Input Voltage Noise, f = 0.1 to 10Hz			0.22			*			*		$μV_{PP}$
			0.035			*			*		μVrms
Input Voltage Noise Density, f = 10Hz e_n			12			*			*		nV/√Hz
f = 100Hz			8			*			*		nV/√Hz
f = 1kHz			8			*			*		nV/√Hz
f = 10kHz			8			*			*		nV/√Hz
Current Noise Density, f = 1kHz i_n			0.2			*			*		pA/√Hz
INPUT VOLTAGE RANGE											
Common-Mode Voltage Range V_{CM}		(V–) +2		(V+) –2	*		*	*		*	V
Common-Mode Rejection CMRR	V_{CM} = (V–) +2V to (V+) –2V	130	140		115	*		115	*		dB
T_A = –40°C to +85°C	V_{CM} = (V–) +2V to (V+) –2V	**128**			**115**			**115**			**dB**
INPUT IMPEDANCE											
Differential			100 || 3			*			*		MΩ || pF
Common-Mode	V_{CM} = (V–) +2V to (V+) –2V		250 || 3			*			*		GΩ || pF
OPEN-LOOP GAIN											
Open-Loop Voltage Gain A_{OL}	V_O = (V–)+0.5V to (V+)–1.2V, R_L = 10kΩ		140			*			*		dB
	V_O = (V–)+1.5V to (V+)–1.5V, R_L = 2kΩ	126	134		*	*		*	*		dB
T_A = –40°C to +85°C	**V_O = (V–)+1.5V to (V+)–1.5V, R_L = 2kΩ**	**126**			*			*			**dB**
FREQUENCY RESPONSE											
Gain-Bandwidth Product GBW			1			*			*		MHz
Slew Rate SR			0.8			*			*		V/μs
Settling Time, 0.1%	V_S = ±15V, G = 1, 10V Step		14			*			*		μs
0.01%	V_S = ±15V, G = 1, 10V Step		16			*			*		μs
Overload Recovery Time	V_{IN} • G = V_S		3			*			*		μs
Total Harmonic Distortion + Noise THD+N	1kHz, G = 1, V_O = 3.5Vrms		0.002			*			*		%

* Specifications same as OPA277P, U.

NOTE: (1) V_S = ±15V.

ELECTRICAL CHARACTERISTICS: $V_S = \pm5V$ to $V_S = \pm15V$ (CONT)

At T_A = +25°C, and R_L = 2kΩ, unless otherwise noted.
Boldface limits apply over the specified temperature range, –40°C to +85°C.

PARAMETER	CONDITION	OPA277P, U OPA2277P, U MIN	TYP(1)	MAX	OPA277PA, UA OPA2277PA, UA OPA4277PA, UA MIN	TYP(1)	MAX	OPA277AIDRM, OPA2277AIDRM MIN	TYP(1)	MAX	UNITS
OUTPUT											
Voltage Output V_O	R_L = 10kΩ	(V–) +0.5		(V+) –1.2	*		*	*		*	V
T_A = –40°C to +85°C	R_L = 10kΩ	**(V–) +0.5**		**(V+) –1.2**	*		*	*		*	**V**
	R_L = 2kΩ	(V–) +1.5		(V+) –1.5	*		*	*		*	V
T_A = –40°C to +85°C	R_L = 2kΩ	**(V–) +1.5**		**(V+) –1.5**	*		*	*		*	**V**
Short-Circuit Current I_{SC}			±35			*			*		mA
Capacitive Load Drive C_{LOAD}			See Typical Curve			*			*		
POWER SUPPLY											
Specified Voltage Range V_S		±5		±15	*		*	*		*	V
Operating Voltage Range		±2		±18	*		*	*		*	V
Quiescent Current (per amplifier) I_Q	I_O = 0		±790	±825		*	*		*	*	μA
T_A = –40°C to +85°C	I_O = 0			**±900**			*			*	**μA**
TEMPERATURE RANGE											
Specified Range		–40		+85	*		*	*		*	°C
Operating Range		–55		+125	*		*	*		*	°C
Storage Range		–55		+125	*		*	*		*	°C
Thermal Resistance θ_{JA}											
SO-8 Surface-Mount			150			*					°C/W
DIP-8			100			*					°C/W
DIP-14			80			*					°C/W
SO-14 Surface-Mount			100			*					°C/W
DFN-8(2)									45		°C/W

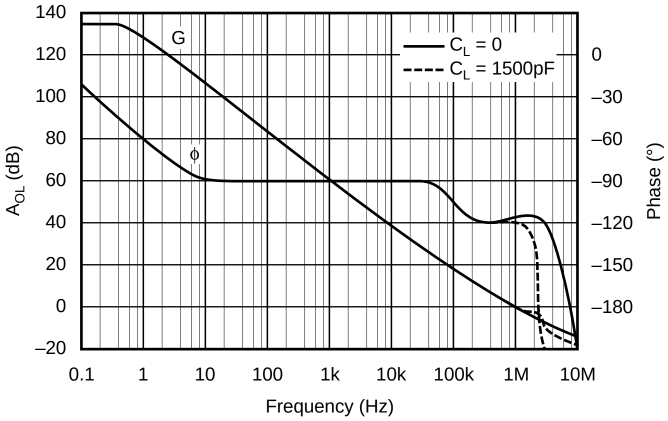
* Specifications same as OPA277P, U.

NOTES: (1) V_S = ±15V.
(2) Thermal pad soldered to printed circuit board (PCB).

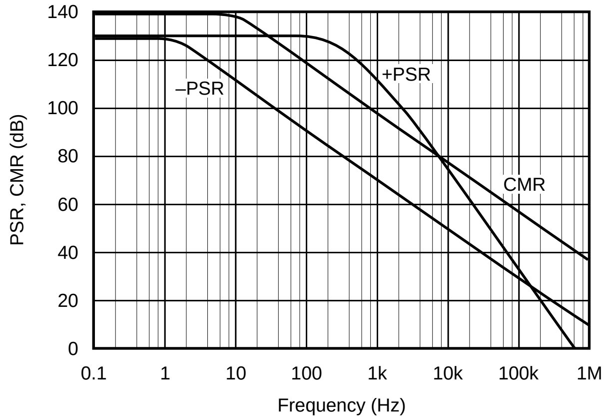
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = ±15V, and R_L = 2kΩ, unless otherwise noted.

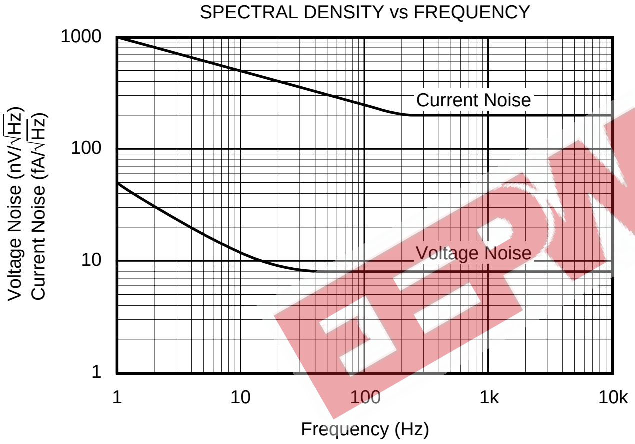
OPEN-LOOP GAIN/PHASE vs FREQUENCY



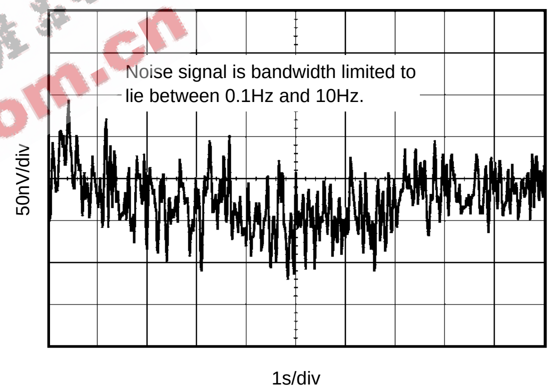
POWER SUPPLY AND COMMON-MODE REJECTION vs FREQUENCY



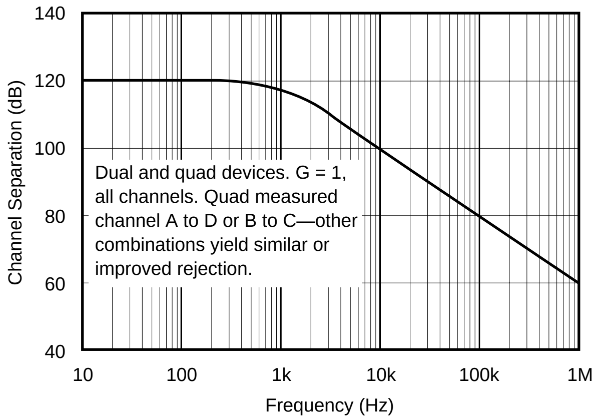
INPUT NOISE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



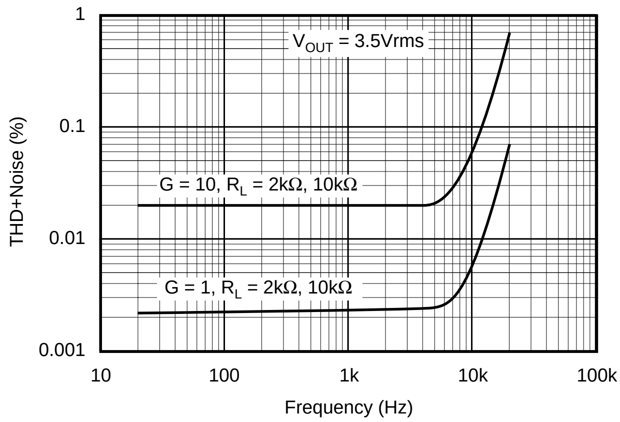
INPUT NOISE VOLTAGE vs TIME



CHANNEL SEPARATION vs FREQUENCY



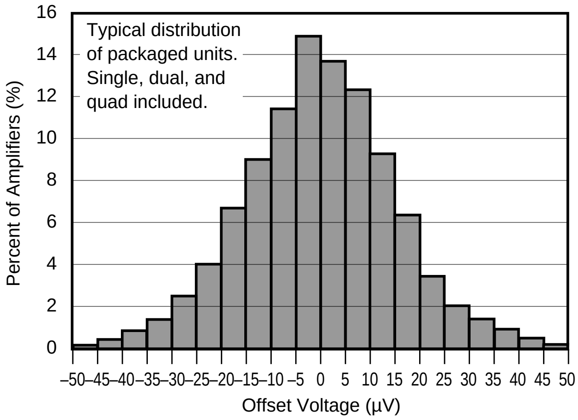
TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



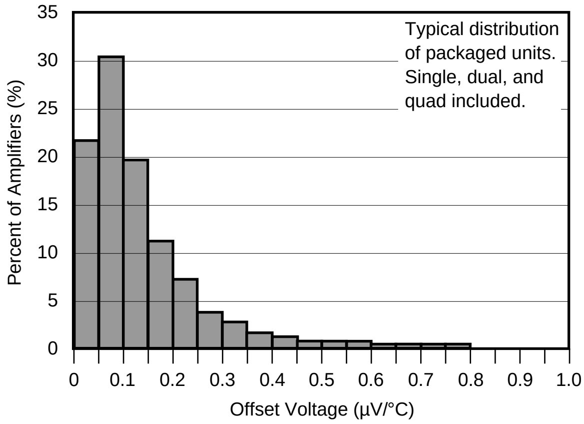
TYPICAL CHARACTERISTICS (CONT)

At $T_A = +25°C$, $V_S = ±15V$, and $R_L = 2kΩ$, unless otherwise noted.

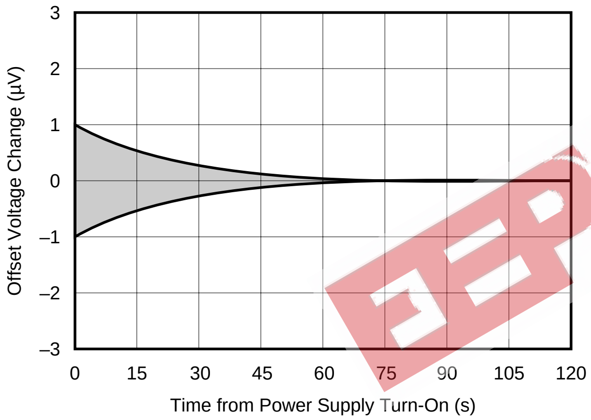
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



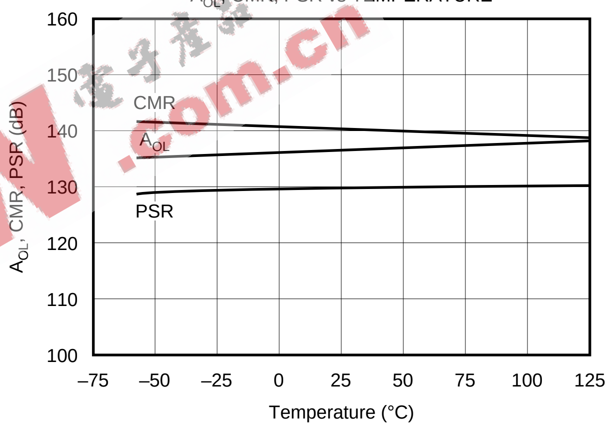
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



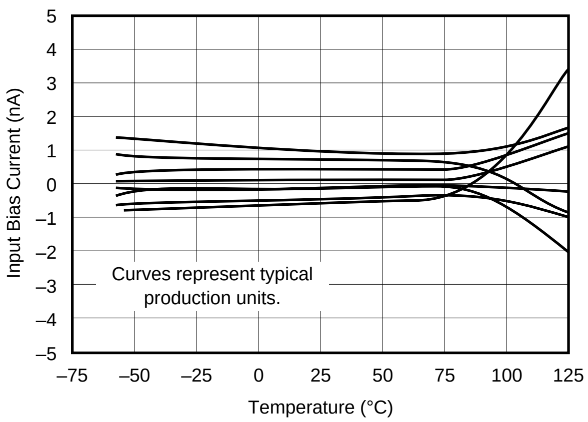
WARM-UP OFFSET VOLTAGE DRIFT



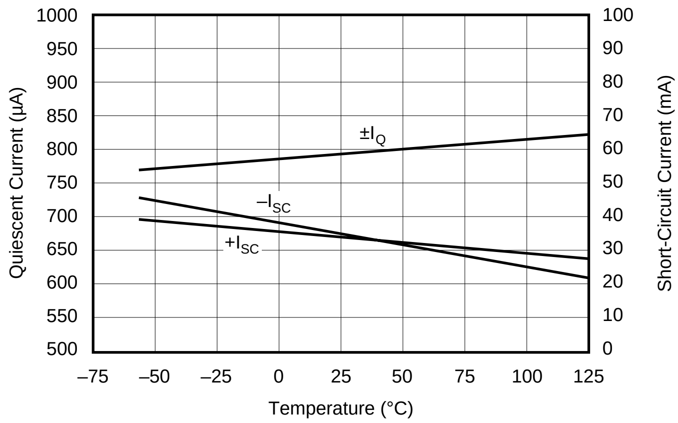
A_{OL}, CMR, PSR vs TEMPERATURE



INPUT BIAS CURRENT vs TEMPERATURE



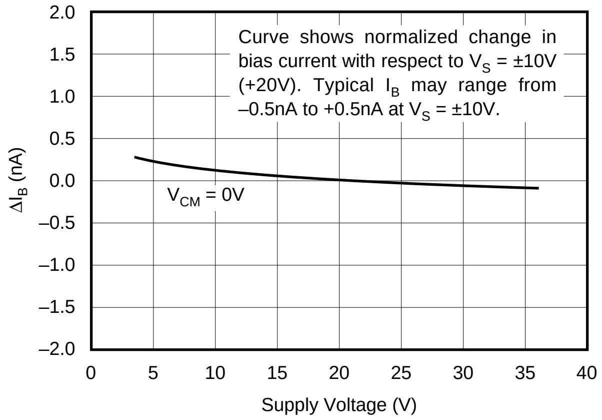
QUIESCENT CURRENT AND SHORT-CIRCUIT CURRENT vs TEMPERATURE



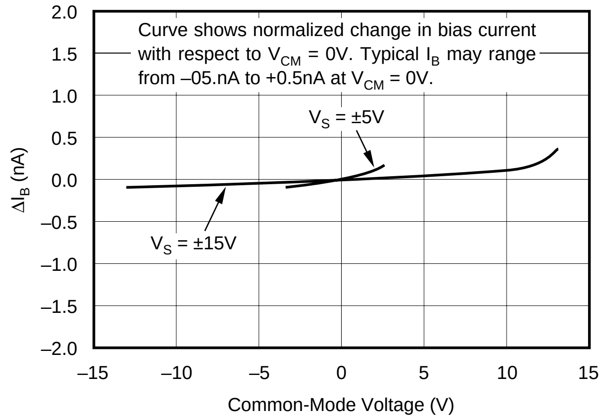
TYPICAL CHARACTERISTICS (CONT)

At $T_A = +25°C$, $V_S = ±15V$, and $R_L = 2kΩ$, unless otherwise noted.

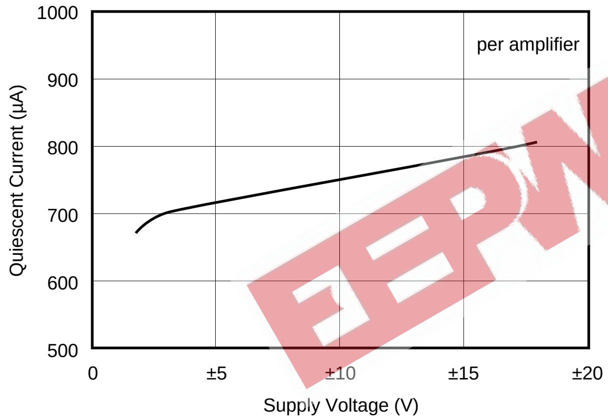
CHANGE IN INPUT BIAS CURRENT vs POWER SUPPLY VOLTAGE



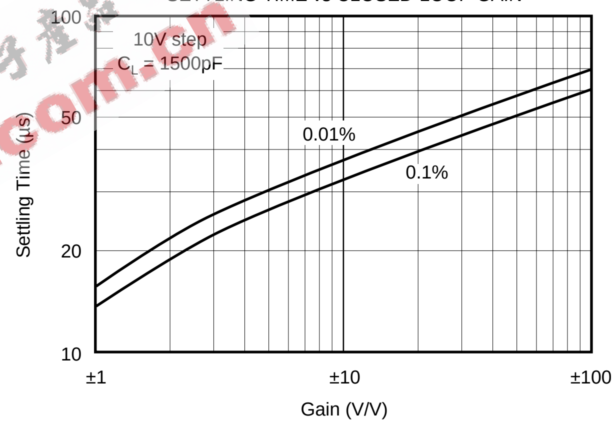
CHANGE IN INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



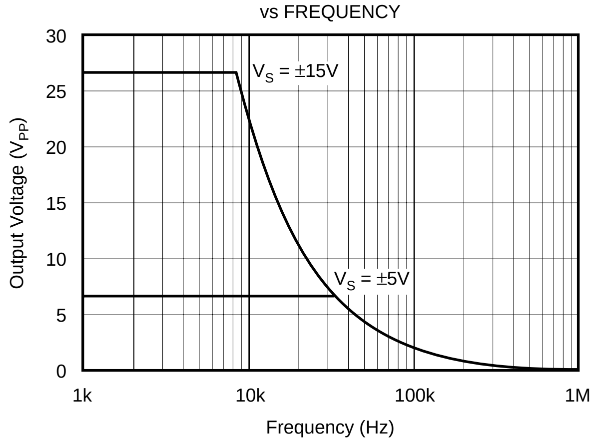
QUIESCENT CURRENT vs SUPPLY VOLTAGE



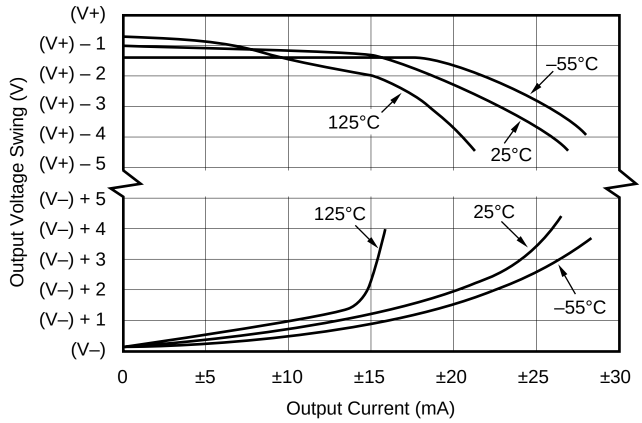
SETTLING TIME vs CLOSED-LOOP GAIN



MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



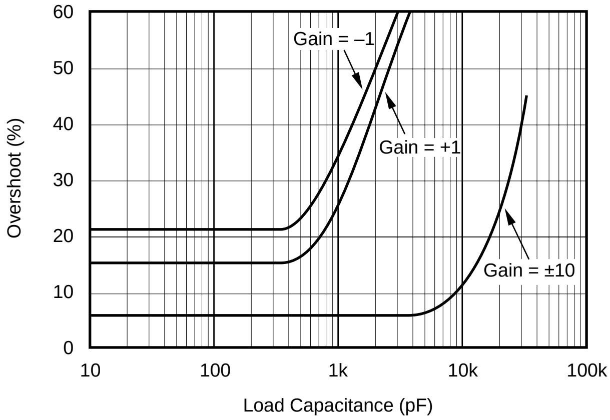
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



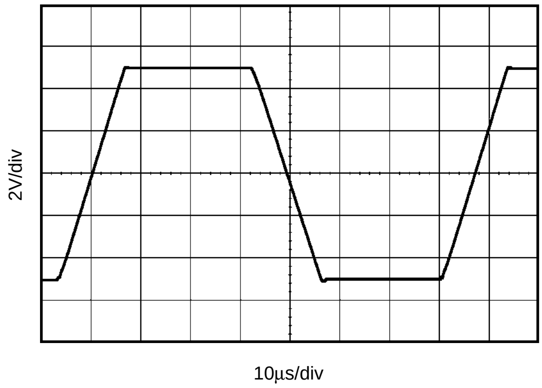
TYPICAL CHARACTERISTICS (CONT)

At $T_A = +25°C$, $V_S = ±15V$, and $R_L = 2kΩ$, unless otherwise noted.

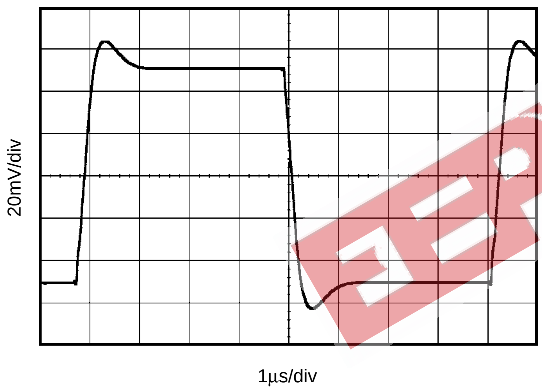
SMALL-SIGNAL OVERSHOOT
vs LOAD CAPACITANCE



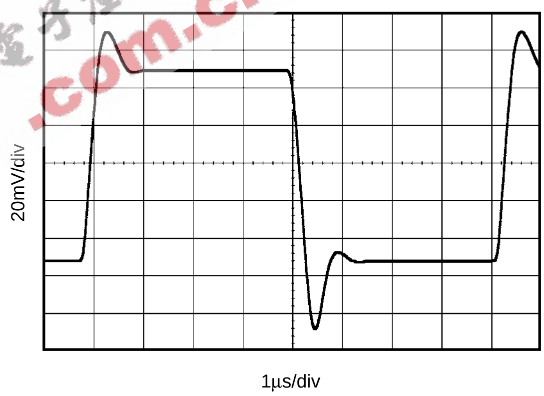
LARGE-SIGNAL STEP RESPONSE
G = +1, CL = 1500pF, V_S = +15V



SMALL-SIGNAL STEP RESPONSE
G = +1, C_L = 0, V_S = ±15V



SMALL-SIGNAL STEP RESPONSE
G = +1, C_L = 1500pF, V_S = ±15V



APPLICATIONS INFORMATION

The OPA277 series is unity-gain stable and free from unexpected output phase reversal, making it easy to use in a wide range of applications. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins. In most cases 0.1µF capacitors are adequate.

The OPA277 series has very low offset voltage and drift. To achieve highest performance, circuit layout and mechanical conditions should be optimized. Offset voltage and drift can be degraded by small thermoelectric potentials at the op amp inputs. Connections of dissimilar metals will generate thermal potential which can degrade the ultimate performance of the OPA277 series. These thermal potentials can be made to cancel by assuring that they are equal in both input terminals.

- Keep thermal mass of the connections made to the two input terminals similar.
- Locate heat sources as far as possible from the critical input circuitry.
- Shield op amp and input circuitry from air currents such as cooling fans.

OPERATING VOLTAGE

OPA277 series op amp operate from ±2V to ±18V supplies with excellent performance. Unlike most op amps which are specified at only one supply voltage, the OPA277 series is specified for real-world applications; a single limit applies over the ±5V to ±15V supply range. This allows a customer operating at V_S = ±10V to have the same assured performance as a customer using ±15V supplies. In addition, key parameters are assured over the specified temperature range, –40°C to +85°C. Most behavior remains unchanged through the full operating voltage range (±2V to ±18V). Parameters which vary significantly with operating voltage or temperature are shown in typical performance curves.

OFFSET VOLTAGE ADJUSTMENT

The OPA277 series is laser-trimmed for very low offset voltage and drift so most circuits will not require external adjustment. However, offset voltage trim connections are provided on pins 1 and 8. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 1. This adjustment should be used only to null the offset of the op amp. This adjustment should not be used to compensate for offsets created elsewhere in a system since this can introduce additional temperature drift.

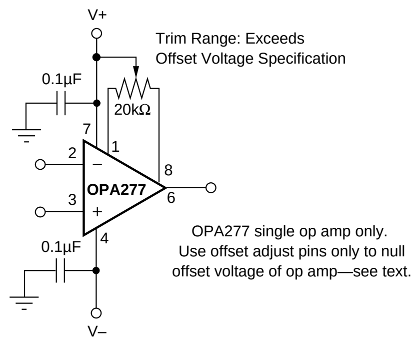


FIGURE 1. OPA277 Offset Voltage Trim Circuit.

INPUT PROTECTION

The inputs of the OPA277 series are protected with 1kΩ series input resistors and diode clamps. The inputs can withstand ±30V differential inputs without damage. The protection diodes will, of course, conduct current when the inputs are over-driven. This may disturb the slewing behavior of unity-gain follower applications, but will not damage the op amp.

INPUT BIAS CURRENT CANCELLATION

The input stage base current of the OPA277 series is internally compensated with an equal and opposite cancellation circuit. The resulting input bias current is the difference between the input stage base current and the cancellation current. This residual input bias current can be positive or negative.

When the bias current is canceled in this manner, the input bias current and input offset current are approximately the same magnitude. As a result, it is not necessary to use a bias current cancellation resistor as is often done with other op amps (Figure 2). A resistor added to cancel input bias current errors may actually increase offset voltage and noise.

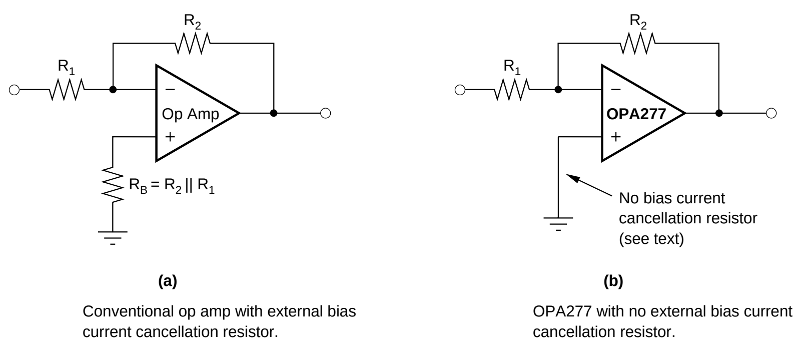


FIGURE 2. Input Bias Current Cancellation.

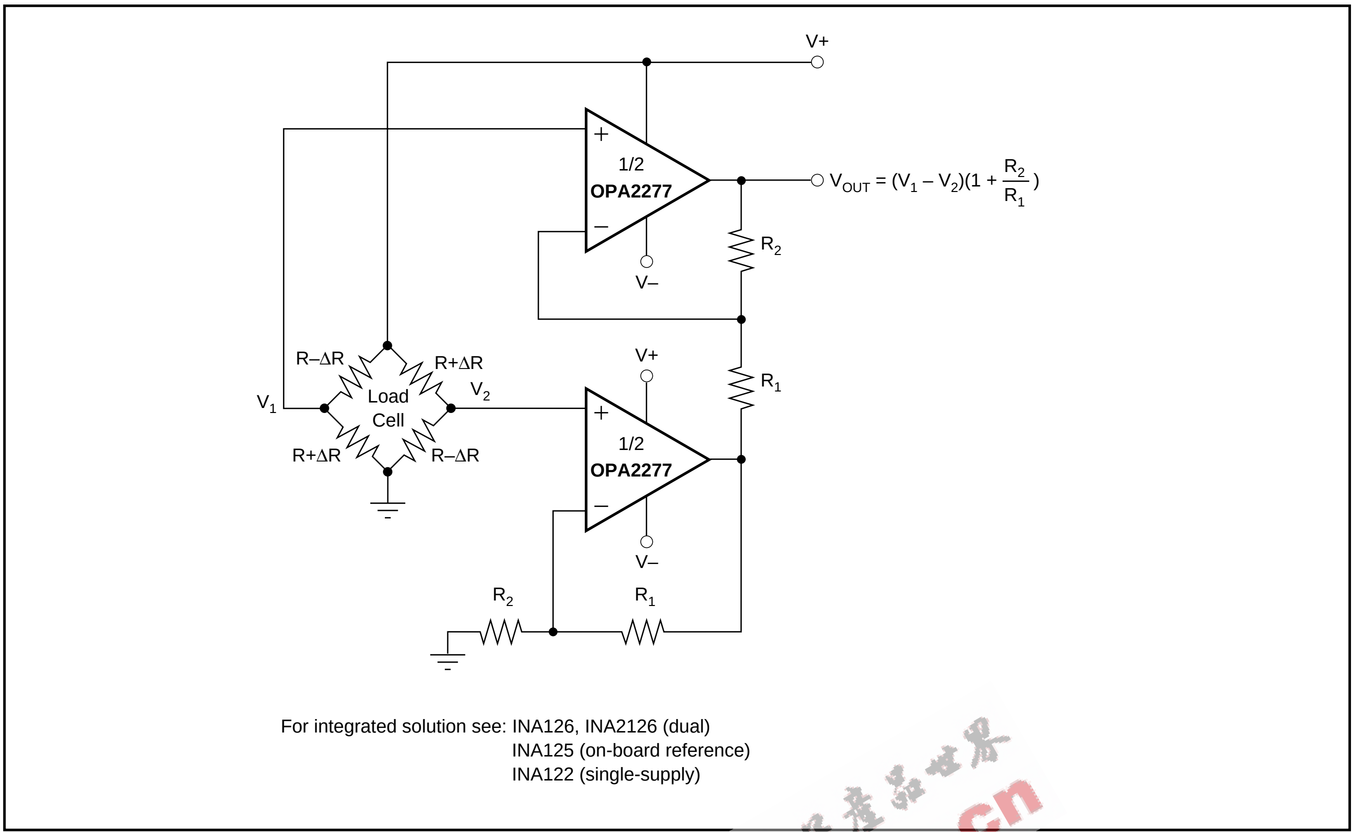


FIGURE 3. Load Cell Amplifier.

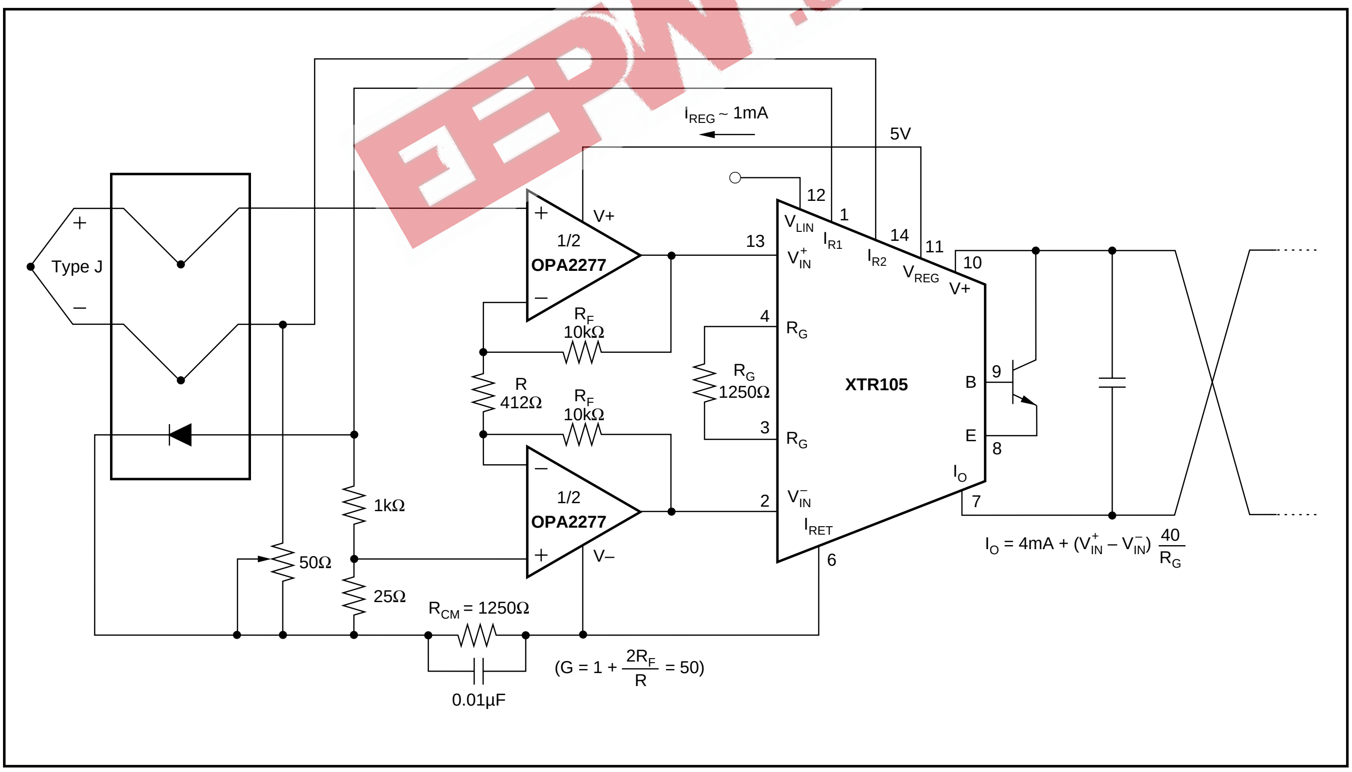


FIGURE 4. Thermocouple Low Offset, Low Drift Loop Measurement with Diode Cold Junction Compensation.

DFN PACKAGE

The OPA277 series uses the 8-lead DFN (also known as SON), which is a QFN package with contacts on only two sides of the package bottom. This leadless, near-chip-scale package maximizes board space and enhances thermal and electrical characteristics through an exposed pad.

DFN packages are physically small, have a smaller routing area, improved thermal performance, and improved electrical parasitics, with a pinout scheme that is consistent with other commonly-used packages, such as SO and MSOP. Additionally, the absence of external leads eliminates bent-lead issues.

The DFN package can be easily mounted using standard printed circuit board (PCB) assembly techniques. See Application Note, *QFN/SON PCB Attachment* (SLUA271) and Application Report, *Quad Flatpack No-Lead Logic Packages* (SCBA017), both available for download at www.ti.com.

The exposed leadframe die pad on the bottom of the package should be connected to V–.

LAYOUT GUIDELINES

The leadframe die pad should be soldered to a thermal pad on the PCB. Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad **must** be soldered to the PCB to provide structural integrity and long-term reliability.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
OPA2277AIDRMR	PREVIEW	SON	DRM	8	3000	TBD	Call TI	Call TI
OPA2277AIDRMRG4	ACTIVE	SON	DRM	8	3000	TBD	Call TI	Call TI
OPA2277AIDRMT	ACTIVE	SON	DRM	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA2277AIDRMTG4	ACTIVE	SON	DRM	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA2277P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2277PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2277PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2277PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2277U	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2277U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2277U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2277UA	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2277UA/2K5	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA2277UA/2K5E4	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA2277UAE4	ACTIVE	SOIC	D	8	100	TBD	Call TI	Call TI
OPA2277UAG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2277UG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA277AIDRMR	ACTIVE	SON	DRM	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA277AIDRMRG4	ACTIVE	SON	DRM	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA277AIDRMT	ACTIVE	SON	DRM	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA277AIDRMTG4	ACTIVE	SON	DRM	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA277P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA277PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA277PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA277PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA277U	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

PACKAGE OPTION ADDENDUM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
OPA277U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA277U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA277UA	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA277UA/2K5	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA277UA/2K5E4	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA277UAE4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA277UAG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA277UG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA4277PA	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA4277PAG4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA4277UA	ACTIVE	SOIC	D	14	58	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA4277UA/2K5	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA4277UA/2K5E4	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA4277UAE4	ACTIVE	SOIC	D	14	58	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA4277UAG4	ACTIVE	SOIC	D	14	58	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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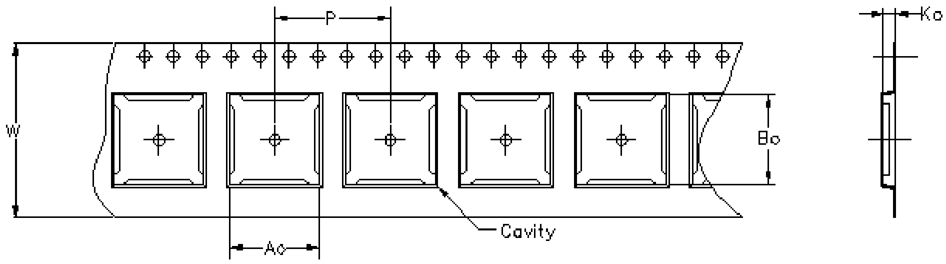
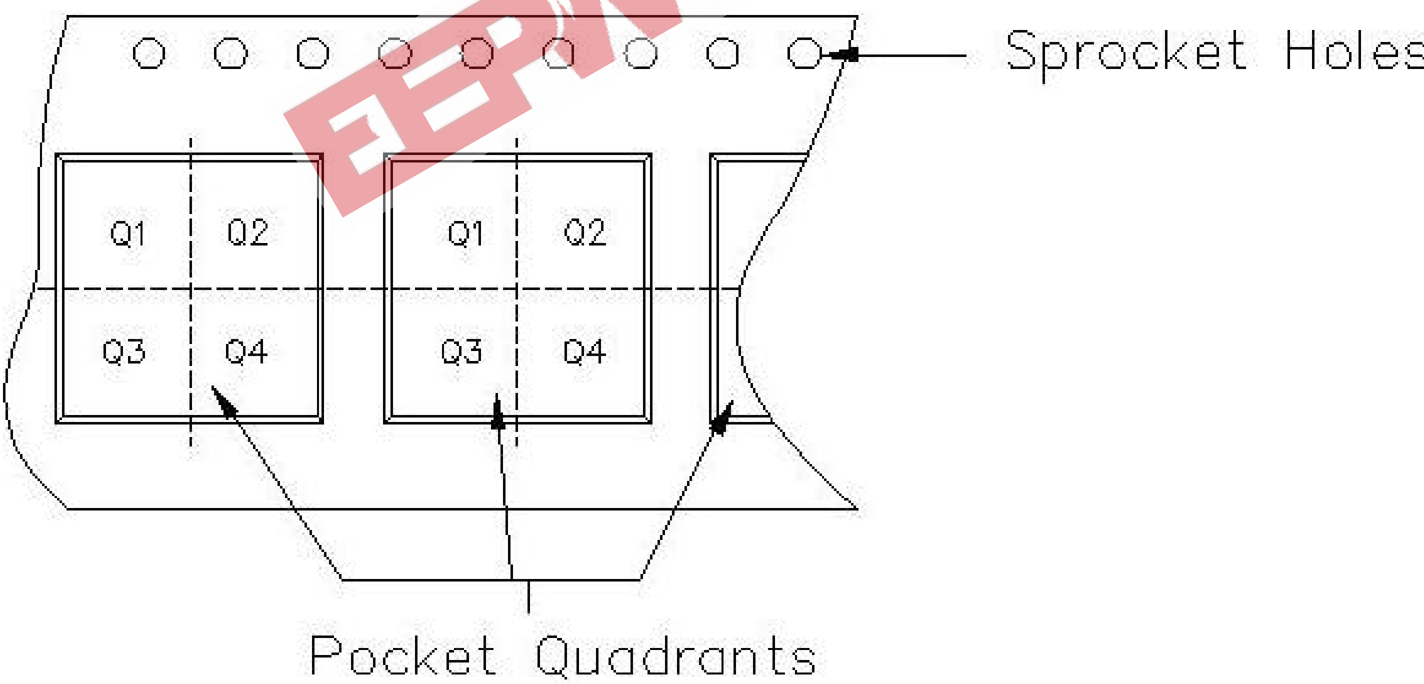


Carrier tape design is defined largely by the component lentgh, width, and thicknes

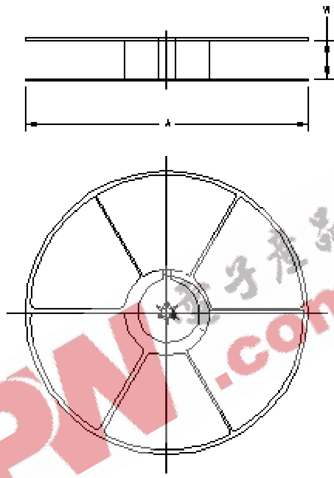
Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



TAPE AND REEL INFORMATION

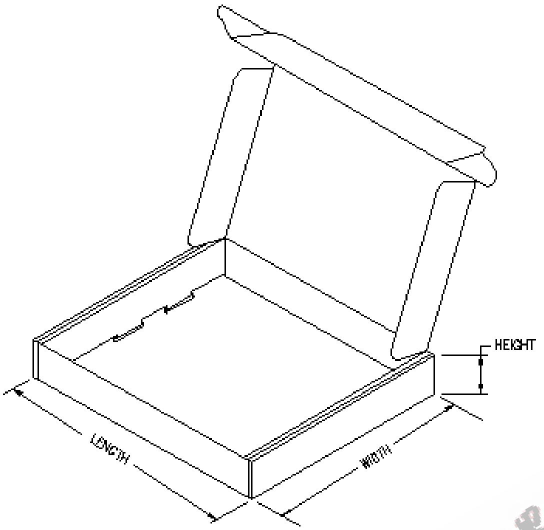
PACKAGE MATERIALS INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2277AIDRMT	DRM	8	MLA	180	12	4.3	4.3	1.5	8	12	Q2
OPA2277UA/2K5	D	8	MLA	330	12	6.9	5.4	2.0	8	12	Q1
OPA277AIDRMR	DRM	8	MLA	330	12	4.3	4.3	1.5	8	12	Q2
OPA277AIDRMT	DRM	8	MLA	180	12	4.3	4.3	1.5	8	12	Q2
OPA277UA/2K5	D	8	MLA	330	12	6.9	5.4	2.0	8	12	Q1
OPA4277UA/2K5	D	14	MLA	330	16	6.5	9.5	2.1	8	16	Q1

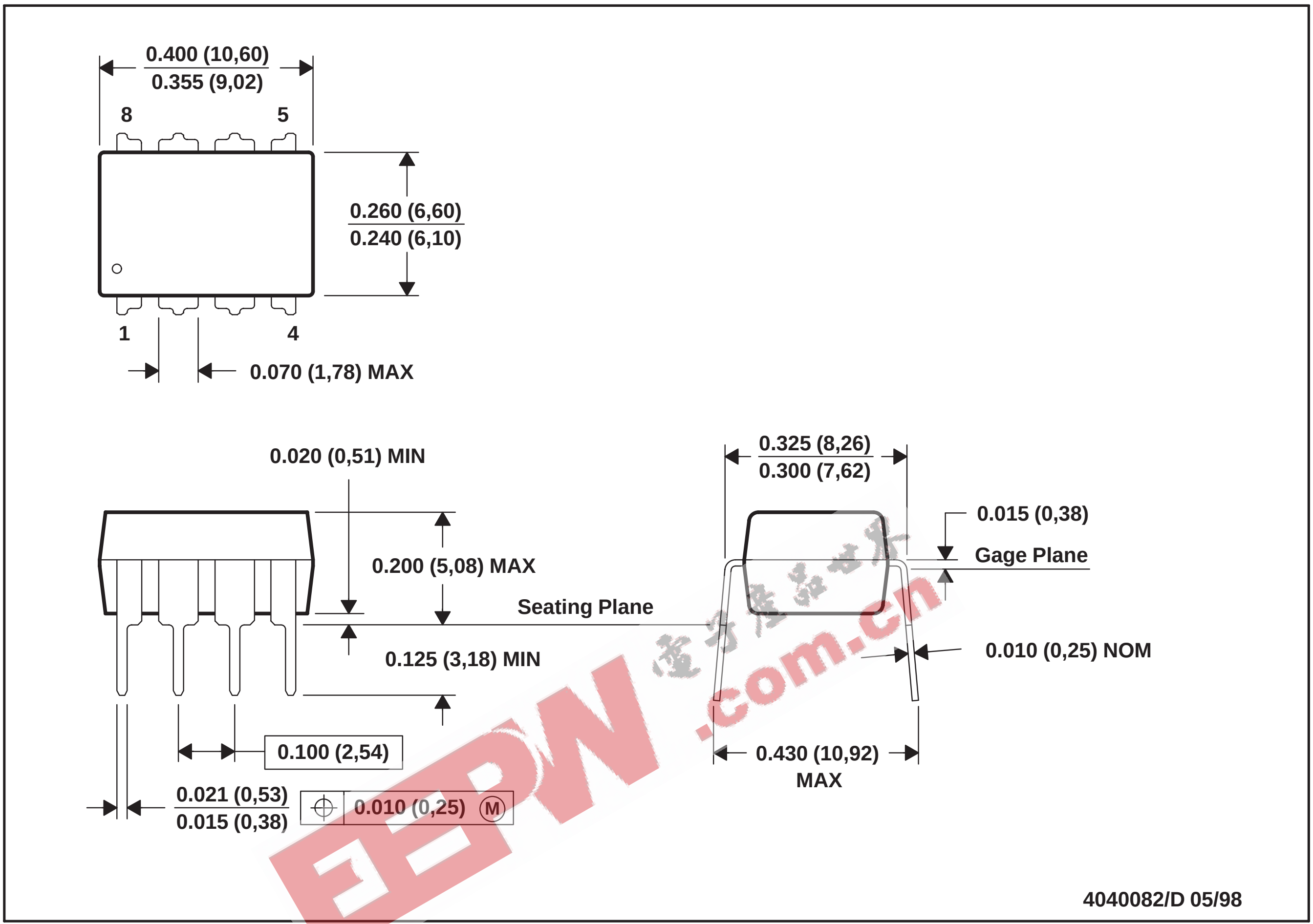


TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
OPA2277AIDRMT	DRM	8	MLA	190.0	212.7	31.75
OPA2277UA/2K5	D	8	MLA	346.0	346.0	29.0
OPA277AIDRMR	DRM	8	MLA	346.0	346.0	29.0
OPA277AIDRMT	DRM	8	MLA	190.0	212.7	31.75
OPA277UA/2K5	D	8	MLA	390.0	348.0	63.0
OPA4277UA/2K5	D	14	MLA	346.0	346.0	33.0


HEIGHT
LENGTH
WIDTH

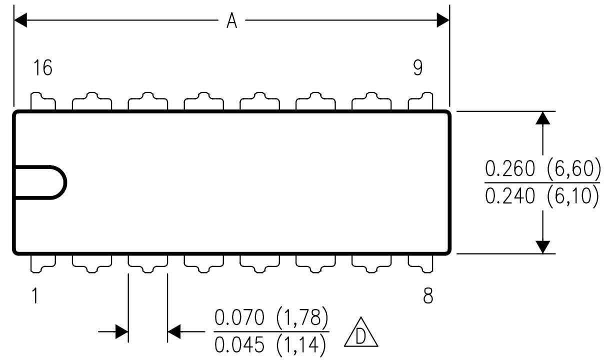
P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



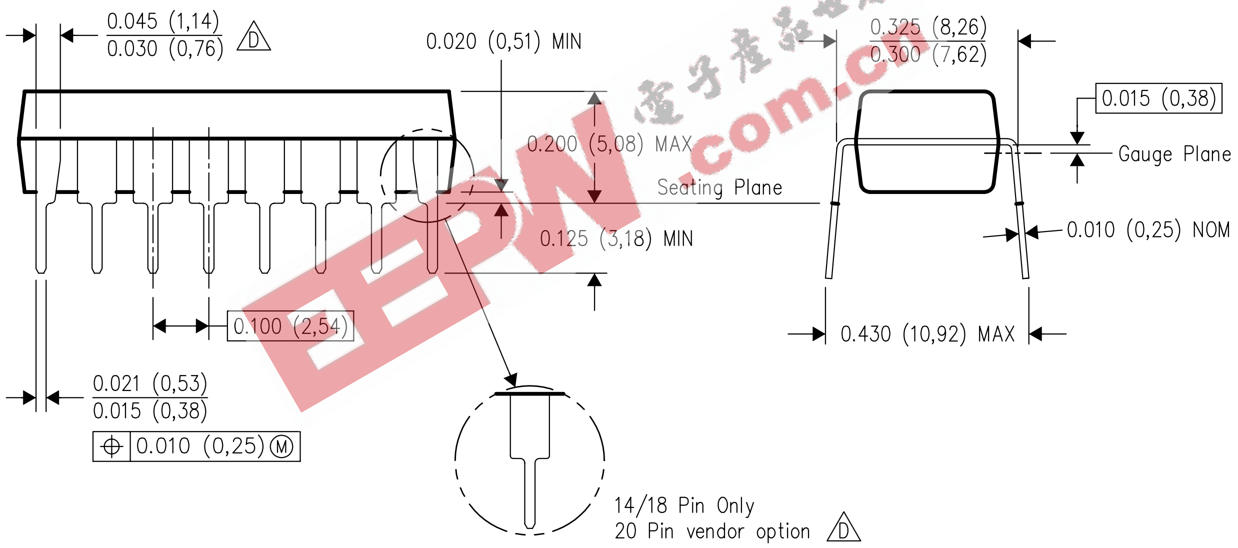
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



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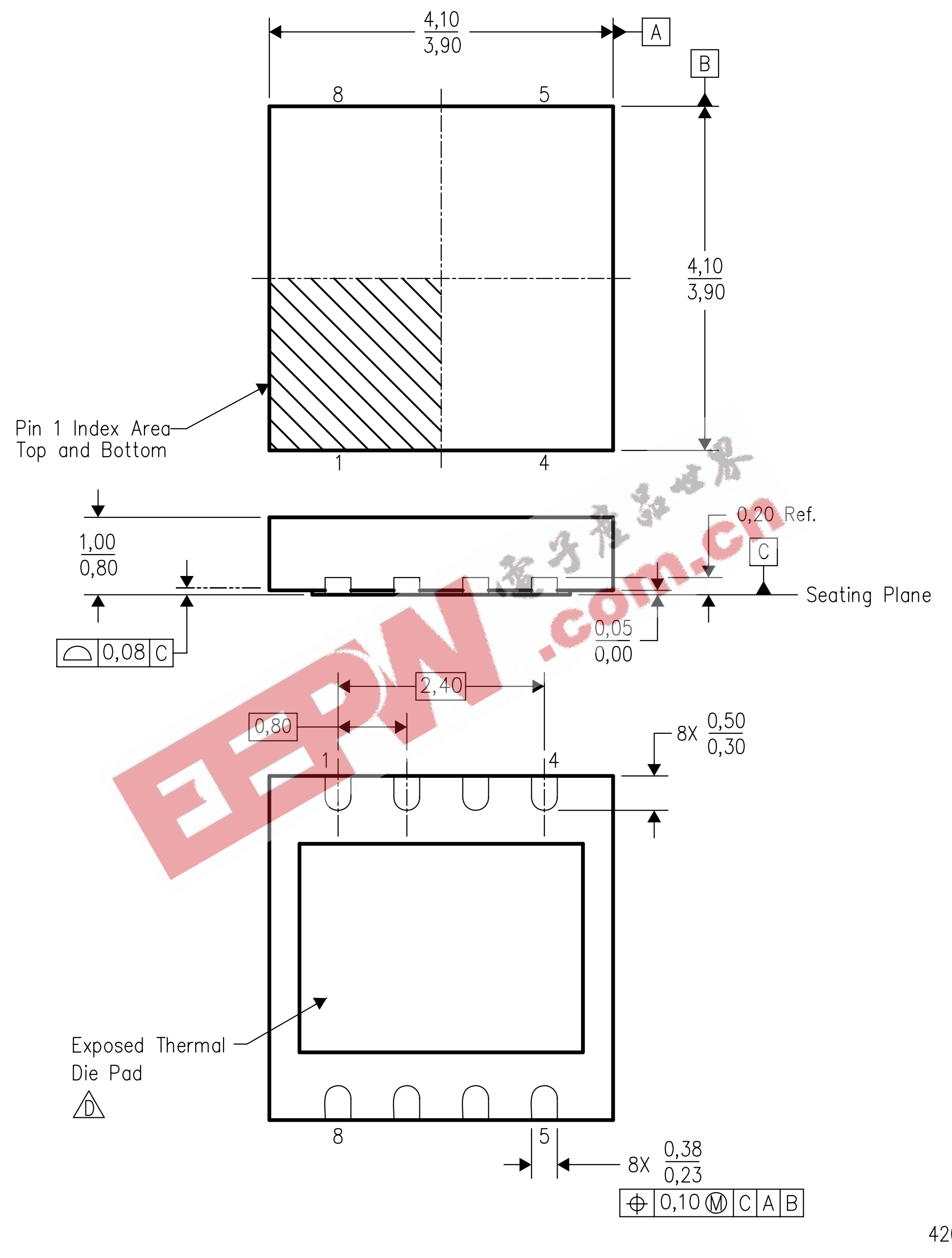
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DRM (S–PDSO–N8) PLASTIC SMALL OUTLINE



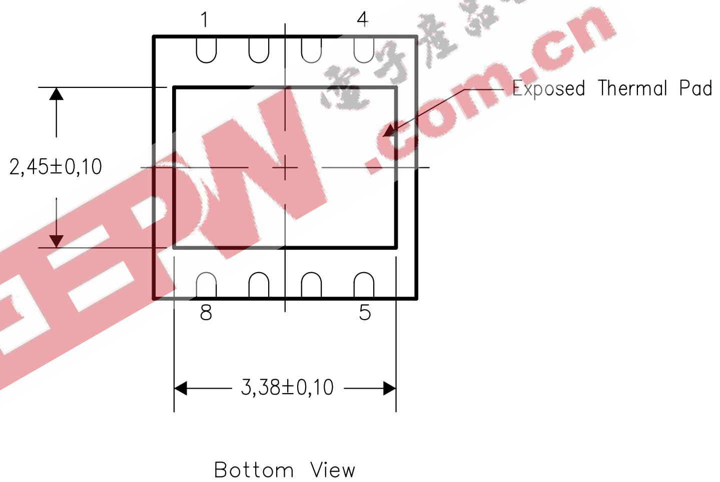
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–229.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

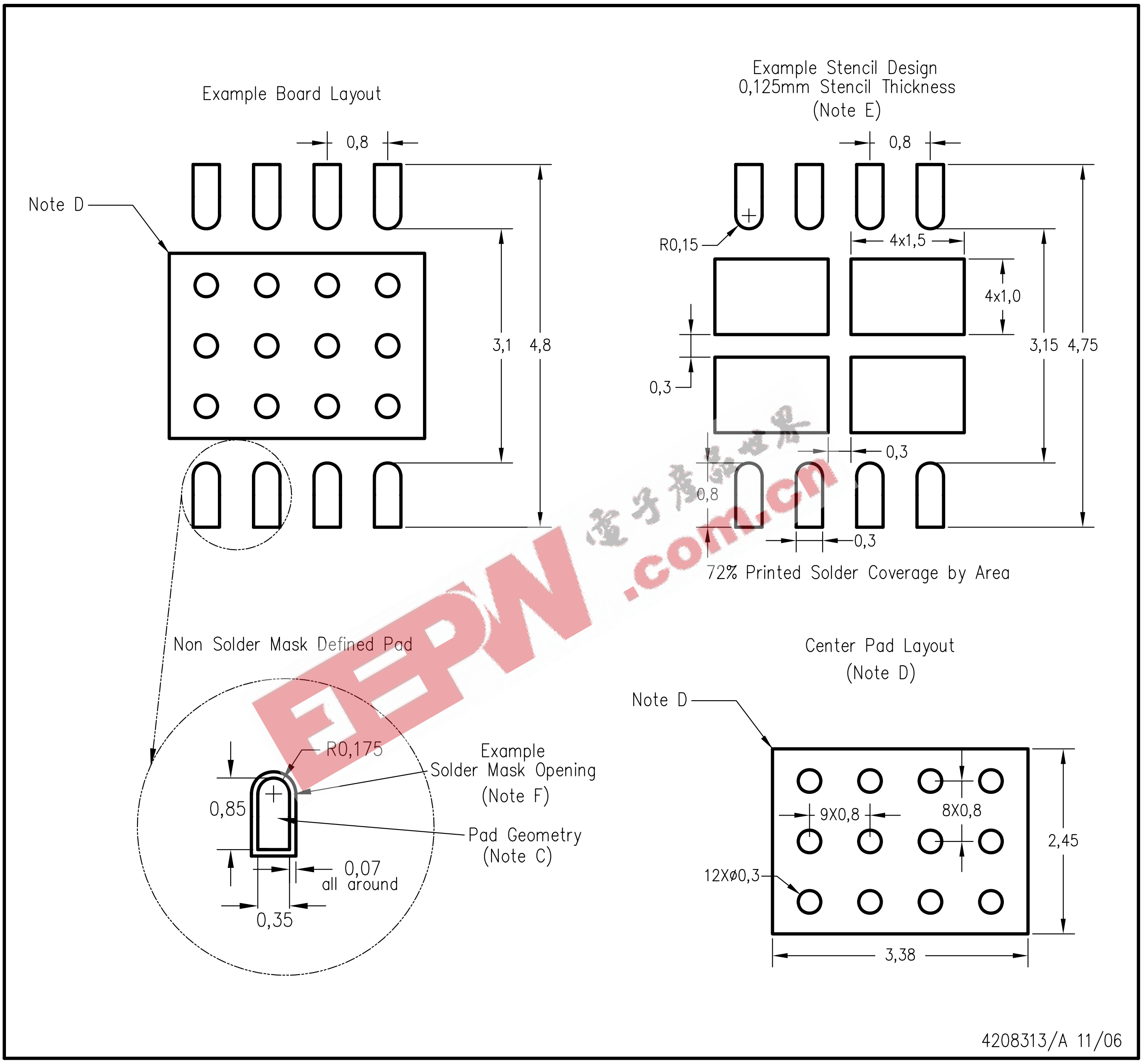
The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

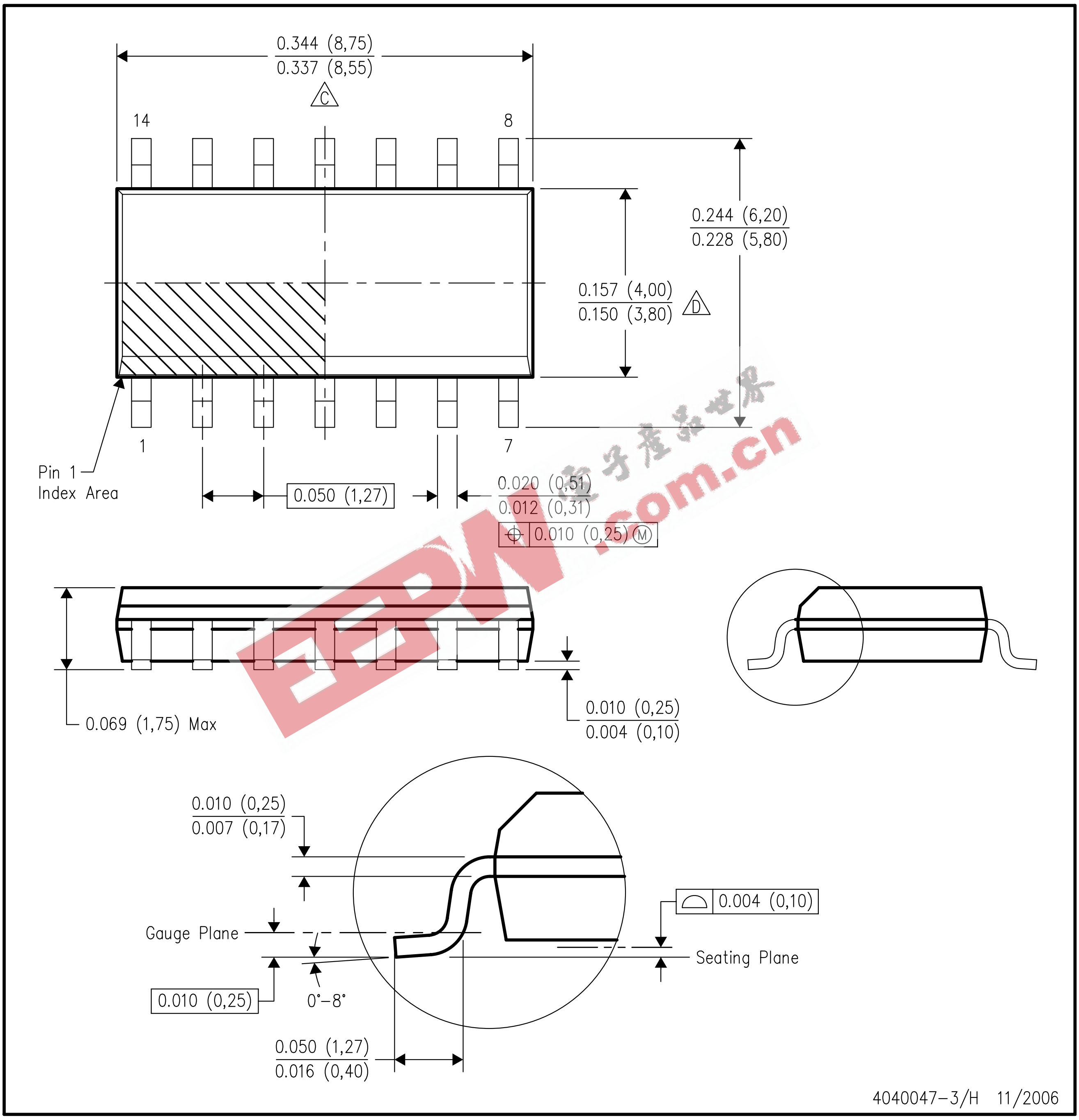
Exposed Thermal Pad Dimensions

DRM (S-PDSO-N8)



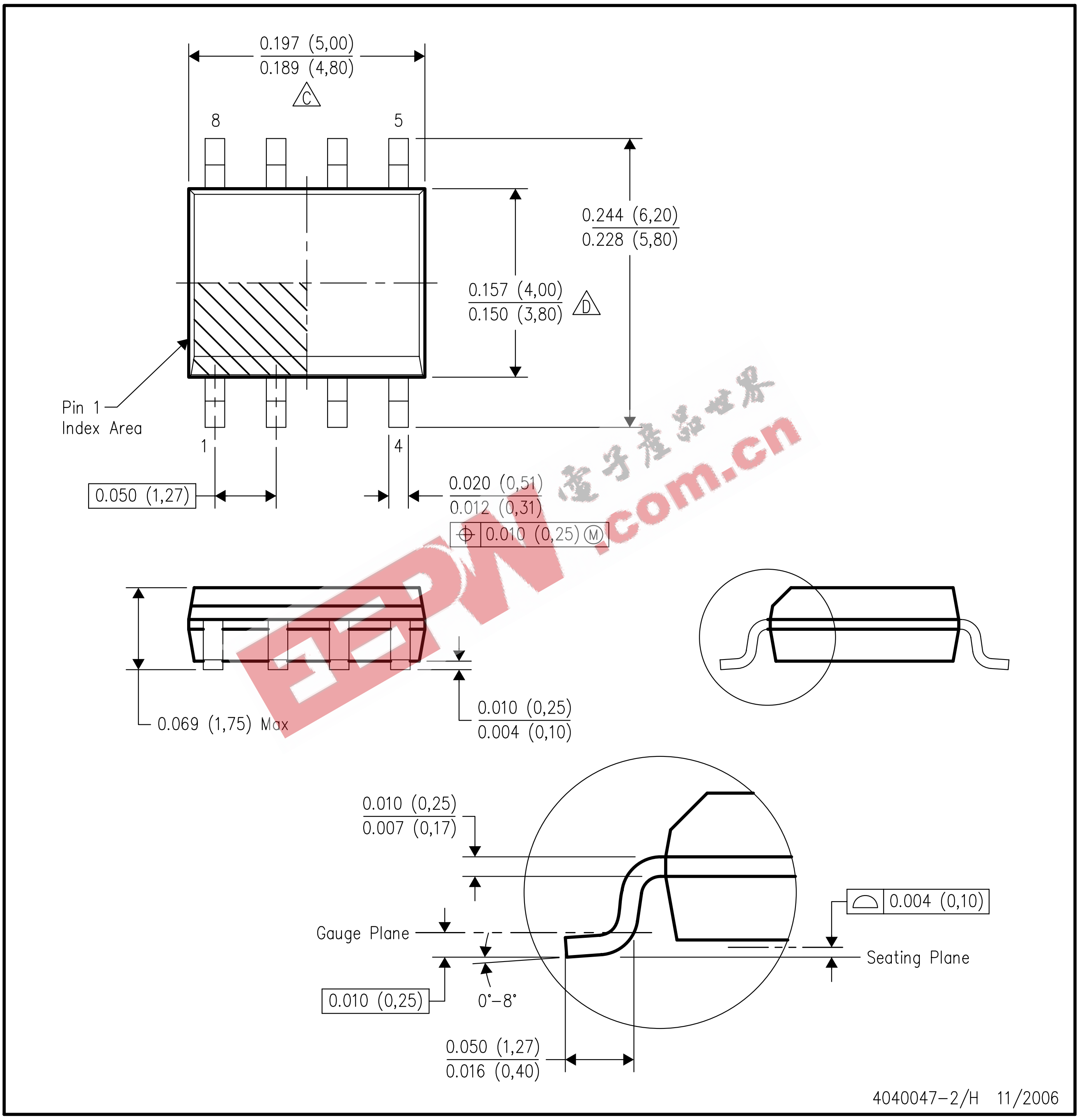
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

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