OZ6833

ACPI CardBus Controller

FEATURES

- Single-chip CardBus host adapter
- Supports 2 PCMCIA 1.0 and JEIDA 4.2 R2 cards or 2 CardBus cards
- ACPI-PCI Bus Power Management Interface Specification Rev1.0 Compliant
- Supports OnNow LAN wakeup, OnNow Ring Indicate, PCI CLKRUN#, PME#, and CardBus CCLKRUN#
- Compliant with PCI specification v2.1S, 1998 PC Card Standard 7.0
- Yenta PCI to PCMCIA CardBus Bridge register compatible
- ExCA (Exchangeable Card Architecture) compatible registers map-able in memory and I/O space
- Intel 82365SL PCIC Register Compatible
- Supports PCMCIA_ATA Specification
- Supports 5V/3.3V PC Cards and 3.3V CardBus cards
- Supports two PC Card or CardBus slots with hot insertion and removal
- Supports multiple FIFOs for PCI/CardBus data transfer
- Supports Direct Memory Access for PC/PCI and PC/Way on PC Card socket
- Programmable interrupt protocol: PCI, PCI+ISA, PCI/Way, or PC/PCI interrupt signaling modes
- Win'98 IRQ and PC-97/98 compliant
- Parallel or Serial interface for socket power control devices (TI or Micrel)
- Zoomed Video Support
- Integrated PC 98 – Subsystem Vendor ID support, with auto lock bit
- LED Activity Pins

ORDERING INFORMATION

OZ6833T – 208 pin TQFP
OZ6833B – 208 pin Mini-BGA

GENERAL DESCRIPTION

The OZ6833 ACPI CardBus controller provides a high performance, synchronous, 32-bit, bus master/target interface between computers and plug in PC Cards. CardBus is the new 32-bit interface standard of Personal Computer Memory Card International Association, PCMCIA. The CardBus provides 32-bit interface with multiplexed address and data lines. This will allow the addition of high performance computer system enhancements and new functions in a user-friendly way. Further, the expansion capability of the CardBus will provide benefits to the end user. CardBus is intended to support "temporal" add-in functions on PC Cards, such as Memory cards, Network interfaces, FAX/Modems and other wireless communication cards, etc. The high performance and capability of the CardBus interface will enable further development of many new functions and applications.

The OZ6833 CardBus controller is a 33MHz PCI compliant master/target device that attaches to the PCI bus and manages two PC Card sockets. The PC Card sockets support both 3.3V / 5V versions of 8/16-bit PCMCIA R2 card or 32-bit CardBus card. R2 card support is compatible with the Intel 82365SL PCIC controller. CardBus card support is fully compatible with the 1998 PC Card Standard V7.0. The OZ6833 is a stand alone device. It does not require an additional buffer chip for the two PC Card socket interface. The OZ6833 is implemented with a complex multiple FIFO data buffer for the PCI and CardBus interface to provide better PCI/CardBus access.

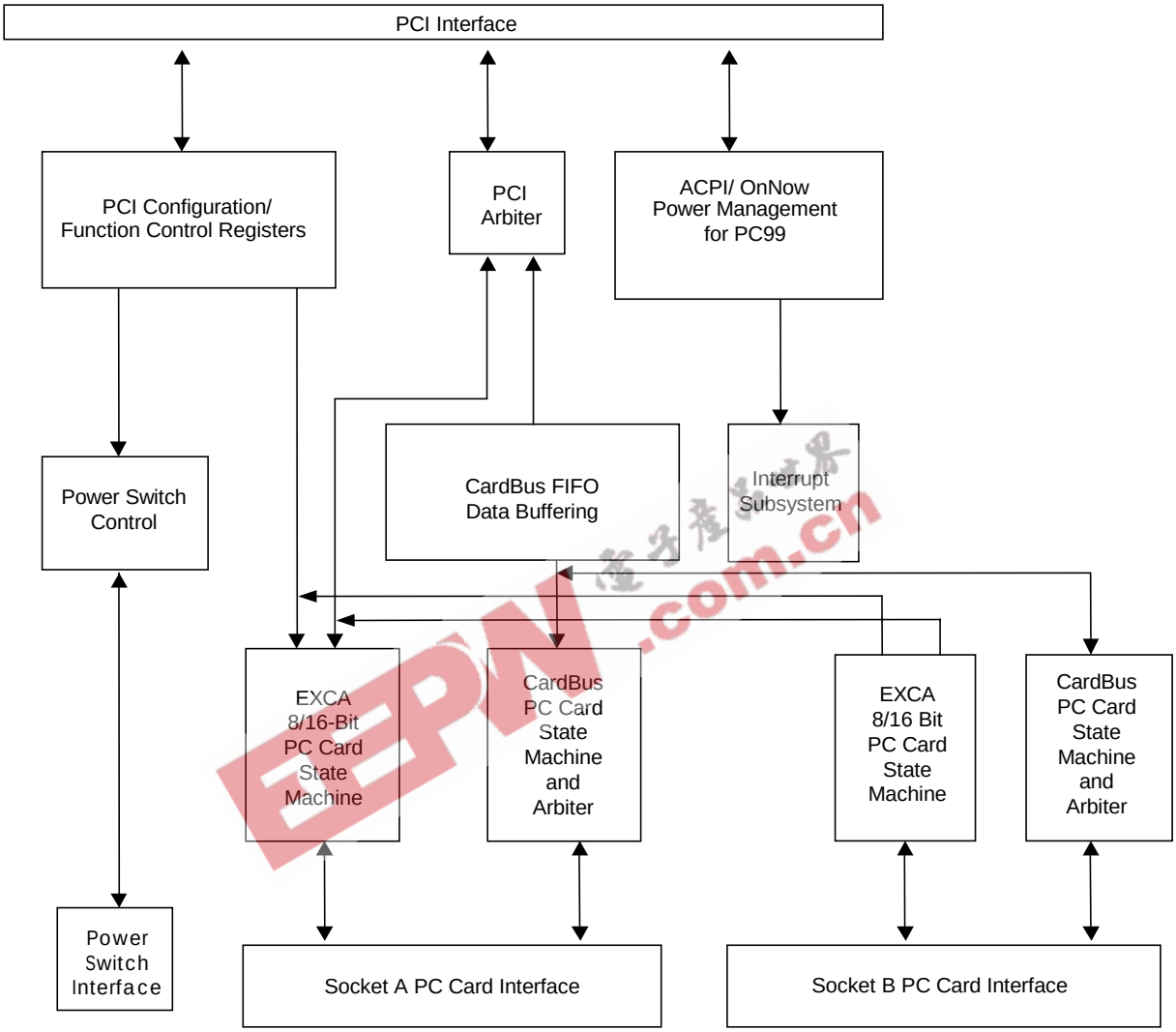
The FIFO buffers allow the bridge to accept data from a target bus while moving data to it, facilitating deadlock prevention. In addition, the OZ6833 is designed with dynamic PC Card hot insertion and removal and auto configuration capabilities.

The OZ6833 ACPI CardBus Controller provides the power saving mixed 5V / 3.3V capability. An advance CMOS process minimizes system power consumption. The device also provides a power-down mode, allowing host software to reduce power consumption further while stopping internal clock distribution and the clocks on PC Card sockets. The OZ6833 is not only a CardBus bridge, but also a socket controller. The OZ6833 supports two master devices and arbitrates the priority of each. Further, it supports inter CardBus direct data transfer. The register set in the OZ6833 is the superset of the OZ67xx register set, assuring full compatibility with existing socket/card-services software and PC-card applications. The OZ6833 provides the most advanced design flexibility for the PC Card interface in notebook computer design.

To enhance the performance between the PCI bus and any CardBus card, two buffers (each composed of 16 double words) are added on both sides going from PCI to CardBus or the other way around. By implementing these buffers, the OZ6833 will not refuse data from a target bus while moving data and preventing deadlock situations.

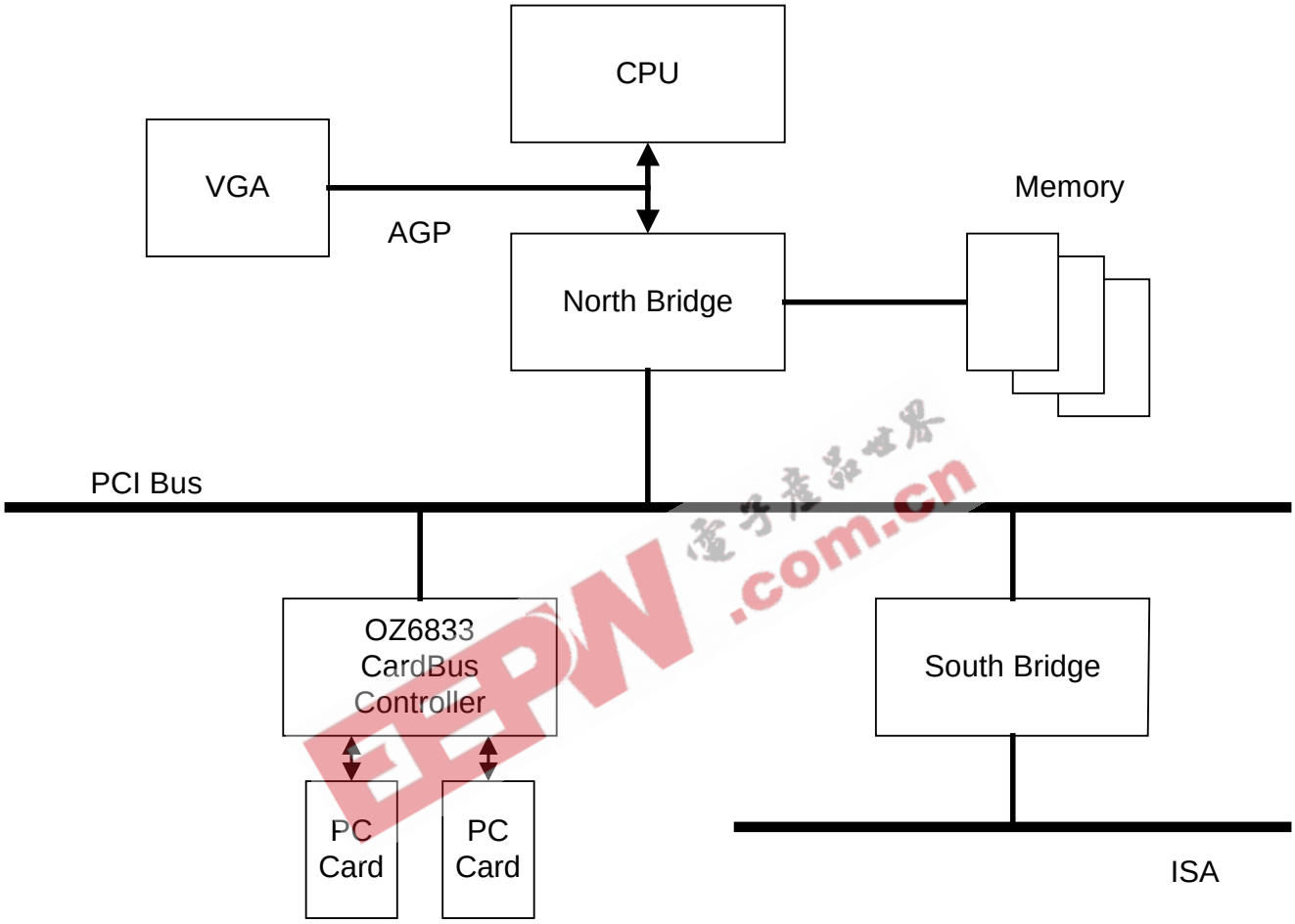
In order to allow maximum flexibility for system designers, the CINT# of the PC card 32-bit may be programmed to steer to either INTA# or INTB# of the PCI bus. Further, the interrupts may be programmed to route through the bridge to either PCI INT lines or IRQ interrupts on the ISA bus.

FUNCTIONAL BLOCK DIAGRAM

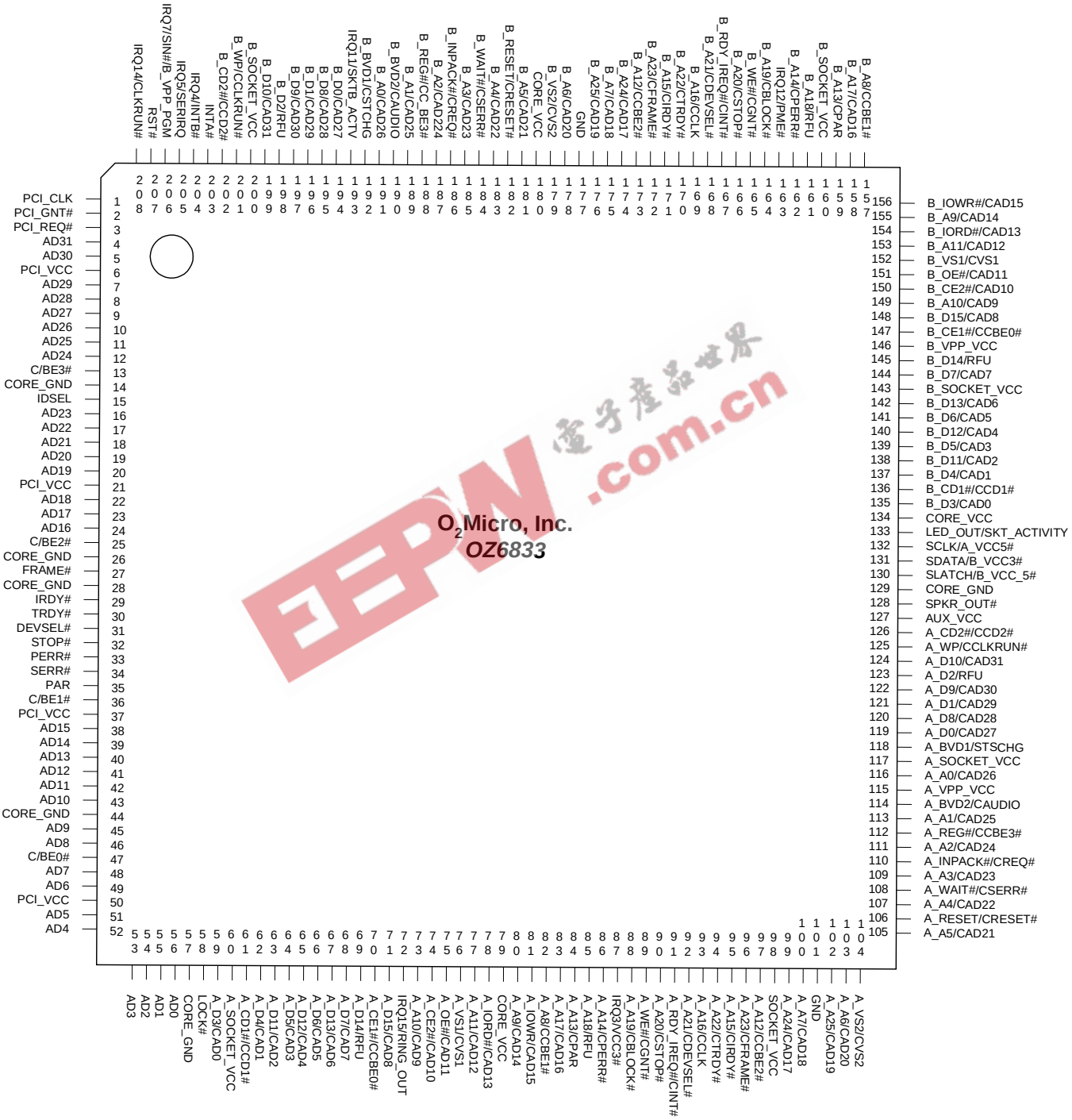


SYSTEM BLOCK DIAGRAM

The following diagram is a typical system block diagram utilizing the OZ6833 ACPI CardBus controller with other related chipsets.



PIN DIAGRAM - 208 PIN TQFP



PIN LIST

Bold Text = Normal Default Pin Name

PCI Bus Interface Pins

Pin Name	Description	Pin Number		Input	Type	Power Rail	Drive
		TQFP	BGA				
AD[31:0]	**PCI Bus Address Input/Data:** These pins connect to PCI bus signals AD[31:0]. A Bus transaction consists of an address phase followed by one or more data phases.	4-5, 7-12, 16-20, 22-24, 38-43, 45-46, 48-49, 51-56	B1, C1, D2, D1, E4, E3, E2, E1, G4, F1, G2, G3, H4, H2, H3, J4, M2, M3, N4, M1, N2, N1, P2, P1, P3, R2, R3, T2, U1, T3, U2, P4	TTL	I/O	4	PCI Spec
C/BE[3:0]#	**PCI Bus Command/Byte Enable:** The command signaling and byte enables are multiplexed on the same pins. During the address phase of a transaction, C/BE[3:0]# are interpreted as the bus commands. During the data phase, C/BE[3:0]# are interpreted as byte enables. The byte enables are to be valid for the entirety of each data phase, and they indicate which bytes in the 32-bit data path are to carry meaningful data for the current data phase.	13, 25, 36, 47	F4, H1, M4, R1	TTL	I/O	4	-
FRAME#	**Cycle Frame:** This input indicates to the OZ6833 that a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is de-asserted, the transaction is in its final phases.	27	J3	TTL	I/O	4	-
IRDY#	**Initiator Ready:** This input indicates the initiating agent's ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#.	29	J1	TTL	I/O	4	-
TRDY#	**Target Ready:** This output indicates target Agent's the OZ6833's ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#.	30	K2	TTL	I/O	4	PCI Spec
STOP#	**Stop:** This output indicates the current target is requesting the master to stop the current transaction.	32	L4	TTL	I/O	4	PCI Spec
IDSEL	**Initialization Device Select:** This input is used as a chip select during configuration read and write transactions. This is a point-to-point signal. IDSEL can be used as a chip select during configuration read and write transactions.	15	F3	TTL	I	4	-
DEVSEL#	**Device Select:** This output is driven active LOW when the PCI address is recognized as supported, thereby acting as the target for the current PCI cycle. The Target must respond before timeout occurs or the cycle will terminate.	31	K3	TTL	I/O	4	PCI Spec
PERR#	**Parity Error:** The output is driven active LOW when a data parity error is detected during a write phase.	33	K1	-	TO	4	PCI Spec

Pin Name	Description	Pin Number		Input	Type	Power Rail	Drive
		TQFP	BGA				
SERR#	**System Error:** This output is driven active LOW to indicate an address parity error.	34	L2	-	TO	4	PCI Spec
PAR	**Parity:** This pin generates PCI parity and ensures even parity across AD[31:0] and C/BE[3:0]#. During the address phase, PAR is valid after one clock. With data phases, PAR is stable one clock after a write or read transaction.	35	L3	TTL	I/O	4	PCI Spec
PCI_CLK	**PCI Clock:** This input provides timing for all transactions on the PCI bus to and from the OZ6833. All PCI bus signals, except RST#, are sampled and driven on the rising edge of PCI_CLK. This input can be operated at frequencies from 0 to 33MHz.	1	A1	TTL	I	4	-
RST#	**Device Reset**: This input is used to initialize all registers and internal logic to their reset states and place most OZ6833 pins in a HIGH-impedance state.	207	C3	TTL	I	1	-
RI_OUT	**Ring Indicate Out**: This pin is Ring Indicate when the following occurs while O_2 Mode Control B Register (index 2Eh) bit 7 is set to 1: 1) Power Control (Index+02h) bit 7 set to 1 2) Interrupt and General Control (Index+03h) bit 7 set to 1 3) PCI O_2Micro Control 2 (Offset: D4h) bit X = 0	72	P8	-	TO	1	4mA
CLKRUN#	**PCI Clock Run Request:** This signal is used by the central resource to request permission to stop the PCI clock or to slow it down, and the OZ6833 responds accordingly. To enable the CLKRUN# signal, you need to enable ExCA register 3B bit[3:2].	208	B2	TTL	I/O	4	PCI Spec
PME#	**Power Management Event:** A power management event is the process by which the OZ6833 can request a change of its power consumption state. Usually, a PME occurs during a request to change from a power saving state to the fully operational state.	163	D13	-	TO	5	4mA
SKTB_ACTV	**Socket B Activity:** This signal indicates that there is any activity on the socket B read/write access. Refer to PCI Configuration Register 90h.	193	A7	-	TO	1	4mA
INTA#	**PCI Bus Interrupt A:** This output indicates a programmable interrupt request generated from any of a number of card actions. Although there is no specific mapping requirement for connecting interrupt lines from the OZ6833 to the system, a common use is to connect this pin to the system PCI bus INTA# signal.	203	A3	-	TO	4	PCI Spec

Pin Name	Description	Pin Number		Input	Type	Power Rail	Drive
		TQFP	BGA				
INTB#	**PCI Bus Interrupt B:** This output indicates a programmable interrupt request generated from any of a number of card actions. Although there is no specific mapping requirement for connecting interrupt lines from the OZ6833 to the system, a common use is to connect this pin to the system PCI bus INTB# signal.	204	C4	-	TO	4	PCI Spec
SOUT#/ IRQSER	**SOUT#/IRQSER:** In PC/PCI Serial Interrupt Signaling mode, this pin is the serial interrupt output, SOUT#. In PC/Way mode, this pin is the IRQ serializer pin to the interrupt controller.	205	B3	TTL	I/O	4	PCI Spec
SIN#	**SIN#:** In PC/PCI Serial Input Signaling mode, this pin is the serial interrupt input, SIN#.	206	A2	TTL	I/O	4	PCI Spec
GNT#	**Grant:** This signal indicates that access to the bus has been granted.	2	D4	TTL	I	4	PCI Spec
REQ#	**Request:** This signal indicates to the arbiter that the OZ6833 requests use of the bus.	3	C2	N/A	TO	4	PCI Spec
LOCK#	**PCI LOCK#:** This signal is used by a PCI master to perform a locked transaction to a target memory. LOCK# is used to prevent more than one master from using a particular system resource.	58	U3	TTL	I/O	4	PCI Spec
PCI_VCC	**PCI Bus VCC:** These pins can be connected to either a 3.3- or 5-volt power supply. The PCI bus interface pin outputs listed in this table (Table 2-1) will operate at the voltage applied to these pins, independent of the voltage applied to other OZ6833 pin groups.	6, 21, 37, 50	D3, G1, L1, T1	-	PWR		-

PCMCIA Sockets Interface Pins

Socket A pin number --- Socket B pin number

Name[1]	Description[2]	Pin Number				Qty	I/O	Pwr	Drive
		Socket A		Socket B					
		TQFP	BGA	TQFP	BGA				
-REG#/ CCBE3#	**Register Access:** During PCMCIA memory cycles, this output chooses between attribute and common memory. During I/O cycles for non-DMA transfers, this signal is active (low). During ATA mode, this signal is always inactive. For DMA cycles on the OZ6833 to a DMA-capable card, -REG is inactive during I/O cycles to indicate DACK to the PCMCIA card. **CardBus Command Byte Enable:** In CardBus mode, this pin is the CCBE3#.	112	P15	188	D7	1	I/O	2 or 3	CardBus spec.
A[25:24]/ CAD[19, 17]	PCMCIA socket address 25:24 outputs. **CardBus Address/Data:** CardBus mode, these pins are the CAD bits 19 and 17.	102, 99	R15, U15	176, 174	D10, B11	2	I/O	2 or 3	CardBus spec.
A23/ CFRAME#	PCMCIA socket address 23 output. **CardBus Frame:** In CardBus mode, this pin is the CFRAME# signal.	96	U14	172	D11	1	I/O	2 or 3	CardBus spec.

Name[1]	Description[2]	Pin Number				Qty	I/O	Pwr	Drive
		Socket A		Socket B					
		TQFP	BGA	TQFP	BGA				
A22/ CTRDY#	PCMCIA socket address 22 output. **CardBus Target Ready:** In CardBus mode, this pin is the CTRDY# signal.	94	R13	170	A13	1	I/O-PU	2 or 3	CardBus spec.
A21/ CDEVSEL#	PCMCIA socket address 21 output. **CardBus Device Select:** In CardBus mode, this pin is the CDEVSEL# signal.	92	U12	168	C13	1	I/O-PU	2 or 3	CardBus spec.
A20/ CSTOP#	PCMCIA socket address 20 output. **CardBus Stop:** In CardBus mode, this pin is the CSTOP# signal.	90	T12	166	A14	1	I/O-PU	2 or 3	CardBus spec.
A19/ CBLOCK#	PCMCIA socket address 19 output. **CardBus Lock:** In CardBus mode, this signal is the CBLOCK# signal used for locked transactions.	88	P12	164	C14	1	I/O-PU	2 or 3	CardBus spec.
A18/ RFU	PCMCIA socket address 18 output. **Reserved:** In CardBus mode, this pin is reserved for future use.	85	U10	161	B14	1	TO	2 or 3	CardBus spec.
A17/ CAD16	PCMCIA socket address 17 output. **CardBus Address/Data:** In CardBus mode, this pin is the CAD bit 16.	83	R10	158	D14	1	I/O	2 or 3	CardBus spec.
A16/ CCLK#	PCMCIA socket address 16 output. **CardBus Clock:** In CardBus mode, this pin supplies the clock to the inserted card.	93	P13	169	B12	1	I/O	2 or 3	CardBus spec.
A15/ CIRDY#	PCMCIA socket address 15 output. **CardBus Initiator Ready:** In CardBus mode, this pin is the CIRDY# signal.	95	T13	171	C12	1	I/O-PU	2 or 3	CardBus spec.
A14/ CPERR#	PCMCIA socket address 14 output. **CardBus Parity Error:** CardBus mode, this pin is the CPERR# signal.	86	T11	162	A15	1	I/O-PU	2 or 3	CardBus spec.
A13/ CPAR	PCMCIA socket address 13 output. **CardBus Parity:b** In CardBus mode, this pin is the CPAR signal.	84	P11	159	B15	1	I/O	2 or 3	CardBus spec.
A12/ CCBE2#	PCMCIA socket address 12 output. **CardBus Command/Byte Enable:** In CardBus mode, this pin is the CCBE2# signal.	97	U13	173	A12	1	I/O	2 or 3	CardBus spec.
A[11:9]/ CAD[12, 9, 14]	PCMCIA socket address 11:9 output. **CardBus Address/Data:** In CardBus mode, these pin are the CAD bits 12, 9 and 14.	77, 73, 80	U8, U7, P10	153, 149, 155	C17, E17, C16	3	I/O	2 or 3	CardBus spec.
A8/ CCBE1#	PCMCIA socket address 8 output. **CardBus Command/Byte Enable:** In CardBus mode, this pin is the CCBE1# signal.	82	T10	157	A17	1	I/O	2 or 3	CardBus spec.
A[7:0]/ CAD[18, 20-26]	PCMCIA socket address 7:0 outputs. **CardBus Address/Data:** In CardBus mode, these pins are the CAD bits 18 and 20:26.	100, 103, 105, 107, 109, 111, 113, 116	R14, T15, U17, T17, P16, N14, N16, N15	175, 178, 181, 183, 185, 187, 189, 191	C11, B10, A10, C9, A9, C8, A8, C7	8	I/O	2 or 3	CardBus spec.
D15/ CAD8	PCMCIA socket data/0 bit 15. **CardBus Address/Data:** In CardBus mode, this pin is the CAD bit 8.	71	R7	148	D17	1	I/O	2 or 3	CardBus spec.
D14/ RFU	PCMCIA socket data I/0 bit 14. **Reserved:** In CardBus mode, this pin is reserved for future use.	69	U6	145	E14	1	I/O	2 or 3	2 mA

Name[1]	Description[2]	Pin Number				Qty	I/O	Pwr	Drive
		Socket A		Socket B					
		TQFP	BGA	TQFP	BGA				
D[13:3]/ CAD[6, 4, 2, 31, 30, 28, 7, 5, 3, 1, 0]	PCMCIA socket data I/0 bits 13:3. **CardBus Address/Data:** In CardBus mode, this pin is the CAD bit 6 4, 2, 31, 30, 28, 7, 5, 3, 1, and 0, respectively.	67, 65, 63, 124, 122, 120, 68, 66, 64, 62, 59	R6, P6, T5, K14, L16, L14, P7, T6, U5, R5, R4	142, 140, 138, 199, 197, 195, 144, 141, 139, 137, 135	F16, F14, G16, A5, B5, D5, F17, G17, G15, H17, H15	11	I/O	2 or 3	CardBus spec.
D2/ RFU	PCMCIA socket data I/O bit 2. **Reserved:** In CardBus mode, this pin is reserved for future use.	123	L15	198	A6	1	I/O	2 or 3	CardBus spec.
D[1:0]/ CAD[29,27]	PCMCIA socket data I/O bits 1:0. **CardBus Address/Data:** In CardBus mode, these pins are the CAD bits 29 and 27, respectively.	121, 119	M17, M15	196, 194	C6, B6	2	I/O	2 or 3	CardBus spec.
-OE/ CAD11	**Output Enable**: This output goes active (low) to indicate a memory read from the PCMCIA socket to the OZ6833. **CardBus Address/Data:** In CardBus mode, this pin is the CAD bit 11.	75	R8	151	D16	1	I/O	2 or 3	CardBus spec.
-WE/ CGNT#	**Write Enable**: This output goes active (low) to indicate a memory write from the OZ6833 to the PCMCIA socket. **CardBus Grant:** In CardBus mode, this pin is the CGNT# signal.	89	U11	165	B13	1	TO	2 or 3	CardBus spec.
-IORD/ CAD13	**I/O Read**: This output goes active (low) for I/O reads from the socket to the OZ6833. **CardBus Address/Data:** In CardBus mode, this pin is the CAD bit 13.	78	T9	154	C15	1	I/O	2 or 3	CardBus spec.
-IOWR/ CAD15	**I/O Write**: This output goes active (low) for I/O writes from the OZ6833 to the socket. **CardBus Address/Data:** In CardBus mode, this pin is the CAD bit 15.	81	U9	156	B16	1	I/O	2 or 3	CardBus spec.
WP/ -IOIS16/ CCLKRUN#	**Write Protect/ I/O Is 16-Bit**: In Memory Card Interface mode, this inputs is interpreted as the status of the write protect switch on the PCMCIA card. In I/O Card Interface mode, this input indicates the size of the I/O data at the current address on the PCMCIA card. **CardBus Clock Run:** In CardBus mode, this pin is the CCLKRUN# signal, which starts and stops the CardBus CCLK. To enable the CLKRUN# signal, ExCA register 3Bh/7Bh bit[3:2] must be enabled.	125	L17	201	B4	1	I/O-PU	2 or 3	CardBus spec.

Name[1]	Description[2]	Pin Number				Qty	I/O	Pwr	Drive
		Socket A		Socket B					
		TQFP	BGA	TQFP	BGA				
-INPACK/ CREQ#	**Input Acknowledge**: The -INPACK function is not applicable in PCI bus environments. However, for compatibility with other Cirrus Logic products, this pin should be connected to the PCMCIA socket's -INPACK pin. **CardBus Request:** In CardBus mode, this pin is the CREQ# signal.	110	R17	186	B8	1	I-PU	2 or 3	CardBus spec.
RDY/ -IREQ/ CINT#	**Ready/Interrupt Request**: In Memory Card Interface mode, this input indicates to the OZ6833 that the card is either ready or busy. In I/O Card Interface mode, this input indicates a card interrupt request. **CardBus Interrupt:** In CardBus mode, this pin is the CINT# signal. This signal is active-low and level-sensitive.	91	R12	167	D12	1	I-PU	2 or 3	CardBus spec.
-WAIT/ CSERR#	**Wait**: This input indicates a request by the card to the OZ6833 to halt the cycle in progress until this signal is deactivated. **CardBus System Error:** In CardBus mode, this pin is the CSERR# signal.	108	P14	184	D8	1	I-PU	2 or 3	CardBus spec.
CD[2:1]/ CCD[2:1]#	**Card Detect**: These inputs indicate to the OZ6833 that a card is in the socket. They are internally pulled high to the voltage of the AuxVCC power pin. **CardBus Card Detect:** In CardBus mode, these inputs are used with CVS[2:1] to detect presence and type of card.	126, 61	K16, P5	202, 136	A4, G14	2	I-PU-Schmitt	1	CardBus spec.
-CE2/ CAD10	**Card Enable** pin is driven low by the OZ6833 during card access cycles to control byte/word card access. -CE1 enables even-numbered address bytes, and -CE2 enables odd-numbered address bytes. When configured for 8-bit cards, only -CE1 is active and A0 is used to indicate access of odd- or even-numbered bytes. **CardBus Address/Data:** In CardBus mode, this pin is the CAD bit 10.	74	T8	150	D15	1	I/O	2 or 3	CardBus spec.
-CE1/ CCBE0#	**Card Enable** pin is driven low by the OZ6833 during card access cycles to control byte/word card access. -CE1 enables even-numbered address bytes, and -CE2 enables odd-numbered address bytes. When configured for 8-bit cards, only -CE1 is active and A0 is used to indicate access of odd- or even-numbered bytes. **CardBus Command/Byte Enable:** In CardBus mode, this pin is the CCBEO# signal.	70	T7	147	E16	1	I/O	2 or 3	CardBus spec.
RESET/ CRST#	**Card Reset**: This output is low for normal operation and goes high to reset the card. To prevent reset glitches to a card, this signal is high-impedance unless a card is seated in the socket, card power is applied, and the card's interface signals are enabled. **CardBus Reset:** In CardBus mode, this pin is the CRST# output.	106	R16	182	B9	1	TO	2 or 3	CardBus spec.

Name[1]	Description[2]	Pin Number				Qty	I/O	Pwr	Drive
		Socket A		Socket B					
		TQFP	BGA	TQFP	BGA				
BVD2/ -SPKR/ -LED/ CAUDIO	**Battery Voltage Detect 2/Speaker/ LED**: In Memory Card Interface mode, this input serves as the BVD2 (battery warning status) input. In I/O Card Interface mode, this input can be configured as a card's -SPKR binary audio input. For ATA or non-ATA (SFF-68) disk-drive support, this input can also be configured as a drive-status LED input. **CardBus Audio:** In CardBus mode, this pin is the CAUDIO input.	114	P17	190	B7	1	I-PU	2 or 3	-
BVD1/ -STSCHG/ -RI/ -CSTSCHG	**Battery Voltage Detect 1/Status Change/Ring Indicate**: In Memory Card Interface mode, this input serves as the BVD1 (battery-dead status) input. In I/O Card Interface mode, this input is the -STSCHG input, which indicates to the OZ6833 that the card's internal status has changed. If bit 7 of the **Interrupt and General Control** register is set to `1`, this pin serves as the ring indicate input for wakeup-on-ring system power management support. **CardBus Status Change:** In CardBus mode, this pin is the CSTSCHG. This pin can be used to generate PME#.	118	M16	192	D6	1	I-PU	2 or 3	-
VS2/ CVS2	**Voltage Sense 2:** This pin is used in conjunction with VS1 to determine the operating voltage of the card. This pin is internally pulled high to the voltage of the AuxVCC power pin under the combined control of the external data write bits and the CD pull up control bits. This pin connects to PCMCIA socket pin 57. **CardBus Voltage Sense:** In CardBus mode, these pins are the CVS2 pin.	104	T16	179	C10	1	I/O-PU	1	CB-spec
VS1/ CVS1	**Voltage Sense 1:** This pin is used in conjunction with VS2 to determine the operating voltage of the card. This pin is internally pulled high to the voltage of the AuxVCC power pin under the combined control of the external data write bits and the CD pull up control bits. This pin connects to PCMCIA socket pin 43. **CardBus Voltage Sense:** In CardBus mode, these pins are the CVS1 pin.	76	P9	152	B17	1	I/O-PU	1	CB-spec
SOCKET_VCC	Connect these pins to the Vcc supply of the socket (pins 17 and 51 of the respective PCMCIA socket). These pins can be 0, 3.3, or 5 V, depending on card presence, card type, and system configuration. The socket interface outputs (listed in this table, Table 2-2) will operate at the voltage applied to these pins, independent of the voltage applied to other OZ6833 pin groups.	117, 98, 60	N17, T14, U4	200, 160, 143	C5, A16, F15	3	PWR	-	-

[1]To differentiate the sockets in the pin diagram, all socket- specific pins have either A_ or B_ prefixes to the pin names indicated. For example, A_A[25:0] and B_A[25:0] are the independent address buses to the sockets.
[2]When a socket is configured as an ATA drive interface, socket interface pin functions change.

Power Control and General Interface Pins

Pin Name	Description	Pin Number		Input	Type	Power Rail	Drive
		TQFP	BGA				
SPKR_OUT	**Speaker Output:** This output can be used as a digital output to a speaker to allow a system to support PC Card fax/modem/voice and audio sound output. This output is enabled by setting the socket's **Misc. Control 1** register bit 4 to "1" (for the socket whose speaker signal is to be directed from BVD2/-SPKR/-Led to this pin).	128	J14	TTL	I/O	1	12mA
LED_OUT/ SKTA_ACTV	**LED Output/SKTA_ACTV:** This output can be used as an LED driver to indicate disk activity when a socket's BVD2/-SPKR/-LED pin has been programmed for LED support. In the O2 Mode(Index 3B/7B bit 5) , this pin indicates the socket A activity. The socket B activity refers to PCI Configuration Register offset 90h (Mux Control register)	133	J17	TTL	I/O	1	12mA
CPWRCLK/ A_VCC5#	**Card Power Clock:** This input is used as a reference clock (10-100 kHz, usually 32 kHz) to control the serial interface of the socket power control chips. A_VCC5#: This active-LOW output controls the 5 -volt supply to the A socket's VCC pins. The active-LOW level of this output is mutually exclusive with that of -VCC_3.	132	H14	TTL	I/O	1	12mA
CPWRDATA/ B_VCC3#	**Card Power Serial Data:** This pin serves as output DATA pin when used with the serial interface of Texas Instruments' TPS2202IDF socket power control chip. B_VCC3#: This active-LOW output controls the 3.3-volt supply to the A socket's VCC pins. The active-LOW level of this output is mutually exclusive with that of -VCC_5.	131	**J15**	TTL	I/O	1	12mA
CPWRLATC/ B_VCC5#	**Card Power Serial Latch:** This pin serves as output LATCH pin when used with the serial interface of Texas Instruments' TPS2202IDF socket power control chip. B_VCC5#: This active-LOW output controls the 5 -volt supply to the A socket's VCC pins. The active-LOW level of this output is mutually exclusive with that of -VCC_3.	130	J16	N/A	I/O	1	12mA

Pin Name	Description	Pin Number		Input	Type	Power Rail	Drive
		TQFP	BGA				
A_VCC3#	This active-LOW output controls of the 3.3-volt supply to the socket's VCC pins. The active-LOW level of this output is mutually exclusive with of VCC_5#. **This mode active only in SktPwr Parallel mode enabled**	87	R11	N/A	TO	1	4mA
A_VPP_VCC	**VPP_VCC:** This active-HIGH output controls the socket A VCC supply to the socket's VPP1 and VPP2 pins. The active-HIGH level of this output is mutually exclusive with that of VPP_PGM. **This mode active only in SktPwr Parallel mode enabled**	115	M14	N/A	TO	1	4mA
B_VPP_VCC	**VPP_VCC:** This active-HIGH output controls the socket B VCC supply to the socket's VPP1 and VPP2 pins. The active-HIGH level of this output is mutually exclusive with that of VPP_PGM. **This mode active only in SktPwr Parallel mode enabled**	146	E15	N/A	TO	1	4mA

Power, Ground, and Reserved Pins

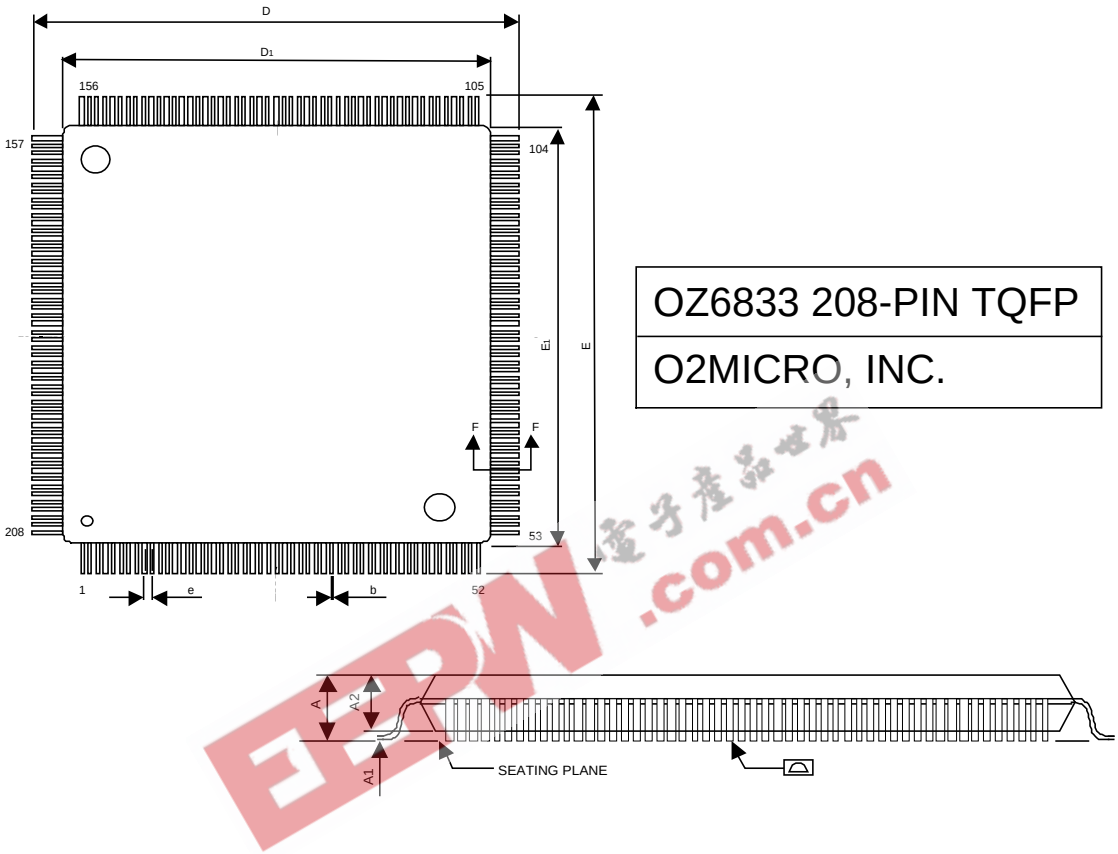
Pin Name	Description	Pin Number		Input	Type	Power Rail	Drive
		TQFP	BGA				
AUX_VCC	This pin is connected to the system's 5-volt power supply. In systems where 5 volts is not available, this pin can be connected to the system's 3.3-volt supply if your PCI_VCC and CORE_VCC connected to 3.3V	127	K15	N/A	PWR	-	-
CORE_VCC	This pin provides power to the core circuitry of the OZ6833. It could be connected to a 3.3 power supply.	134, 79, 180	H16, R9, D9	N/A	PWR	-	-
CORE_GND	All OZ6833 ground pins should be connected to system ground.	26, 14, 28, 44, 57, 101, 129, 177	A11, J2, K4, K17, N3, T4, F2, U16	N/A	GND	-	-

Legend

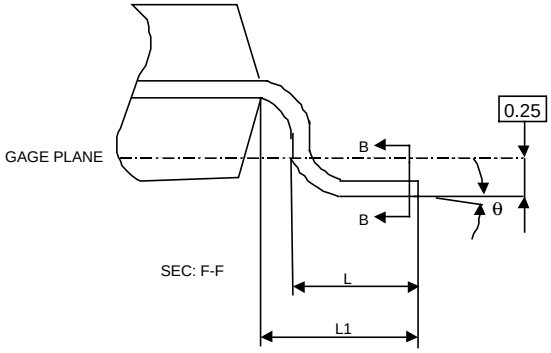
I/O Type	Description
I	Input Pin
I-PU	Input pin with internal pull-up
O	Output
OD	Open-drain
TO	Tri-state output
TO-PU	Tri-state output with internal pull-up
OD-PU	Open-drain output with internal pull-up
PW	Power pin

Power Rail	Source of Output's Power
1	AUX_VCC: outputs powered from AUX_VCC
2	A_SLOT_VCC: outputs powered from the socket A
3	B_SLOT_VCC: outputs powered from the socket B
4	PCI_VCC: outputs powered from PCI bus power supply
5	CORE_VCC: outputs powered from the CORE_VCC

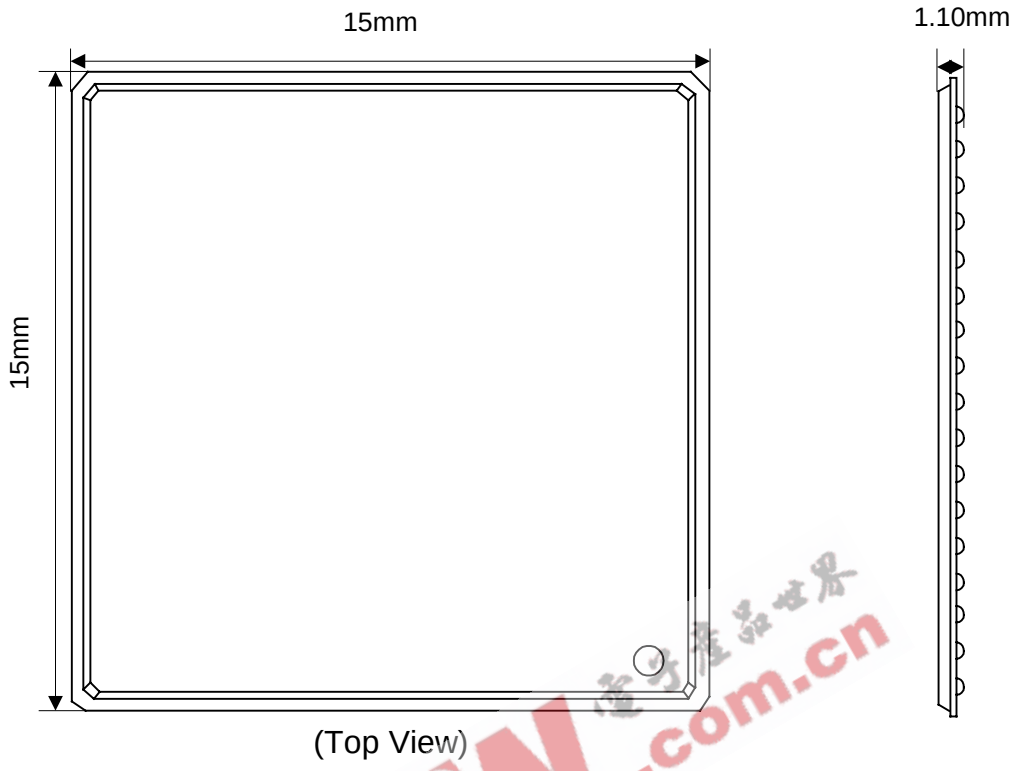
PACKAGE SPECIFICATIONS



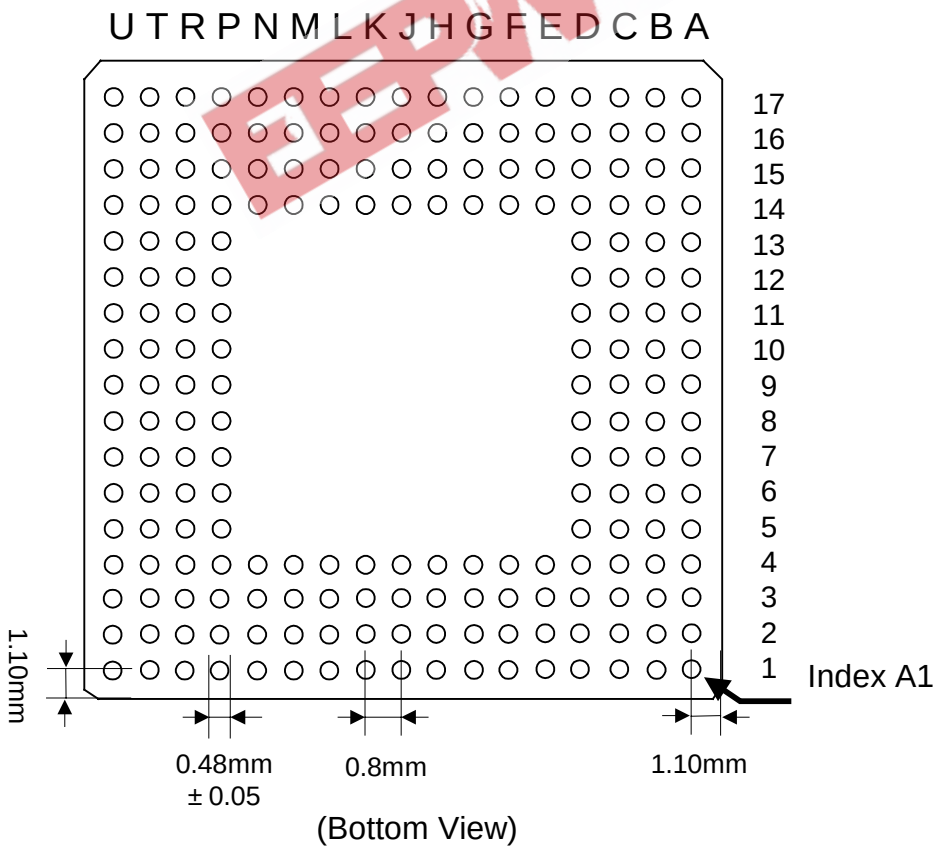
Symbol	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.063	-	-	1.60
A_1	0.002	-	0.006	0.05	-	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	-	0.008	0.09	-	0.20
D		1.181			30.00 BSC.	
D_1		1.102			28.00 BSC.	
E		1.181			30.00 BSC.	
E_1		1.102			28.00 BSC.	
e		0.020 BSC.			0.50 BSC.	
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1		0.039 REF			1.00 REF	
θ	0°	3.5°	7°	0°	3.5°	7°



208 PIN – BGA



(Top View)



(Bottom View)