OZ968

SMBus Smart Inverter Controller

FEATURES

- Single-stage power conversion
- Constant frequency design eliminates interference with LCDs
- Built-in open-lamp protection and short-circuit protection
- Reliable 2-winding transformer design eliminates arcing failures and the need for fold-back wiring
- 32-level dimming and 256-level contrast control via SMBus
- High efficiency, 90% typical
- Supports both floating secondary and grounded secondary designs

ORDERING INFORMATION

OZ968G - 16-pin plastic SOP

GENERAL DESCRIPTION

The OZ968 is a unique single-stage, high-efficiency, CCFL backlight controller. It drives a zero-voltage-switching circuit and provides a near sinusoidal output voltage and current waveforms for a CCFL backlight. Typical operating frequency ranges from 30KHz to 100KHz. These advances drive the OZ968 beyond comparable conventional inverter designs with two power conversion stages (one operates at a variable frequency, the other at a constant frequency).

Operating in a PWM push-pull drive, the transformer in an OZ968 backlight inverter requires only one primary winding and one secondary winding. The secondary winding requires no fold-back treatment.

The OZ968 supports a bi-directional, two-wire bus, data transmission protocol to control dimming (32 levels) and contrast (256 levels). Supply current is 1mA in active mode, 150µA in standby mode.

The OZ968 is available in a 16-pin SOP package. It is specified over the commercial temperature range 0°C to +70°C.

TYPICAL APPLICATION CIRCUIT

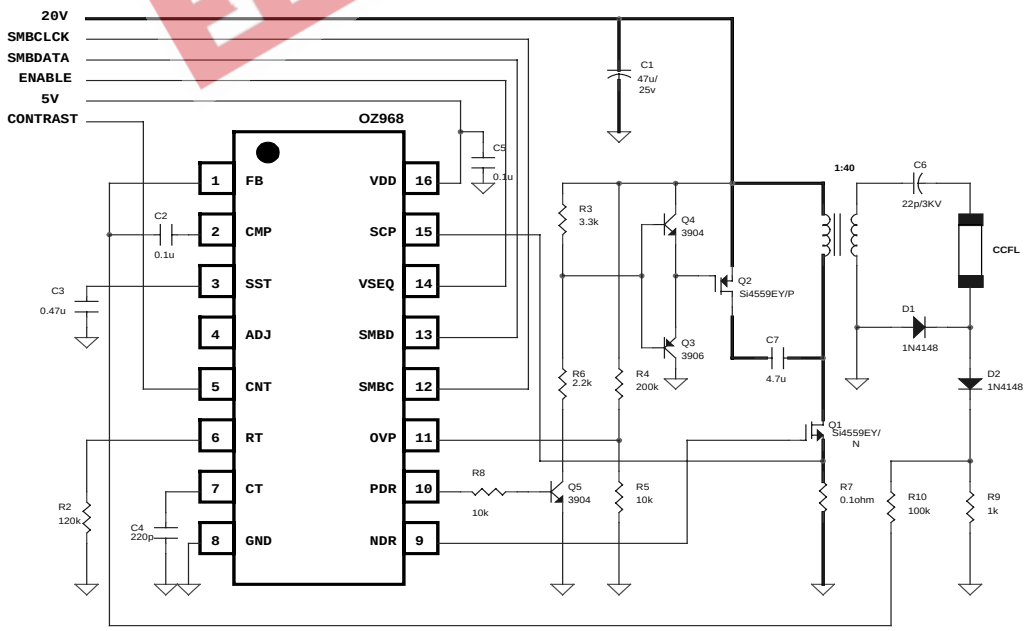


Figure 1. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

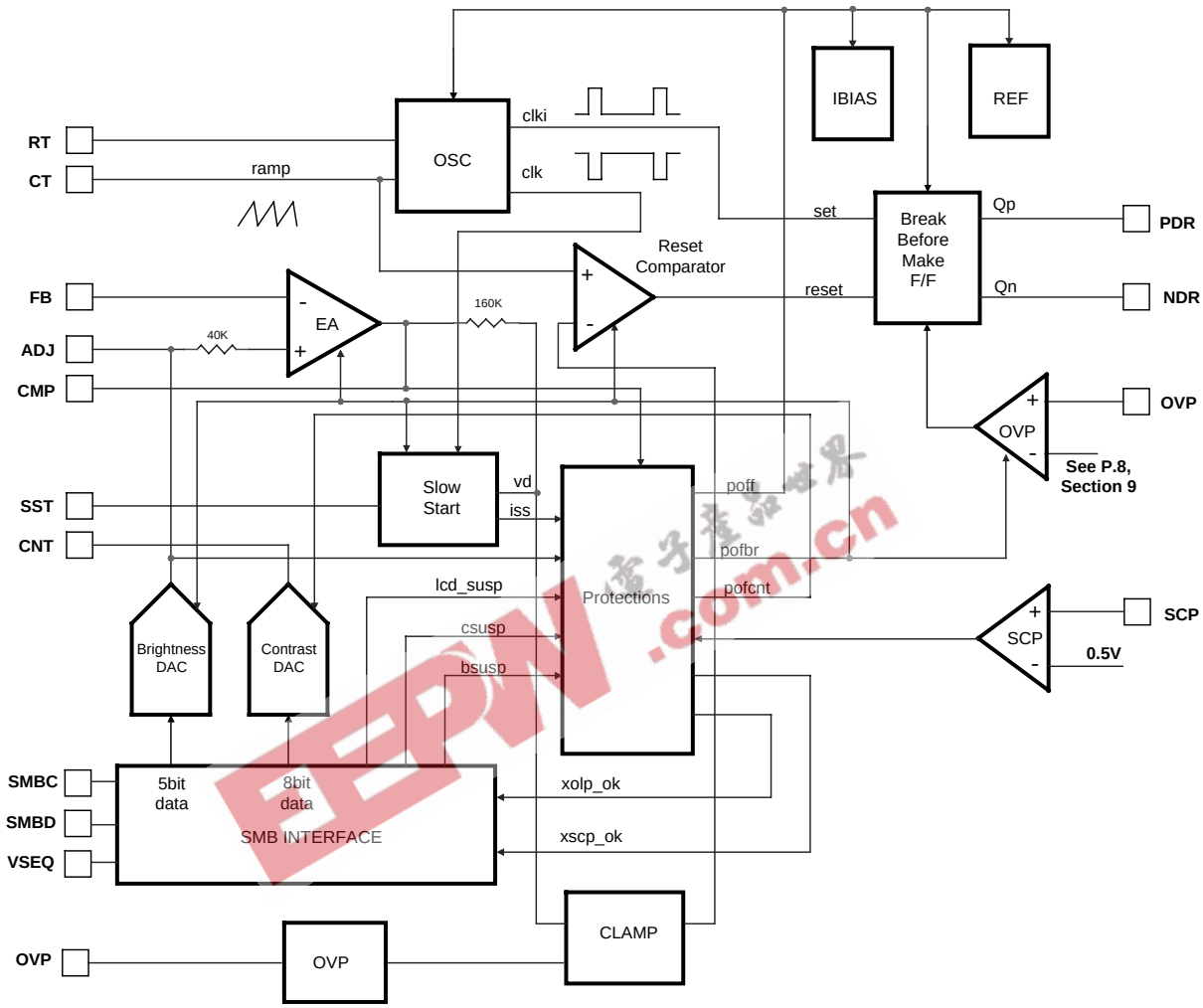


Figure 2. Functional Block Diagram

PIN CONFIGURATION

Pin No.	Name	Description
1	FB	Current sense feedback.
2	CMP	Compensation for the current sense feedback.
3	SST	Soft start in two steps. Two-interval current sources of 50µA and 0.6µA provide 1:26.6 ratio between the two time intervals of soft start. Connect a capacitor between this pin and the ground to adjust the soft-start timing.
4	ADJ	The output of the brightness D/A converter. The brightness has 32 adjustable levels. The default range is between 0.9V to 2.5V.
5	CNT	The output of the contrast D/A converter. The contrast has 256 levels from 0.8V to 2.8 V (8mV per step). This output has a current capability of up to 2mA.
6	RT	Timing resistor.
7	CT	Timing capacitor. CT and RT set the clock frequency. Fs = 1.60 / (RT * CT).
8	GND	Ground.
9	NDR	Gate drive output for the N-MOSFET.
10	PDR	Gate drive output for the P-MOSFET.
11	OVP	Over-voltage protection sense input.
12	SMBC	SMBus Clock Input/Output
13	SMBD	SMBus Data Input/Output.
14	VSEQ	Vee power sequence input.
15	SCP	Short-circuit protection sense input.
16	VDD	Supply voltage input.

ABSOLUTE MAXIMUM RATINGS

VDD	7.0 V
GND	+/- 0.3 V
Storage temp.	-55 to 150 ^{O}C
Operating temp.	0 to 70 ^{O}C
Operating junction temp.	150 ^{O}C
Logic inputs	-0.3 V to VDD+0.3 V

RECOMMENDED OPERATING RANGE

VDD	4.75 V to 5.25 V
Fosc	30 KHz to 100 KHz
Rt	50 K to 150 K

FUNCTIONAL SPECIFICATIONS

Parameter	Test Conditions VDD = 5V, Tj =25, Test Circuit	Limits Min	Typ	Max	Unit
Oscillator					
Initial accuracy	Ct = 270pF, Rt = 100k	54	59	64	KHz
Temp. stability	TA = 0°C to 70°C	-	200	500	ppm/ °C
Line regulation	4.5 V < VDD <5.5V	-	2	3	%
Error Amplifier					
Bias current		-	2.5	5	µA
Input offset voltage		-	2.0	5.0	mV
Open loop voltage gain		60	80	-	dB
Unity gain bandwidth		-	2.0	-	MHz
Dimming D/A Output (ADJ – floating)					
Maximum level		2.40	2.50	2.65	V
Minimum level		0.8	0.9	1.0	V
Power-on reset default		2.40	2.5	2.65	V
Settling time		-	10	-	µs
D/A output levels		-	32	-	
Contrast D/A Output					
Maximum level		2.70	2.80	2.95	V
Minimum level		0.75	0.80	0.90	V
Power-on reset default		0.75	0.80	0.90	V
Settling time		-	10	-	µs
Maximum output current		-	2.0	2.2	mA
Load regulation		-	50	100	mV/mA
D/A output levels		-	256	-	
Under-voltage Lockout					
Power-on Voltage		3.8	4.0	4.2	V
Hysteresis		-	0.3	-	V
Break-before-Make					
Delay (between NDR and PDR)	100KHz, 800pF loading	-	400	-	ns
Supply					
Supply current – Standby Mode		-	150	-	µA
Supply current – Active Mode	100KHz, 800pF loading	-	1	2	mA
Output (NDR and PDR)					
Output high voltage	VDD = 5.0V	4.75	-	-	V
Output low voltage	VDD = 5.0V	-	-	0.25	V
Output resistance	VDD = 5.0V	-	50	-	Ω

TWO-WIRE BUS REGISTER DESCRIPTION

The following register map describes the SMBus interface between SMBus Host and the OZ968

Register Map

For Write commands.

Function	Slave Address (7-bit)	Register Index (Hex)	Data
Contrast	0101 000	A9	byte
Brightness	0101 000	AA	byte

Contrast (A9)

SMBus Protocol: Read or Write Byte
Input/Output: Byte -- bit flags mapped as follows:

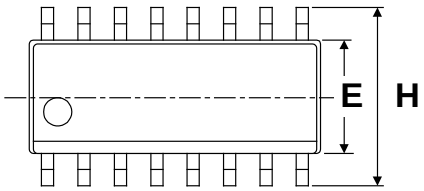
Bit #	Name	R/W	Default	Description
7:0	D7-D0	r/w	0000 0000	Bits D7-D0 contain the contrast level setting. When D7-D0 = FF, the CNT pin of the OZ968 outputs 2.8V. When D7-D0 = 00, the CNT pin outputs 0.8V.

Brightness (AA)

SMBus Protocol: Read or Write Byte
Input/Output: Byte -- bit flags mapped as follows:

Bit #	Name	R/W	Default	Description
7:0	D7-D0	r/w	0000 0000	Bits D7-D0 contain the brightness level setting. When D7-D0 = FF, the OZ968 inverter outputs miniimum brightness. When D7-D0 = 00, the OZ968 inverter outputs maximum brightness.

PACKAGE INFORMATION



SOP-16 PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.0532	0.0688	1.35	1.75
A1	0.0040	0.0098	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.0075	0.0098	0.19	0.25
D	0.3859	0.3937	9.80	10.00
E	0.1497	0.1574	3.80	4.00
e	0.050 BCS.		1.27 BCS.	
H	0.2284	0.2440	5.80	6.20
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°