Bulletin I2776 rev. E 04/99

International
IOR Rectifier

P400 SERIES

PASSIVATED ASSEMBLED CIRCUIT ELEMENTS

40A

Features

- Glass passivated junctions for greater reliability
- Electrically isolated base plate
- Available up to 1200 V_{RRM}, V_{DRM}
- High dynamic characteristics
- Wide choice of circuit configurations
- Simplified mechanical design and assembly
- UL E78996 approved

Description

The P400 series of Integrated Power Circuits consists of power thyristors and power diodes configured in a single package. With its isolating base plate, mechanical designs are greatly simplified giving advantages of cost reduction and reduced size.
Applications include power supplies, control circuits and battery chargers.

Major Ratings and Characteristics

Parameters		P400	Units
I_D		40	A
	@ T_C	80	°C
I_{FSM}	@ 50Hz	385	A
	@ 60Hz	400	A
I^2t	@ 50Hz	745	A^2s
	@ 60Hz	680	A^2s
$I^2\sqrt{t}$		7450	$A^2\sqrt{s}$
V_{RRM}		400 to 1200	V
V_{INS}		2500	V
T_J		- 40 to 125	°C

ELECTRICAL SPECIFICATIONS

Voltage Ratings

Type number	V_{RRM} maximum repetitive peak reverse voltage V	V_{RSM} maximum non-repetitive peak reverse voltage V	V_{DRM} maximum repetitive peak off-state voltage V	I_{RRM} max. @ T_J max. mA
P401, P421, P431	400	500	400	10
P402, P422, P432	600	700	600	
P403, P423, P433	800	900	800	
P404, P424, P434	1000	1100	1000	
P405, P425, P435	1200	1300	1200	

On-state Conduction

	Parameter	P400	Units	Conditions
I_D	Maximum DC output current	40	A	@ T_C = 80°C, full bridge circuits
I_{TSM} / I_{FSM}	Max. peak one-cycle non-repetitive on-state or forward current	385	A	t = 10ms, No voltage reapplied; Sinusoidal half wave, Initial $T_J = T_J$ max.
		400		t = 8.3ms, No voltage reapplied; Sinusoidal half wave, Initial $T_J = T_J$ max.
		325		t = 10ms, 100% V_{RRM} reapplied; Sinusoidal half wave, Initial $T_J = T_J$ max.
		340		t = 8.3ms, 100% V_{RRM} reapplied; Sinusoidal half wave, Initial $T_J = T_J$ max.
I^2t	Maximum I^2t for fusing	745	A^2s	t = 10ms, No voltage reapplied; Initial $T_J = T_J$ max.
		680		t = 8.3ms, No voltage reapplied; Initial $T_J = T_J$ max.
		530		t = 10ms, 100% V_{RRM} reapplied; Initial $T_J = T_J$ max.
		480		t = 8.3ms, 100% V_{RRM} reapplied; Initial $T_J = T_J$ max.
$I^2\sqrt{t}$	Maximum $I^2\sqrt{t}$ for fusing	7450	$A^2\sqrt{s}$	t = 0.1 to 10ms, no voltage reapplied I^2t for time tx = $I^2\sqrt{t} \cdot \sqrt{tx}$
$V_{T(TO)1}$	Low value of threshold voltage	0.83	V	(16.7% x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ max.
$V_{T(TO)2}$	High value of threshold voltage	1.03		(I > π x $I_{T(AV)}$), $T_J = T_J$ max.
r_{t1}	Low level value of on-state slope resistance	9.61	mΩ	(16.7% x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ max.
r_{t2}	High level value of on-state slope resistance	7.01		(I > π x $I_{T(AV)}$), $T_J = T_J$ max.
V_{TM} / V_{FM}	Max. peak on-state or forward voltage drop	1.4	V	T_J = 25°C, I_{TM} = π x $I_{T(AV)}$ T_J = 25°C, I_{TM} = π x $I_{F(AV)}$
di/dt	Maximum non repetitive rate of rise of turned on current	200	A/µs	T_J = 125°C from 0.67 V_{DRM} I_{TM} = π x $I_{T(AV)}$, I_g = 500mA, tr < 0.5µs, tp > 6µs
I_H	Maximum holding current	130	mA	T_J = 25°C anode supply = 6V, resistive load
I_L	Maximum latching current	250	mA	T_J = 25°C anode supply = 6V, resistive load

Blocking

	Parameter	P400	Units	Conditions
dv/dt	Maximum critical rate of rise of off-state voltage	200	V/µs	T_J = 125°C, exponential to 0.67 V_{DRM} gate open
I_{RRM} I_{DRM}	Max. peak reverse and off-state leakage current at V_{RRM}, V_{DRM}	10	mA	T_J = 125°C, gate open circuit
I_{RRM}	Max peak reverse leakage current	100	µA	T_J = 25°C
V_{INS}	RMS isolation voltage	2500	V	50Hz, circuit to base, all terminal shorted, T_J = 25°C, t = 1s

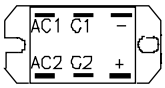
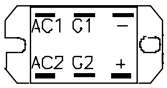
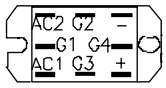
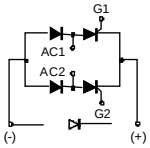
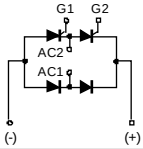
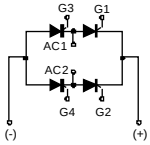
Triggering

	Parameter	P400	Units	Conditions	
P_{GM}	Maximum peak gate power	8	W		
$P_{G(AV)}$	Maximum average gate power	2			
I_{GM}	Maximum peak gate current	2	A		
- V_{GM}	Maximum peak negative gate voltage	10	V		
V_{GT}	Maximum gate voltage required to trigger	3 2 1		T_J = - 40°C T_J = 25°C T_J = 125°C	Anode Supply = 6V resistive load
I_{GD}	Maximum gate current required to trigger	90 60 35	mA	T_J = - 40°C T_J = 25°C T_J = 125°C	Anode Supply = 6V resistive load
V_{GD}	Maximum gate voltage that will not trigger	0.2	V	T_J = 125°C, rated V_{DRM} applied	
I_{GD}	Maximum gate current that will not trigger	2	mA	T_J = 125°C, rated V_{DRM} applied	

Thermal and Mechanical Specification

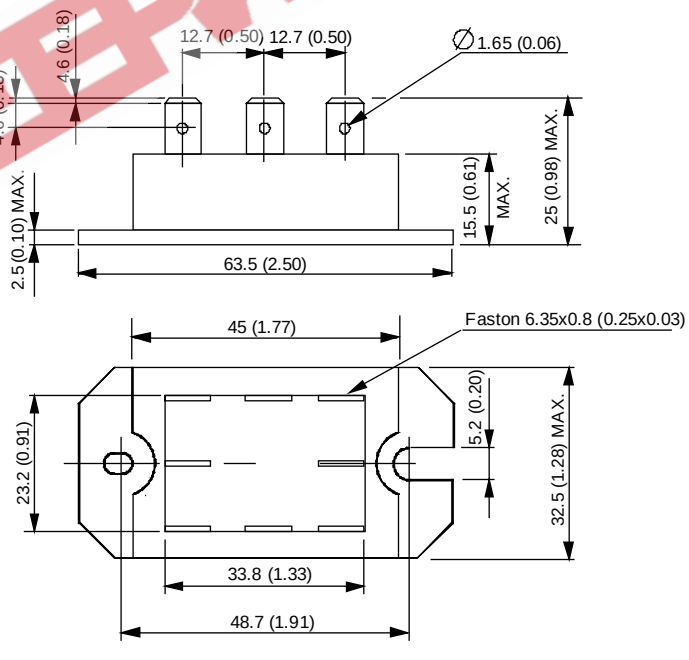
	Parameter	P400	Units	Conditions
T_J	Max. operating temperature range	-40 to 125	°C	
T_{stg}	Max. storage temperature range	-40 to 125		
R_{thJC}	Max. thermal resistance, junction to case	1.05	K/W	DC operation per junction
R_{thCS}	Max. thermal resistance, case to heatsink	0.10	K/W	Mounting surface, smooth and greased
T	Mounting torque, base to heatsink	4	Nm	A mounting compound is recommended and the torque should be checked after a period of 3 hours to allow for the spread of the compound
wt	Approximate weight	58 (2.0)	g (oz)	

Circuit Type and Coding *

	Circuit"0"	Circuit"2"	Circuit"3"
Terminal Positions			
Schematic diagram diagram			
	Single Phase Hybrid Bridge Common Cathode	Single Phase Hybrid Bridge Doubler	Single Phase All SCR Bridge
Basic series	P40.	P42.	P43.
With voltage suppression	P40.K	P42.K	P43.K
With free-wheeling diode	P40.W	-	-
With both voltage suppression and free-wheeling diode	P40.KW	-	-

* To complete code refer to voltage ratings table, i.e.: for 600V P410.W complete code is P402W

Outline Table



All dimensions in millimeters (inches)

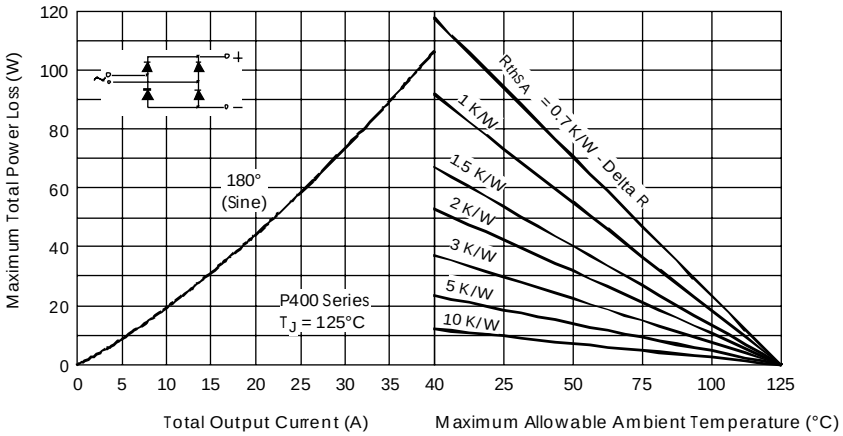


Fig. 1 - Current Ratings Nomogram (1 Module Per Heatsink)

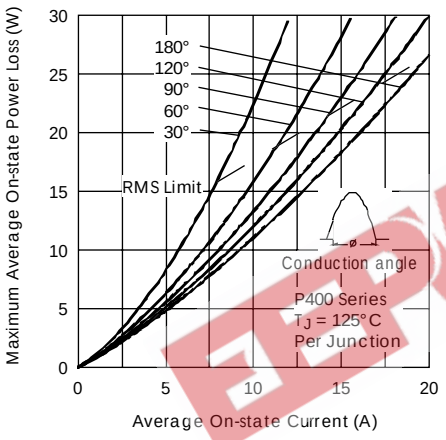


Fig. 2 - On-state Power Loss Characteristics

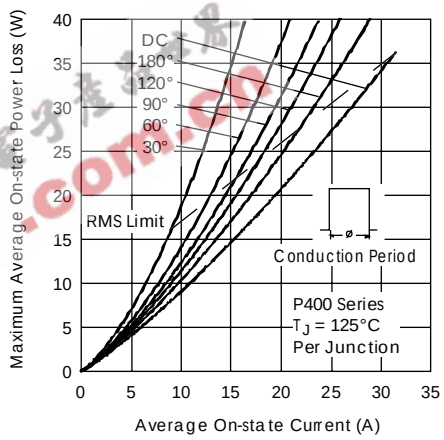


Fig. 3 - On-state Power Loss Characteristics

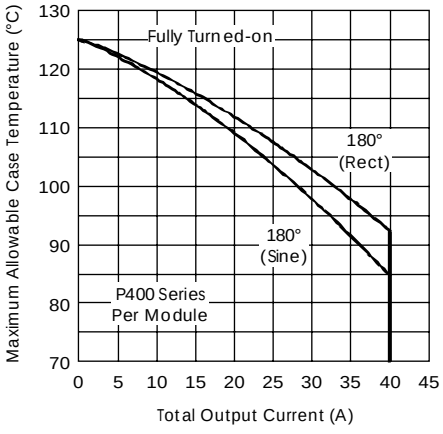


Fig. 4 - Current Ratings Characteristics

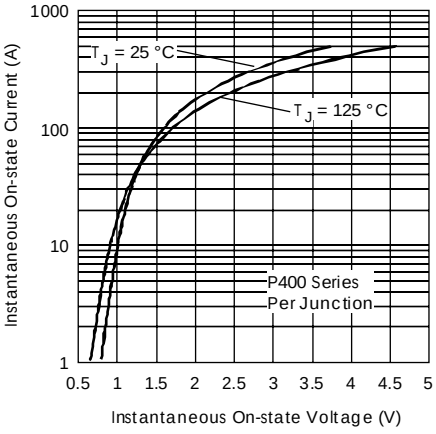


Fig. 5 - On-state Voltage Drop Characteristics

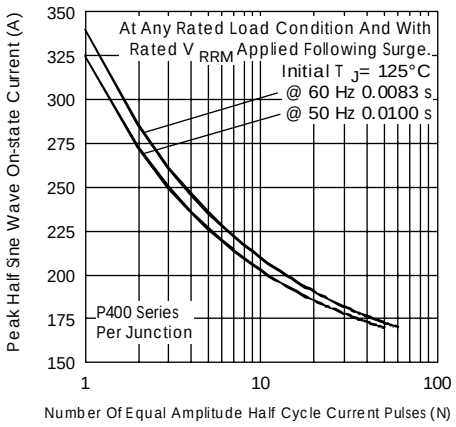


Fig. 6 - Maximum Non-Repetitive Surge Current

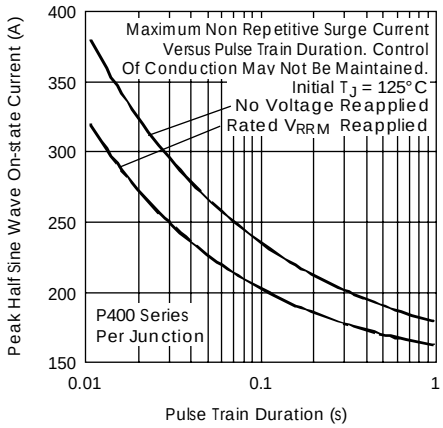


Fig. 7 - Maximum Non-Repetitive Surge Current

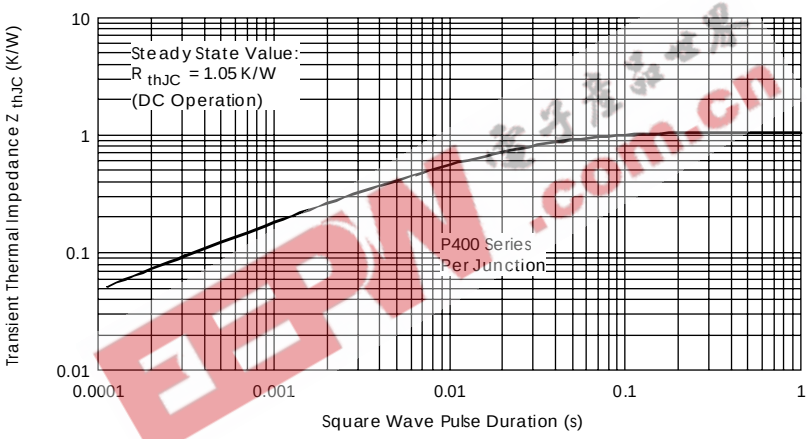


Fig. 8 - Thermal Impedance Z_{thJC} Characteristics

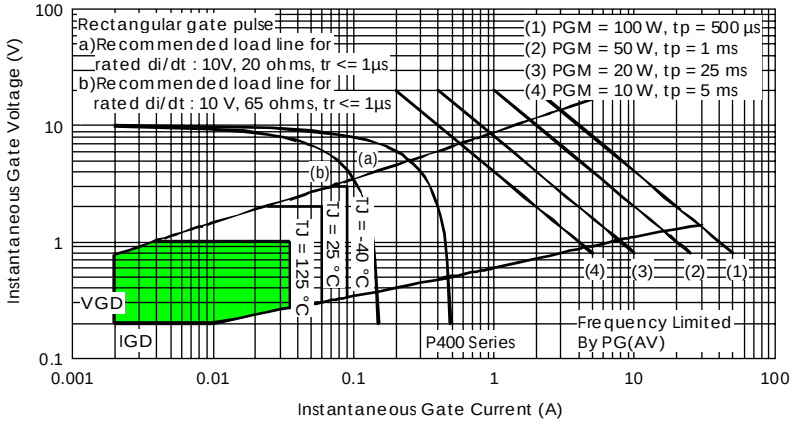


Fig. 9 - Gate Characteristics

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