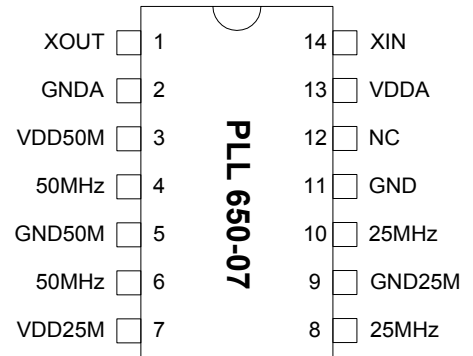


LOW COST Network LAN Clock SOURCE

FEATURES

- Full CMOS output swing with 40-mA output drive capability. 25-mA output drive at TTL level.
- Advanced, low power, sub-micron CMOS processes.
- 25MHz fundamental crystal or clock input.
- 2 outputs fixed at 50MHz, 2 outputs fixed at 25MHz .
- Zero PPM synthesis error in all clocks.
- Ideal for Network switches.
- 3.3V operation.
- Available in 14-Pin 150mil SOIC.

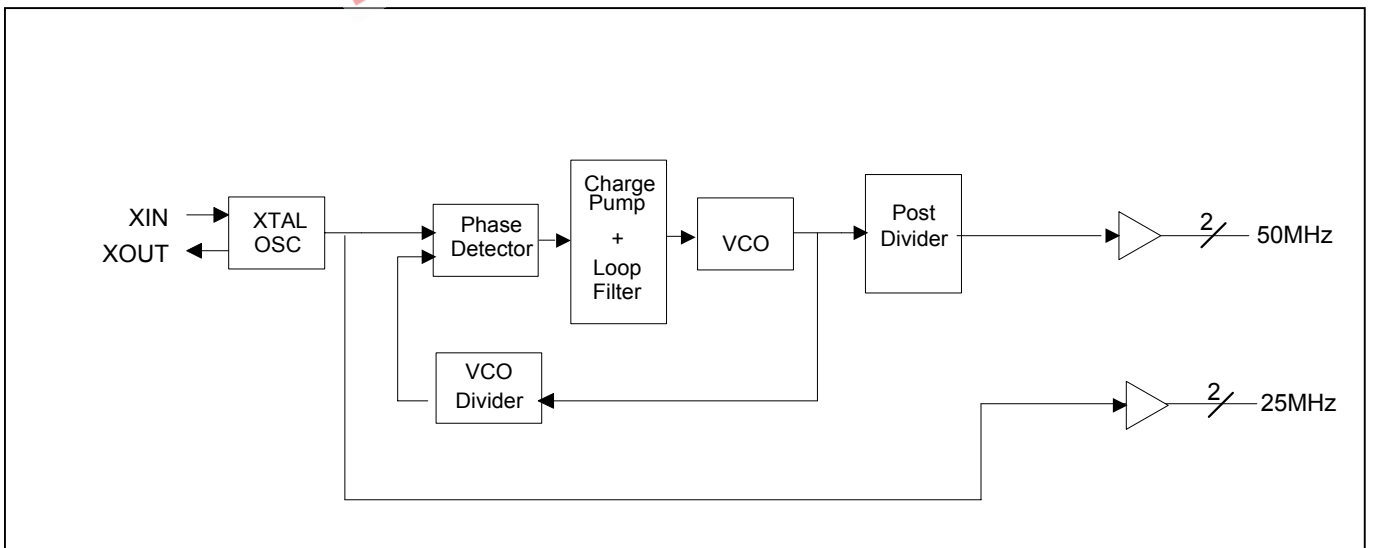
PIN CONFIGURATION



DESCRIPTION

The PLL650-07 is a low cost, low jitter, high performance clock synthesizer. With PhaseLink's proprietary analog Phase Locked Loop techniques, this device can produce multiple clock outputs from a 25.0MHz crystal or reference clock. This makes the PLL650-07 an excellent choice for systems requiring clocking for network chips and ASICs.

BLOCK DIAGRAM



LOW COST Network LAN Clock SOURCE

PIN DESCRIPTIONS

Name	Number	Type	Description
XOUT	1	O	Crystal output.
XIN	14	I	25MHz fundamental crystal input (20pF C _L parallel resonant) or clock input.
50MHz	4,6	O	50MHz outputs.
25MHz	8,10	O	25MHz outputs.
NC	12	-	No connection.
VDD	3,7	P	Power supply.
GND	5,9,11	P	Ground.
VDDA	13	P	Analog power supply
GNDA	2	P	Analog ground.

Electrical Specifications

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V _{DD}		4.6	V
Input Voltage, dc	V _I	-0.5	V _{DD} +0.5	V
Output Voltage, dc	V _O	-0.5	V _{DD} +0.5	V
Storage Temperature	T _S	-65	150	°C
Ambient Operating Temperature*	T _A	-40	85	°C
Junction Temperature	T _J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note:** Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. AC Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Frequency		10	25	27	MHz
Output Rise Time	0.8V to 2.0V with no load			1.5	ns
Output Fall Time	2.0V to 0.8V with no load			1.5	ns
Duty Cycle	@ 50% V _{DD}	45	50	55	%
Max. Absolute Jitter	Short term		±150		ps
Max. Jitter, cycle to cycle				80	ps

LOW COST Network LAN Clock SOURCE
3. DC Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operating Voltage	V_{DD}		2.97		3.63	V
Input High Voltage	V_{IH}			$V_{DD} / 2$		V
Input Low Voltage	V_{IL}			$V_{DD} / 2$	$V_{DD} / 2 - 1$	V
Input High Voltage	V_{IH}	For all normal input	2			V
Input Low Voltage	V_{IL}	For all normal input			0.8	V
Output High Voltage	V_{OH}	$I_{OH} = -25mA$	2.4			V
Output Low Voltage	V_{OL}	$I_{OL} = 25mA$			0.4	V
Output High Voltage At CMOS Level	V_{OH}	$I_{OH} = -8mA$	$V_{DD} - 0.4$			V
Operating Supply Current	I_{DD}	No Load		35		mA
Short-circuit Current	I_S			± 50		mA
Nominal output current	I_{out}	CMOS output level	35	40		mA
Nominal output current	I_{out}	TTL output level	20	25		mA

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LOW COST Network LAN Clock SOURCE

PACKAGE INFORMATION

14 PIN Narrow SOIC (mm)		
	SOIC	
Symbol	Min.	Max.
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	9.80	10.00
E	3.80	4.00
H	5.80	6.20
L	0.40	1.27
e	1.27 BSC	

ORDERING INFORMATION

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL650-07 S C

PART NUMBER	PLL650-07	S	C
		TEMPERATURE C=COMMERCIAL I=INDUSTRIAL	PACKAGE TYPE S=SOIC

Order Number	Marking	Package Option
PLL650-07SC-R	P650-07SC	SOIC - Tape and Reel
PLL650-07SC	P650-07SC	SOIC - Tube

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