MULTI-POWER SUPPLY

RV5VE0×××× SERIES

APPLICATION MANUAL

RICOH

MULTI-POWER SUPPLY

RV5VE0×××SERIES

OUTLINE

The RV5VE0×××series are multi-power supply ICs with high accuracy output voltage and detector threshold and with ultra low supply current by CMOS process. Each of these ICs consists of four voltage regulators,two voltage detectors and control switches.These ICs can achieve the construction of an ideal power supply system in accordance with the user's mask option.

Output Voltage and Detector Threshold can be independently set within each IC by laser trim. The package are of 16pin SSOP(0.8mm pitch) and 16pin SSOP(0.65mm pitch).

FEATURES

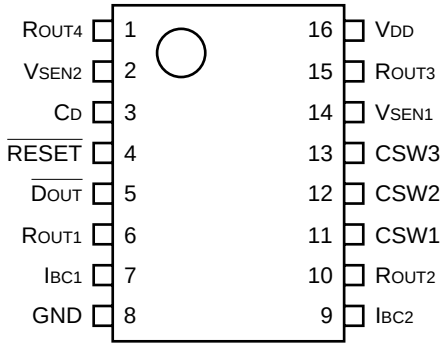
- Ultra-Low Supply Current
- Broad Operating Voltage Range ····· 1.5V to 10.0V
- High Accuracy Output Voltage and Detector Threshold ····· ±2.5%
- Output Voltage and Detector Threshold ····· Stepwise setting with a step of 0.1V is possible (refer to Selection Guide)
- Low Temperature-Drift Coefficients of Output Voltage and Detector Threshold ····· TYP. ±100ppm/°C
- Small Dropout Voltage ····· 50mV when I_{OUT} is 80mA (Regulators 1, 2)
- Small Package ····· 16pin SSOP (0.8mm pitch)
  16pin SSOP (0.65mm pitch)
- Direct connection to CPU is possible by an internal Level Shift Circuit.

APPLICATIONS

- Power source system for hand-held communication equipment such as cellular phones and cordless telephones.
- Power source system for battery-powered appliances.

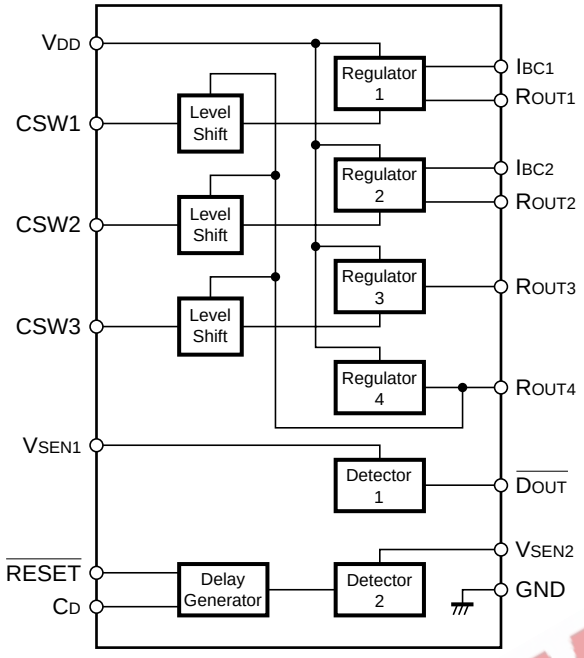
PIN CONFIGURATION

- **RV5VE001×**

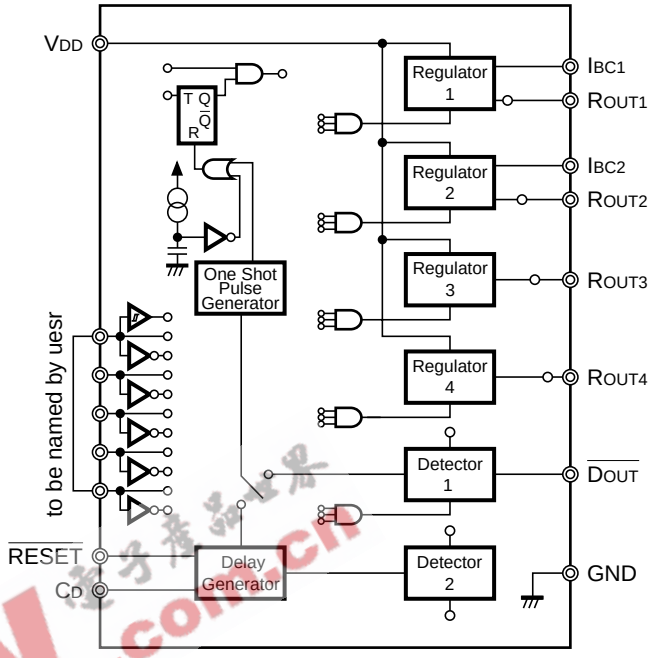


BLOCK DIAGRAMS

• **RV5VE001×**



• **RV5VE0×××(Optional Mask Version)**



SELECTION GUIDE

In the RV5VE0×××series, Standard ICs and Customized ICs by mask option (hereinafter Optional Mask Version ICs) are available at the user's request. Voltage settings for six circuits, four for Regulators and two for Detectors, can be designated.

Part Number is designated as follows :

RV5VE0××× – ×× ← Part Number

↑ ↑ ↑↑ ↑

a b c d e

Code	Contents
a	Designation of Package Type: V : 16pin SSOP (0.65mm pitch)
b	Serial Number for Multi-Power Supply IC (RV5VE) series:
c	Serial Number for Mask Version: ×1 for Standard ICs. Other numbers for Optional Mask Version ICs.
d	Serial Number for Voltage Setting: A to Z are assigned in alphabetical order. (except I,O,Q,X)
e	Designation of Taping Type: Ex. E1, E2 (refer to Taping Specifications)

PIN DESCRIPTION

• RV5VE001×(Standard ICs)

Pin No.	Symbol	Description
1	V_{OUT4}	Output Pin for Voltage Regulator 4.
2	V_{SEN2}	Sense Pin for Voltage Detector 2.
3	C_D	Pin for External Capacitor for Delay Time Setting of Voltage Detector 2.
4	$\overline{RESET}$	Output Pin of Voltage Detector 2. Nch Open Drain Output. “L” Outputat Detection.
5	$\overline{D_{OUT}}$	Output Pin of Voltage Detector 1. Nch Open Drain Output. “L” Output at Detection.
6	V_{OUT1}	Output Pin of Voltage Regulator 1. Connected to Collector of PNP Transistor.
7	I_{BC1}	Connected to Base of External PNP Transistor for Voltage Regulator 1 and controls Base Current.
8	GND	Ground Pin.
9	I_{BC2}	Connected to Base of External PNP Transistor for Voltage Regulator 2 and controls Base Current.
10	V_{OUT2}	Output Pin of Voltage Regulator 2. Connected to Collector of PNP Transistor.
11	CSW1	Control Switch Input Pin for turning Voltage Regulator 1 ON/OFF. Input level for this Input Pin is Active “H” .
12	CSW2	Control Switch Input Pin for turning Voltage Regulator 2 ON/OFF. Input level for this Input Pin is Active “H”
13	CSW3	Control Switch Input Pin for turning Voltage Regulator 3 ON/OFF. Input level for this Input Pin is Active “H” .
14	V_{SEN1}	Sense Pin of Voltage Detector 1.
15	V_{OUT3}	Output Pin of Voltage Regulator 3.
16	V_{DD}	V_{DD} Pin.

• RV5VE0×××(Optional Mask Version ICs)

Pin No.	Symbol	Description
2	To be named by User	5 Pins Nos. 2, 11, 12, 13 and 14 can be designated as Input Pins by User's choice. Refer to Optional Mask Version Guide. Pins other than the above 5 Pins can be selected from the same pins as those used in R×5VE001×(Standard ICs)
11		
12		
13		
14		

OPTIONAL MASK VERSION GUIDE

User can designate an optional mask version in accordance with the following Optional Mask Version Guide:

Item	Description
Sense Pins of Voltage Detectors 1, 2	• sense Pins of Voltage Detectors 1, 2 can be connected to Output ROUT1, ROUT2, ROUT3, ROUT4 of Voltage Regulators, or VDD.
ON/OFF Control of Regulators and Detectors	• ON/OFF Control of Voltage Regulators 1 to 4 and Voltage Detector 1 can be performed by 3 INPUT AND Gate. • ON/OFF Control of Voltage Detector 2 can be directly performed.
ON/OFF Control by Toggle Input (only Pin 11)	• ON/OFF Control of 4 Voltage Regulators and 2 Voltage Detectors can be performed by AND Gate of Toggle Input and Level Input. • Edge Trigger Flip-Flop (Rise Edge Operation) is reset and Initialized at the rise of power source or at the detection operation of Voltage Detector 1 or 2. • Flip-Flop can be reset by one shot pulse at the detection of Voltage Detector 1 or 2, or the reset state can be maintained during the detection operation.
Pins by User's Choice	• Five Input Pins are available as User's Pins as shown in the TABLE shown below. • ON/OFF Control Input Pins for Regulators and detectors. • Sense Pins of Voltage Detectors 1,2. • Active “H” Input or Active “L” Input can be selected.
Output of Voltage Detectors 1, 2	• RESET Output and DOUT Output, which are output from Voltage Detectors 1, 2, can be set at “L” or “H” at the time of the detection. • RESET Output and DOUT Output, which are output from Voltage Detectors 1, 2,can be set at “L” or “H” at the time of OFF by ON/OFF Control. • Output Signals of Voltage Detectors 1, 2 can perform ON/OFF control of Voltage Regulators 1 to 4.

• Functions of Input Pins by User' Choice

Pin No.	Symbol	Functions
2	To be named by User	Control Switch of Each Circuit, Sense Pin of Voltage Detector 1 or 2.
11		Control Switch of Each Circuit, Schmitt trigger input possible.
12		Control Switch of Each Circuit only.
13		Control Switch of Each Circuit only.
14		Control Switch of Each Circuit, Sense Pin of Voltage Detector 1 or 2.

DESCRIPTION OF EACH CIRCUIT

1. Voltage Regulators 1,2

- Voltage Regulators 1, 2 are linear regulators which can be constructed of external PNP Transistor, and are capable of obtaining a large output current by a small Dropout Voltage.
- Output Voltage of each of Voltage Regulators 1, 2 can be set stepwise with a step of 0.1V in the range of 3V to 6V by laser trim.
- Voltage Regulators 1, 2 can be turned ON/OFF by Control Pins.
- Use External PNP Transistor of a low saturation type, with an h_{FE} of 100 or more.
- Use Voltage Regulators 1, 2 with the attachment of a Capacitor with a capacitance of 10µF or more to the Output Pins.

2. Voltage Regulators 3,4

- Voltage Regulators 3, 4 are CMOS type linear regulators and have the same structure as those of Voltage Regulators R×5RL and R×5RE series.
- Output Voltage of each of Voltage Regulators 3, 4 can be set stepwise with a step of 0.1V in the range of 2V to 6V by laser trim.
- Voltage Regulators 3, 4 can be turned ON/OFF by Control Pins.

3. Voltage Detector 1

- When Voltage Detector 1 detects the lowering of V_{SEN1}, the level of the output of Voltage Detector 1 becomes "L" level. The output of Voltage Detector 1 is Nch Open Drain Output.
- Voltage Detector 1 can be set as follows by optional mask:

1. ON/OFF Control of Voltage Detector 1.
2. Output of Voltage Detector 1 at the detection can be set at "L" level or "H" level.
3. Output of Voltage Detector 1 at OFF can be set at "L" level or "H" level.
4. Sense Pins of Voltage Detectors 1, 2 can be connected to Output R_{OUT1}, R_{OUT2}, R_{OUT3}, R_{OUT4} of Voltage Regulators or V_{DD} within the IC.

4. Voltage Detector 2

- When Voltage Detector 2 detects the lowering of V_{SEN2}, the level of the output of Voltage Detector 2 becomes "L" level. The output of Voltage Detector 2 is Nch Open Drain Output.
- Voltage Detector 2 can set Reset Delay Time. Delay Time can be set in accordance with the capacitance C_D of External Capacitor as shown on the following pages.
- Voltage detector 2 can be set as follows by optional mask:

1. ON/OFF Control of Voltage Detector 2.
2. Output of Voltage Detector 2 at the detection can be set at "L" level or "H" level.
3. Output of Voltage Detector 2 at OFF can be set at "L" level or "H" level.
4. Sense Pins of Voltage Detectors 2 can be connected to Output R_{OUT1}, R_{OUT2}, R_{OUT3}, R_{OUT4} of Voltage Regulators or V_{DD} within the IC.

• Formula for calculating Reset Delay Time is

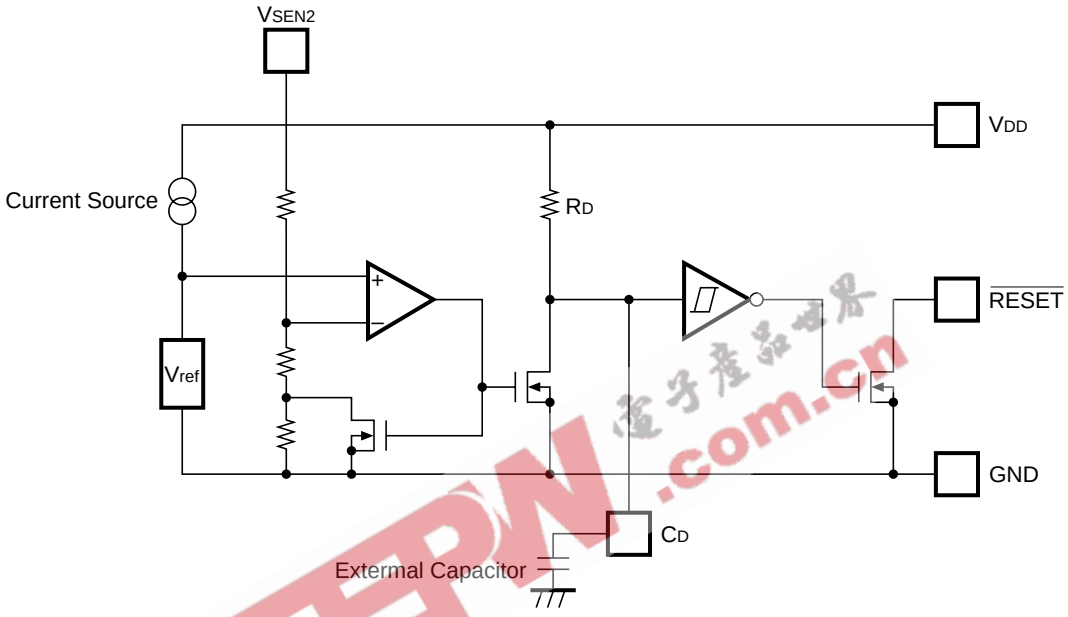
$t_D = 0.69 \times R_D \times C_D$

wherein R_D is the resistance of a built-in resistor and can be set at 1MΩ in IC, so that the above formula is:

$t_D = 0.69 \times 10^6 \times C_D$

Voltage Detector with Delay Circuit is constructed as shown below.

• Block Diagram of Voltage Detector with delay Circuit.



5. Main Power Source Control (in the case of Optional Mask Version)

• This IC includes built-in Edge Trigger Flip-Flop (Rising Edge Operation) and AND Gate, so that Main Power Source of any instruments can be turned ON/OFF by "AND" of Toggle Input and Level Input.

• Edge Trigger Flip-Flop is reset by One Shot Pulse Generator when Voltage Detector 1 or 2 detects the lowering of the voltage. This Flip-Flop can be continuously reset during the detection.

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	+12	V
V_{OUT}	Output Voltage	−0.3 to V_{IN}+0.3	V
I_{OUT}	Output Current	300	mA
$P_{D}1$	Power Dissipation1 (16pin SSOP (0.8mm pitch))	500	mW
$P_{D}2$	Power Dissipation2 (16pin SSOP (0.65mm pitch))	470	mW
Topt	Operating Temperature Range	−30 to +80	°C
Tstg	Storage Temperature Range	−40 to +125	°C
Tsolder	Lead Temperature(Soldering)	260°C 10s	

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum ratings are threshold limit values that must not be exceeded even for an instant under any conditions. Moreover, such values for any two items must not be reached simultaneously. Operation above these absolute maximum ratings may cause degradation or permanent damage to the device. These are stress ratings only and do not necessarily imply functional operation below these limits.

OVERALL CHARACTERISTICS

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{DD}	Operationg Voltage Range		1.5		10.0	V
$R_{OUT}1,2$	Output Voltage Setting Range 1	Step of 0.1V	3.0		6.0	V
$R_{OUT}3,4$	Output Voltage Setting Range 2	Step of 0.1V	2.0		6.0	V
$-V_{DET}$	Detector Threshold Setting Range	Step of 0.1V	2.0		6.0	V

• Electrical Characteristics of R×5VE001×

The following three types of ICs are available as Standard ICs.The details of these ICs are shown in the section of Electrical Characteristics on the following pages:

• List of Standard Voltage Settings

Type Number	R×5VE001A	R×5VE001B	R×5VE001C
Output Voltage of Regulator 1 to 4	5.0V	4.0V	3.0V
Threshold Voltage of Detector 1	5.4V	4.4V	3.4V
Threshold Voltage of Detector 2	4.5V	3.5V	2.5V
Conditions for Input Voltage	6.0V	4.8V	3.6V

• **RV5VE001A**

Voltage Regulators 1, 2 [RV5VE001A]

Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
$V_{OUT1,2}$	Output Voltage		4.875	5.000	5.125	V
$I_{SS1,2}$	Quiescent Current	I_{OUT}=0mA			100	µA
Iopr1,2	Supply Current	I_{OUT}=80mA			1	mA
$V_{DIF1,2}$	Dropout Voltage	$V_{OUT1,2}$=5.0V,I_{OUT}=80mA		0.05	0.3	V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$V_{OUT1,2}$=5.0V 1mA≤I_{OUT}≤80mA			50	mV
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$V_{OUT1,2}$+0.3V≤V_{IN}≤10.0V		0.05	0.3	%/V
RR	Ripple Rejection	f=120Hz,Ripple 0.5Vrms	40	60		dB
Ilim1,2	Current Limit	Base Current of $I_{B1,2}$of PNP Transistor	3		10	mA
$\frac{\Delta V_{OUT}}{\Delta Topt}$	Output Voltage Temperature Coefficient			±100		ppm/°C

(Note 1) Unless otherwise provided, V_{DD} = 6.0V, I_{OUT} = 50mA, Co = 10µF, Rbe = 100kΩ.
(Note 2) Use External Transistor with h_{FE} ≥ 100.
(Note 3) Quiescent Current = Operating Current of Regulators 1, 2 + 0.6/Rbe.
(Note 4) Supply Current = Quiescent (No Load) Current + Load Current/h_{FE}.

Voltage Regulator 3 [RV5VE001A]

Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{OUT3}	Output Voltage		4.875	5.000	5.125	V
I_{SS3}	Supply Current			5.0	10.0	µA
V_{DIF3}	Dropout Voltage	V_{OUT3}=5.0V,I_{OUT}=50mA			0.3	V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	V_{OUT3}=5.0V 1mA≤I_{OUT}≤50mA			50	mV
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	V_{OUT3}+0.5V≤V_{IN}≤10.0V		0.05	0.3	%/V
Ilim3	Current Limit		100		300	mA
$\frac{\Delta V_{OUT}}{\Delta Topt}$	Output Voltage Temperature Coefficient			±100		ppm/°C

(Note) Unless otherwise provided, V_{DD} = 6.0V, I_{OUT} = 30mA

Voltage Regulator 4 [RV5VE001A]

Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{OUT4}	Output Voltage		4.875	5.000	5.125	V
I_{SS4}	Supply Current			1.3	3.9	µA
V_{DIF4}	Dropout Voltage	V_{OUT4}=5.0V,I_{OUT}=20mA			0.3	V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	V_{OUT4}=5.0V 1mA≤I_{OUT}≤20mA			50	mV
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	V_{OUT4}+0.5V≤V_{IN}≤10.0V		0.05	0.3	%/V
Ilim4	Current Limit		100		300	mA
$\frac{\Delta V_{OUT}}{\Delta Topt}$	Output Voltage Temperature Coefficient			±100		ppm/°C

(Note) Unless otherwise provided, V_{DD} = 6.0V, I_{OUT} = 10mA

Voltage Detectors 1,2 [RV5VE001A]

Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
$-V_{DET1}$	Detector Threshold 1	Voltage Detector 1	5.265	5.400	5.535	V
$-V_{DET2}$	Detector Threshold 2	Voltage Detector 2	4.388	4.500	4.612	V
V_{HYS}	Detector Threshold Hysteresis			($-V_{DET}$) ×0.05		V
I_{SS5}	Supply Current	Voltage Detector 1,V_{DD}=6.0V		1.3	3.9	µA
I_{SS6}		Voltage Detector 2,V_{DD}=6.0V		1.5	4.5	µA
I_{OUT}	Output Current	V_{DS}=0.5V, V_{DD}=1.5V		1.5		mA
		V_{DS}=0.5V, V_{DD}=6.0V		11.6		
R_D	Output Delay Resistor	Voltage Detector 2 only	0.5	1.0	2.0	MΩ
I_{SEN}	Sense Pin Input Current	V_{SEN}=6.0V		0.5	2	µA
$\frac{\Delta V_{DET}}{\Delta Topt}$	Detector Threshold Temperature Coefficient			±100		ppm/°C

(Note) Unless otherwise provided, V_{DD} = 6.0V.

Input Pins [RV5VE001A]

Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
I_{leak}	Input Leakage Current		–1		1	µA
V_{IL}	Control Switch Low Level Input Voltage	CSW1 to 4	0		0.8	V
V_{IH}	Control Switch High Level Input Voltage	CSW1 to 4	2.4		V_{DD}	V
V_{SIL}	Schmitt Trigger Low Level Input Voltage	Optional				V
V_{SIH}	Schmitt Trigger High Level Input Voltage	Optional				V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Optional				V

(Note) Unless otherwise provided, V_{DD} = 6.0V.

• **RV5VE001B**

Voltage Regulators 1, 2 [RV5VE001B]

Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
$V_{OUT1,2}$	Output Voltage		3.900	4.000	4.100	V
$I_{SS1,2}$	Quiescent Current	I_{OUT}=0mA			100	µA
Iopr1,2	Supply Current	I_{OUT}=80mA			1	mA
$V_{DIF1,2}$	Dropout Voltage	$R_{OUT1,2}$=4.0V,I_{OUT}=80mA		0.05	0.3	V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$R_{OUT1,2}$=4.0V 1mA≤I_{OUT}≤80mA			50	mV
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$R_{OUT1,2}$+0.3V≤V_{IN}≤10.0V		0.05	0.3	%/V
RR	Ripple Rejection	f=120Hz,Ripple 0.5Vrms	40	60		dB
Ilim1,2	Current Limit	Base Current of $I_{B1,2}$of PNP Transistor	3		10	mA
$\frac{\Delta V_{OUT}}{\Delta Topt}$	Output Voltage Temperature Coefficient			±100		ppm/°C

(Note 1) Unless otherwise provided, V_{DD} = 4.8V, I_{OUT} = 50mA, Co = 10µF, Rbe = 100kΩ.
(Note 2) Use External Transistor with h_{FE} ≥ 100.
(Note 3) Quiescent Current = Operating Current of Regulators 1, 2 + 0.6/Rbe.
(Note 4) Supply Current = Quiescent (No Load) Current + Load Current/h_{FE}.

Voltage Regulator 3 [RV5VE001B]

Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{OUT3}	Output Voltage		3.900	4.000	4.100	V
I_{SS3}	Supply Current			5.0	10.0	µA
V_{DIF3}	Dropout Voltage	R_{OUT3}=4.0V,I_{OUT}=43mA			0.3	V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	R_{OUT3}=4.0V 1mA≤I_{OUT}≤43mA			50	mV
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	R_{OUT3}+0.5V≤V_{IN}≤10.0V		0.05	0.3	%/V
Ilim3	Current Limit		100		300	mA
$\frac{\Delta V_{OUT}}{\Delta Topt}$	Output Voltage Temperature Coefficient			±100		ppm/°C

(Note) Unless otherwiseprovided, V_{DD} = 4.8V, I_{OUT} = 30mA.

Voltage Regulator 4 [RV5VE001B]

Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{OUT4}	Output Voltage		3.900	4.000	4.100	V
I_{SS4}	Supply Current			1.3	3.9	µA
V_{DIF4}	Dropout Voltage	V_{OUT4}=4.0V,I_{OUT}=17.5mA			0.3	V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	V_{OUT4}=4.0V 1mA≤I_{OUT}≤17.5mA			50	mV
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	V_{OUT4}+0.5V≤V_{IN}≤10.0V		0.05	0.3	%/V
Ilim4	Current Limit		100		300	mA
$\frac{\Delta V_{OUT}}{\Delta Topt}$	Output Voltage Temperature Coefficient			±100		ppm/°C

(Note) Unless otherwise provided, V_{DD} = 4.8V, I_{OUT} = 10mA

Voltage Detectors 1,2 [RV5VE001B]

Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
$-V_{DET1}$	Detector Threshold 1	Voltage Detector 1	4.290	4.400	4.510	V
$-V_{DET2}$	Detector Threshold 2	Voltage Detector 2	3.413	3.500	3.587	V
V_{HYS}	Detector Threshold Hysteresis			($-V_{DET}$) ×0.05		V
I_{SS5}	Supply Current	Voltage Detector 1,V_{DD}=4.8V		1.2	3.6	µA
I_{SS6}		Voltage Detector 2,V_{DD}=4.8V		1.4	4.2	µA
I_{OUT}	Output Current	V_{DS}=0.5V, V_{DD}=1.5V		1.5		mA
		V_{DS}=0.5V, V_{DD}=4.8V		9.0		
R_D	Output Delay Resistor	Voltage Detector 2 only	0.5	1.0	2.0	MΩ
I_{SEN}	Sense Pin Input Current	V_{SEN}=4.8V		0.4	1.6	µA
$\frac{\Delta V_{DET}}{\Delta Topt}$	Detector Threshold Temperature Coefficient			±100		ppm/°C

(Note) Unless otherwise provided, V_{DD} = 4.8V.

Input Pins [RV5VE001B]

Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
I_{leak}	Input Leakage Current		–1		1	µA
V_{IL}	Control Switch Low Level Input Voltage	CSW1 to 4	0		0.8	V
V_{IH}	Control Switch High Level Input Voltage	CSW1 to 4	2.0		V_{DD}	V
V_{SIL}	Schmitt Trigger Low Level Input Voltage	Optional				V
V_{SIH}	Schmitt Trigger High Level Input Voltage	Optional				V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Optional				V

(Note) Unless otherwise provided, V_{DD} = 4.8V.

• **RV5VE001C**

Voltage Regulators 1, 2 [RV5VE001C]

Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
$V_{OUT1,2}$	Output Voltage		2.925	3.000	3.075	V
$I_{SS1,2}$	Quiescent Current	I_{OUT}=0mA			100	µA
Iopr1,2	Supply Current	I_{OUT}=80mA			1	mA
$V_{DIF1,2}$	Dropout Voltage	$V_{OUT1,2}$=3.0V,I_{OUT}=80mA		0.05	0.3	V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$V_{OUT1,2}$=3.0V 1mA≤I_{OUT}≤80mA			50	mV
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$V_{OUT1,2}$+0.3V≤V_{IN}≤10.0V		0.05	0.3	%/V
RR	Ripple Rejection	f=120Hz,Ripple 0.5Vrms	40	60		dB
Ilim1,2	Current Limit	Base Current of $I_{B1,2}$of PNP Transistor	3		10	mA
$\frac{\Delta V_{OUT}}{\Delta Topt}$	Output Voltage Temperature Coefficient			±100		ppm/°C

(Note 1) Unless otherwise provided, V_{DD} = 3.6V, I_{OUT} = 50mA, Co = 10µF, Rbe = 100kΩ.
(Note 2) Use External Transistor with h_{FE} ≥ 100.
(Note 3) Quiescent Current = Operating Current of Regulators 1, 2 + 0.6/Rbe.
(Note 4) Supply Current = Quiescent (No Load) Current + Load Current/h_{FE}.

Voltage Regulator 3 [RV5VE001C]

Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{OUT3}	Output Voltage		2.925	3.000	3.075	V
I_{SS3}	Supply Current			5.0	10.0	µA
V_{DIF3}	Dropout Voltage	V_{OUT3}=3.0V,I_{OUT}=35mA			0.3	V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	V_{OUT3}=3.0V 1mA≤I_{OUT}≤35mA			50	mV
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	V_{OUT3}+0.5V≤V_{IN}≤10.0V		0.05	0.3	%/V
Ilim3	Current Limit		100		300	mA
$\frac{\Delta V_{OUT}}{\Delta Topt}$	Output Voltage Temperature Coefficient			±100		ppm/°C

(Note) Unless otherwise provided, V_{DD} = 3.6V, I_{OUT} = 30mA

Voltage Regulator 4 [RV5VE001C]

Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{OUT4}	Output Voltage		2.925	3.000	3.075	V
I_{SS4}	Supply Current			1.1	3.3	µA
V_{DIF4}	Dropout Voltage	V_{OUT4}=3.0V,I_{OUT}=15mA			0.3	V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	V_{OUT4}=3.0V 1mA≤I_{OUT}≤15mA			50	mV
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	V_{OUT4}+0.5V≤V_{IN}≤10.0V		0.05	0.3	%/V
Ilim4	Current Limit		100		300	mA
$\frac{\Delta V_{OUT}}{\Delta Topt}$	Output Voltage Temperature Coefficient			±100		ppm/°C

(Note) Unless otherwise provided, V_{DD} = 3.6V, I_{OUT} = 10mA

Voltage Detectors 1,2 [RV5VE001C]

Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
$-V_{DET1}$	Detector Threshold 1	Voltage Detector 1	3.315	3.400	3.485	V
$-V_{DET2}$	Detector Threshold 2	Voltage Detector 2	2.438	2.500	2.562	V
V_{HYS}	Detector Threshold Hysteresis			($-V_{DET}$) ×0.05		V
I_{SS5}	Supply Current	Voltage Detector 1,V_{DD}=3.6V		1.1	3.3	µA
I_{SS6}		Voltage Detector 2,V_{DD}=3.6V		1.3	3.9	µA
I_{OUT}	Output Current	V_{DS}=0.5V, V_{DD}=1.5V		1.5		mA
		V_{DS}=0.5V, V_{DD}=3.6V		6.5		
R_D	Output Delay Resistor	Voltage Detector 2 only	0.5	1.0	2.0	MΩ
I_{SEN}	Sense Pin Input Current	V_{SEN}=3.6V		0.3	1.2	µA
$\frac{\Delta V_{DET}}{\Delta Topt}$	Detector Threshold Temperature Coefficient			±100		ppm/°C

(Note) Unless otherwise provided, V_{DD} = 6.0V.

Input Pins [RV5VE001C]

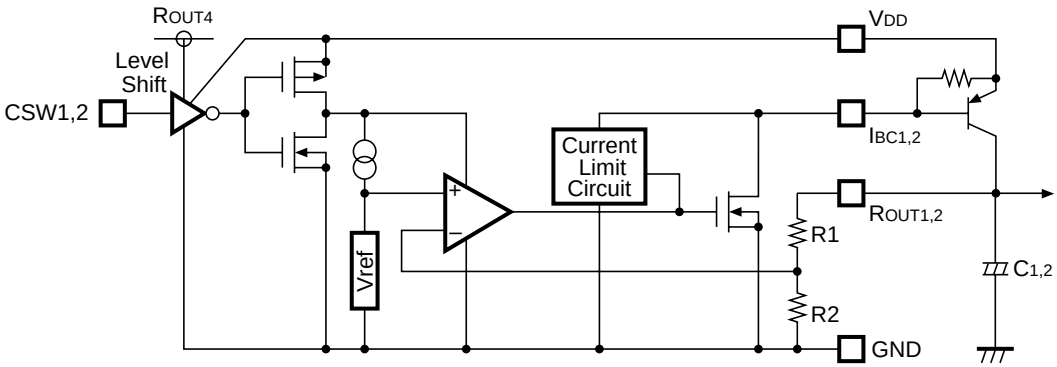
Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
Ileak	Input Leakage Current		–1		1	µA
VIL	Control Switch Low Level Input Voltage	CSW1 to 4	0		0.6	V
VIH	Control Switch High Level Input Voltage	CSW1 to 4	1.6		VDD	V
VSIL	Schmitt Trigger Low Level Input Voltage	Optional				V
VSIH	Schmitt Trigger High Level Input Voltage	Optional				V
VHYS	Schmitt Trigger Hysteresis Voltage	Optional				V

(Note) Unless otherwise provided, VDD = 3.6V.

OPERATION

• Regulators 1,2

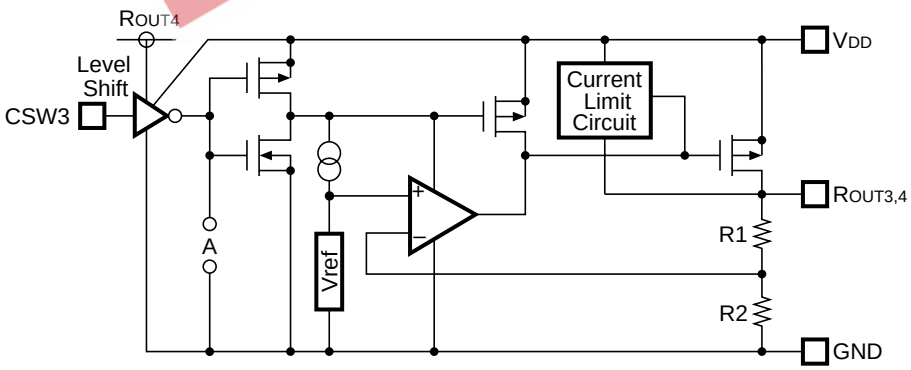


Each of Regulators 1 and 2 is operating with an external PNP transistor as shown in the above figure. Regulators 1 and 2 divide Output Voltage VOUT by Feed-back Registers R1 and R2, and the divided voltage at the node between Registers R1 and R2 is compared with the reference voltage by Error Amplifier, so that the base current of the PNP transistor is adjusted, and a constant voltage is output. The output current from each of Regulators 1 and 2 is monitored by Current Limitter, and when the output current exceeds a limit current, Current Limitter limits the base current of the PNP transistor to the specified limit current.

The level of input signals to CSW 1, 2 is set at the same level as the output voltage level of ROUT4 by built-in level shift circuit.

Phase compensation is made externally with C1,2.

• Regulators 3,4

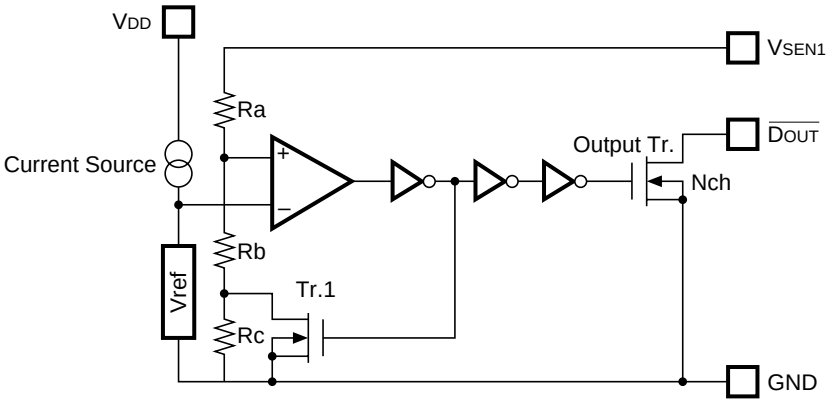


Regulators 3 and 4 divide Output Voltage VOUT by feed-back Registers R1 and R2, and the divided voltage at the node between Registers R1 and R2 is compared with the reference voltage by Error Amplifier, so that a constant voltage is output. The output current from each of Regulators 3 and 4 is monitored by Current Limitter, and when the output current exceeds a limit current, Current Limitter limits the output current to the limit current.

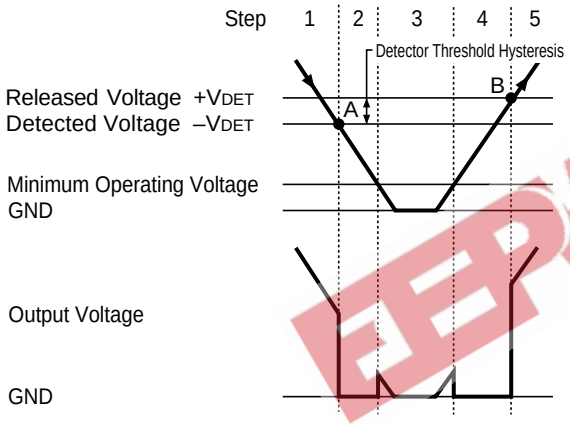
Regulator 4 is connected at Point to the GND in the above figure, so that Regulator 4 is always in operation.

The level of input signals to CSW1, 2 is set at the same level as the output voltage level of ROUT4 by built-in level shift circuits.

• **Detector 1**



Operation Diagram



Step		Step 1	Step 2	Step 3	Step 4	Step 5
Comparator(+)Pin Input Voltage		I	II	II	II	I
Comparator Output		H	L	L	L	H
Tr. 1		OFF	ON	ON	ON	OFF
Output Tr.	Nch	OFF	ON	Indefinite	ON	OFF

I. $\dfrac{Rb + Rc}{Ra + Rb + Rc} \cdot V_{DD}$

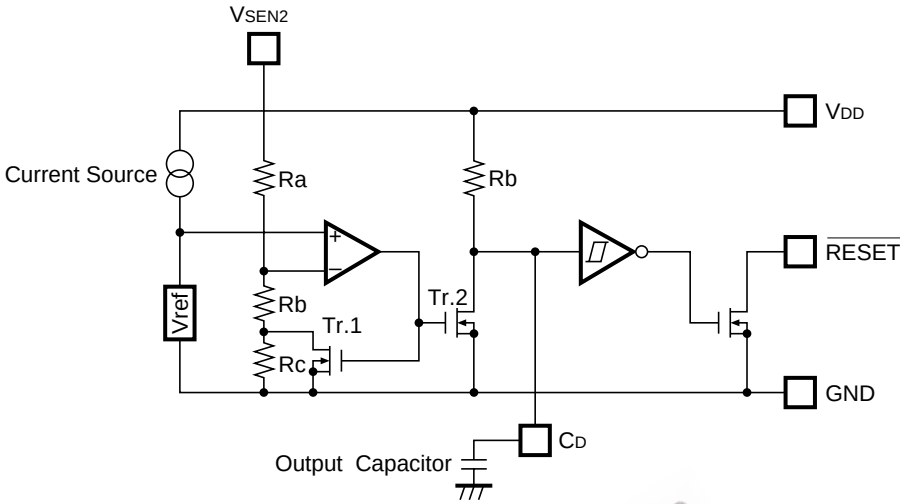
II. $\dfrac{Rb}{Ra + Rb} \cdot V_{DD}$

Step of Operation

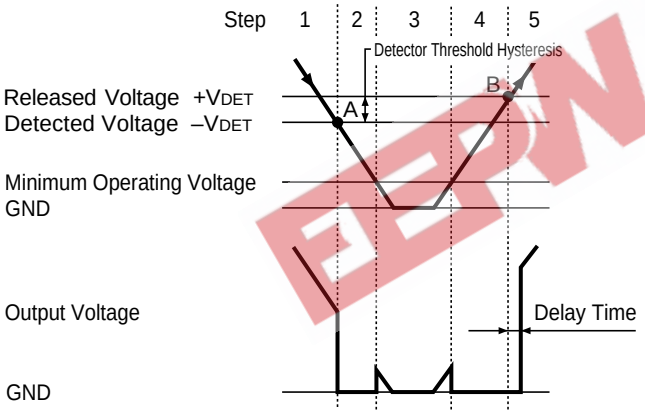
The following descriptions deal with VDD pin and VSEN1 pin as connected each other, but Detector 1 can be detected the different voltage from VDD through VSEN1 pin.

Step 1. Output Voltage is equal to Pull-up Voltage.
Step 2. When Input Voltage (VSEN1)reaches the state of Vref ≥ VSEN1 · (Rb+Rc)/(Ra+Rb+Rc)at Point A (Detected Voltage–VDET), the output of Comparator is reversed, so that Output Voltage becomes GND.
Step 3. Output Voltage becomes indefinite when Power Source Voltage (VDD) is smaller than Minimum Operating Voltage. When the output is pulled-up,VDD is output.
Step 4. Output Voltage becomes equal to GND.
Step 5. When Input Voltage to (VSEN1) reaches the state of Vref ≤ VSEN1 · Rb/(Ra + Rb) at Point B (Released Voltage+VDET), the output of Comparator is reversed, so that Output Voltage becomes equal to Pulled-up Voltage.

• **Detector 2**



Operation Diagram



Step		Step 1	Step 2	Step 3	Step 4	Step 5
Comparato (+) Pin Input Voltage		I	II	II	II	I
Comparator Output		H	L	L	L	H
Tr. 1		OFF	ON	ON	ON	OFF
Output Tr.	Nch	OFF	ON	Indefinite	ON	OFF

$$\text{I.}\quad \frac{Rb + Rc}{Ra + Rb + Rc} \cdot V_{DD}$$

$$\text{II.}\quad \frac{Rb}{Ra + Rb} \cdot V_{DD}$$

Step of Operation

The following descriptions deal with V_{DD} pin and V_{SEN2} pin as connected each other, but Detector 2 can be detected the different voltage from V_{DD} through V_{SEN2} pin.

Step 1. Output Voltage is equal to Pull-up Voltage.

Step 2. When Input Voltage (V_{SEN2}) reaches the state of Vref ≥ V_{SEN2} · (Rb+Rc)/(Ra+Rb+Rc)at Point A (Detected Voltage –V_{DET}), the output of Comparator is reversed, so that Output Voltage becomes GND. Discharging is performed from C_D pin connected to External Capacitor. No delay time is generated.

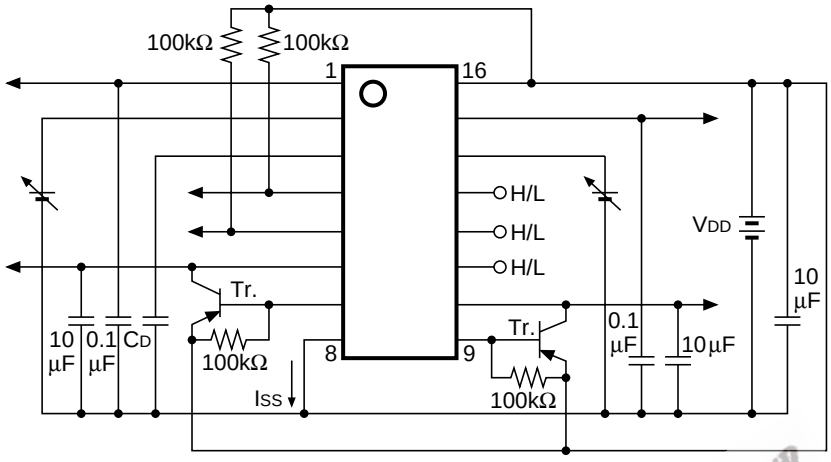
Step 3. Output Voltage becomes indefinite when Power Source Voltage (V_{DD}) is smaller than Minimum Operating Voltage. When the output is pulled-up,V_{DD} is output.

Step 4. Output Voltage becomes equal to GND.

Step 5. When Input Voltage (V_{SEN2}) reaches the state of Vref≤V_{SEN2} · Rb/(Ra + Rb) at Point B (Released Voltage +V_{DET}), the output of Comparator is reversed, and the External Capacitor is charged through C_D pin,so that Output Voltage becomes equal to Pulled-up Voltage after a delay timeT_D (= 0.69 × 10^6 × C_D).

TEST CIRCUITS (RV5VE001A,B,C)

• Test Circuit 1

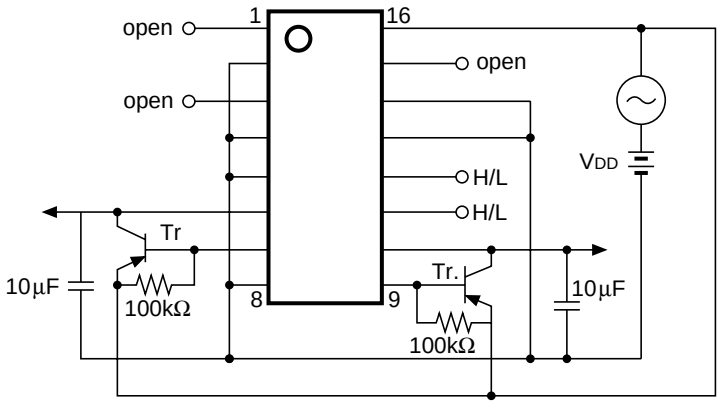


Tr : 2SB804
(h_{FE}=150)

· Output Voltage
· Quiescent Current
· Dropout Voltage
· Load Regulation
· Line Regulation
· Current Limit (Regulator 3, 4)
· Output Voltage Temperature Coefficient
· Detector Threshold
· Detector Threshold Hysteresis
· Output Voltage Transient Response

	CSW1	CSW2	CSW3
Regulator 1	H	L	L
Regulator 2	L	H	L
Regulator 3	L	L	H
Regulator 4	L	L	L
Detector 1	L	L	L
Detector 2	L	L	L

• Test Circuit 2

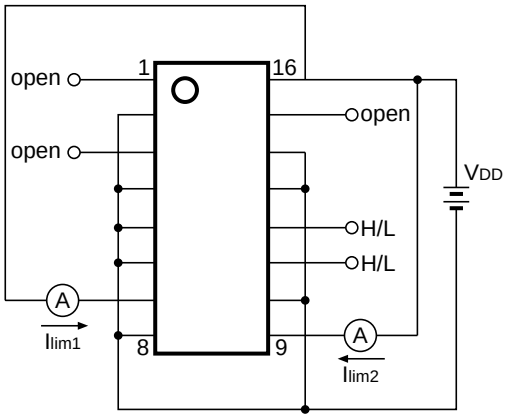


Tr : 2SB804
(h_{FE}=150)

· Ripple Rejection (Regulator 1, 2)

	CSW1	CSW2
Regulator 1	H	L
Regulator 2	L	H

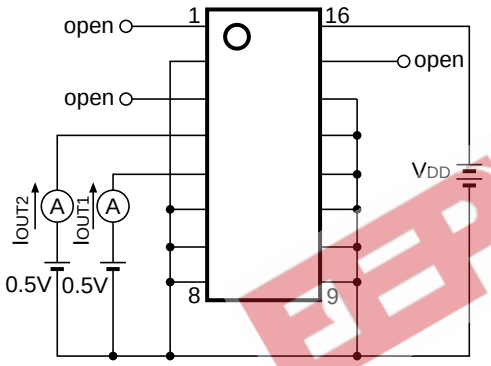
• **Test Circuit 3**



· Current Limit (Regulator 1, 2)

	CSW1	CSW2
Regulator 1	H	L
Regulator 2	L	H

• **Test Circuit 4**

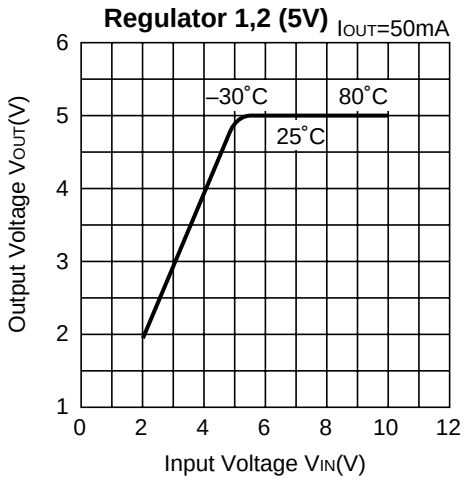


· Output Current (Detector 1, 2)

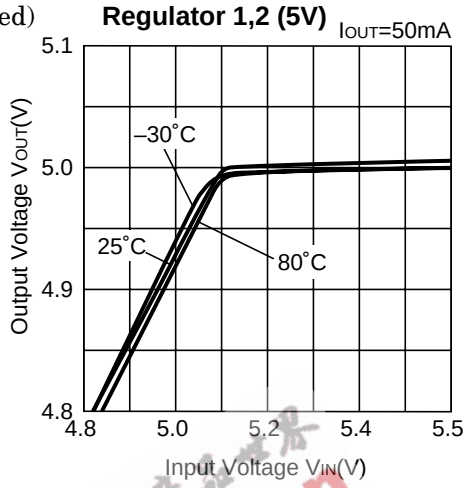
TYPICAL CHARACTERISTICS (RV5VE001A)

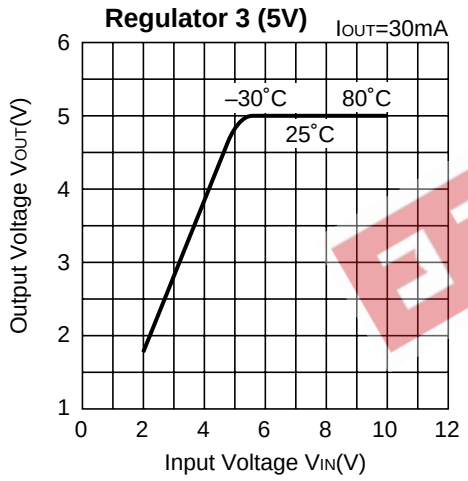
• **Regulator Section**

1) Output Voltage vs. Input Voltage

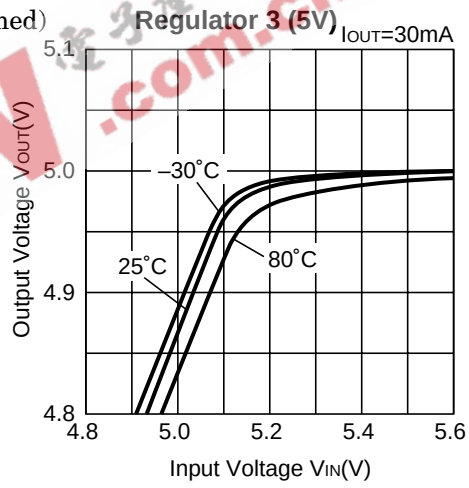


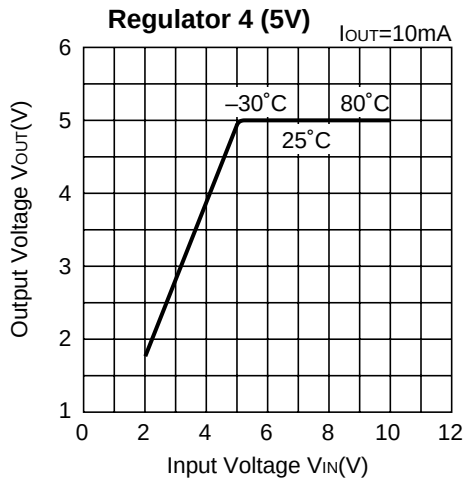
(zoomed)



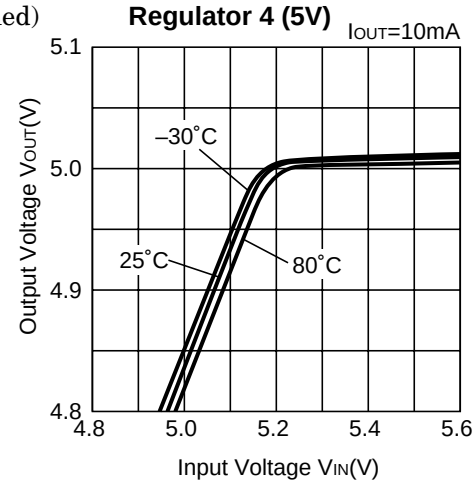


(zoomed)

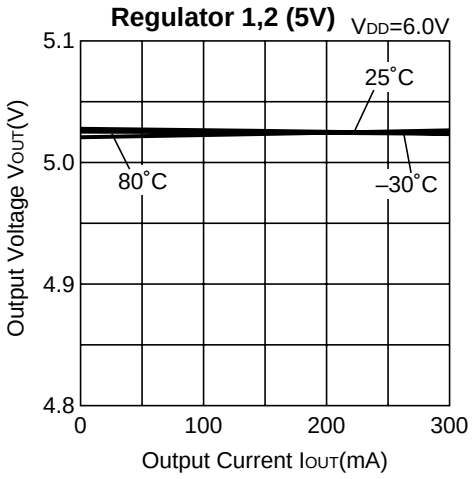


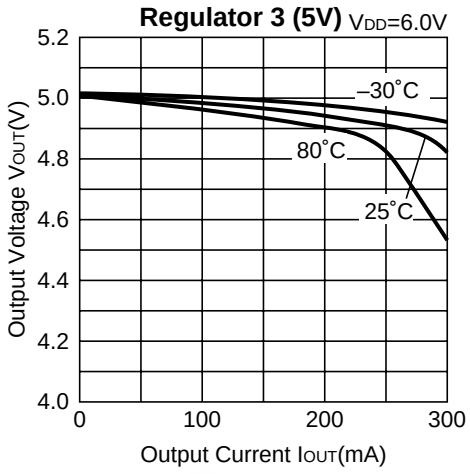


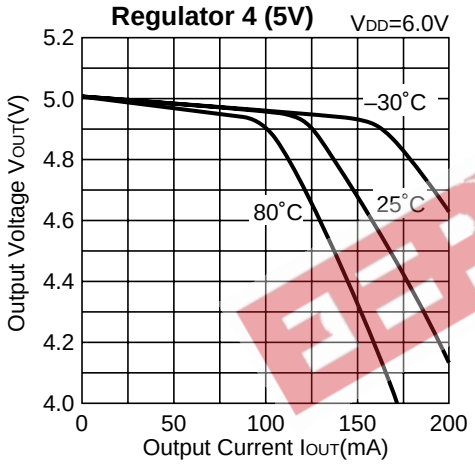
(zoomed)



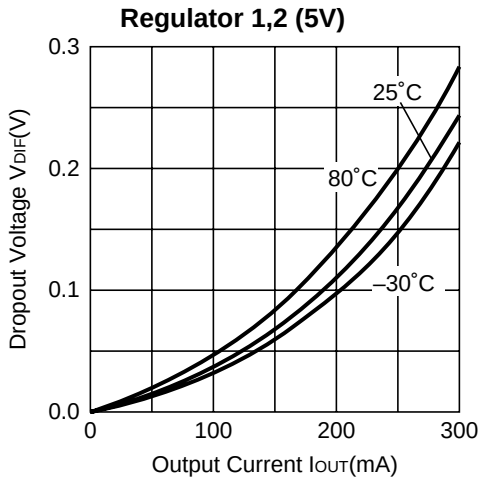
2) Output Voltage vs. Output Current

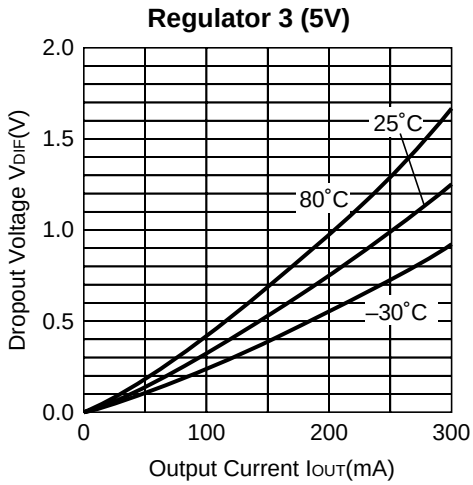


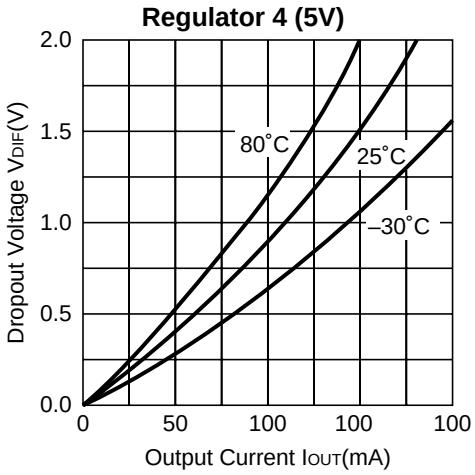




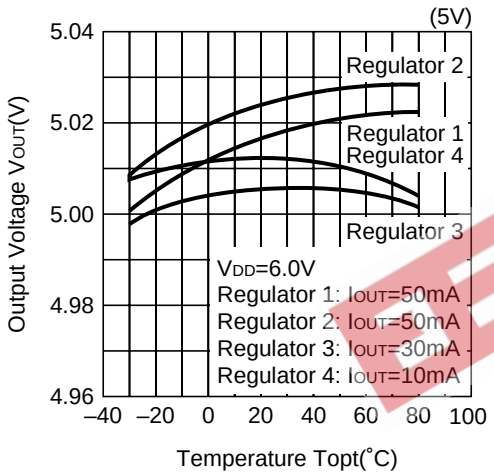
3) Dropout Voltage vs. Output Curret



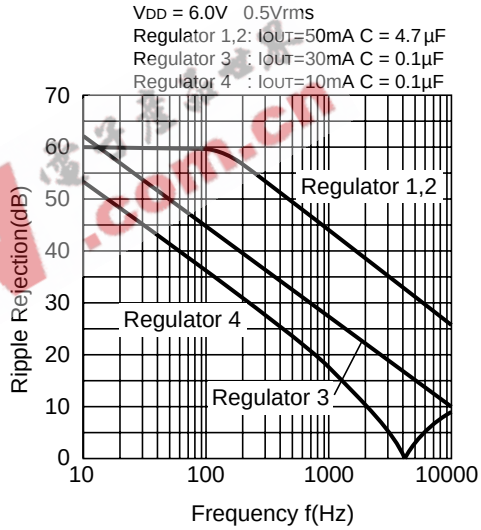




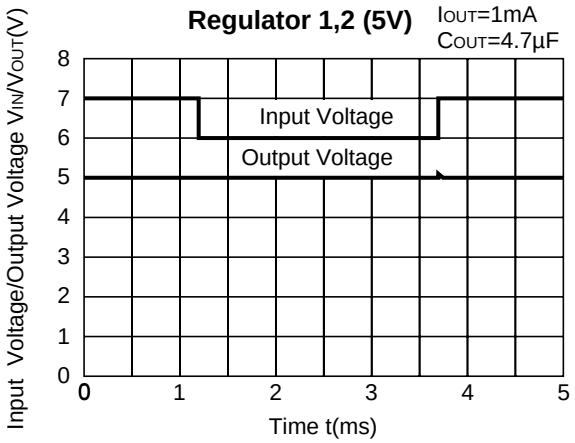
4) Output Voltage vs.Temperature

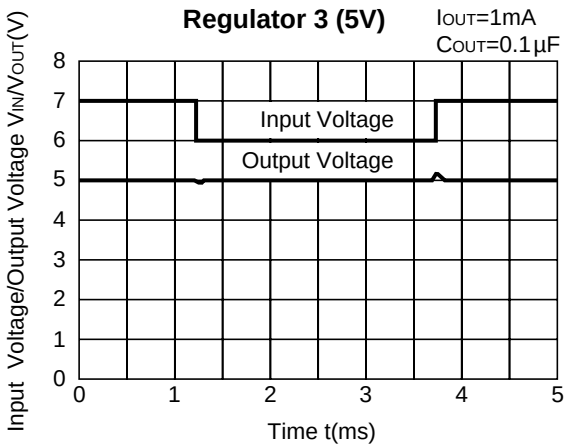


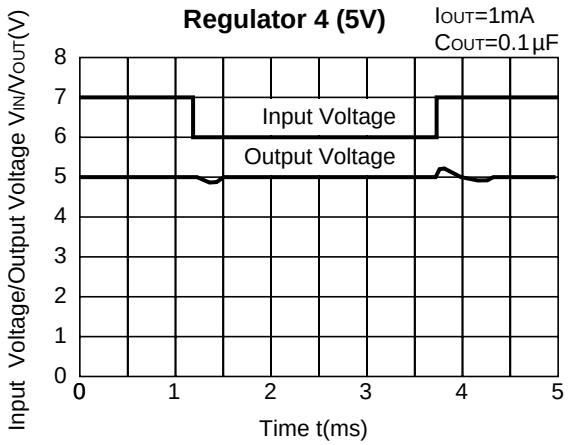
5) Ripple Rejection vs. Frequency



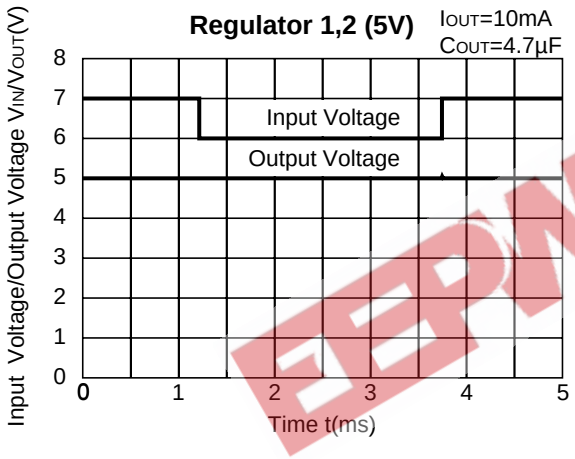
6) Line Transient Response 1

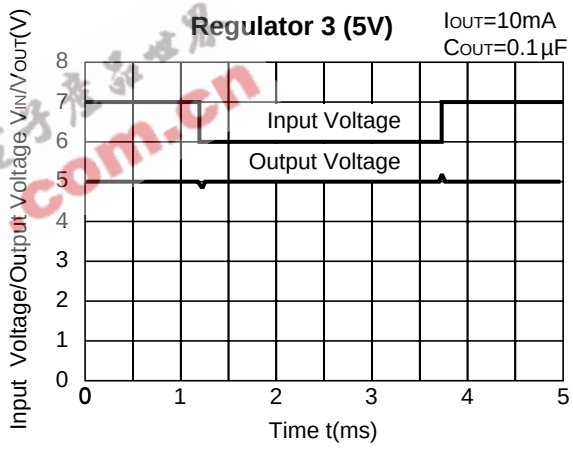


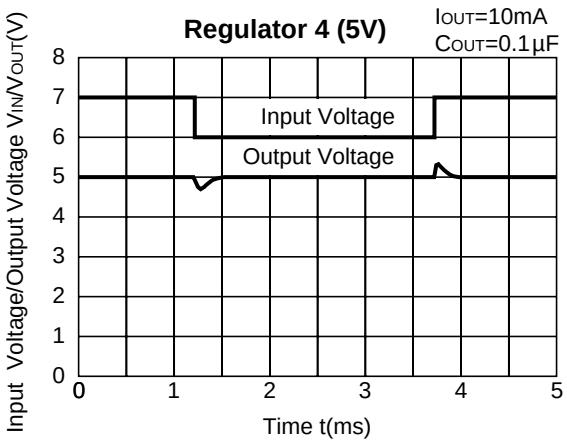




7) Line Transient Response 2

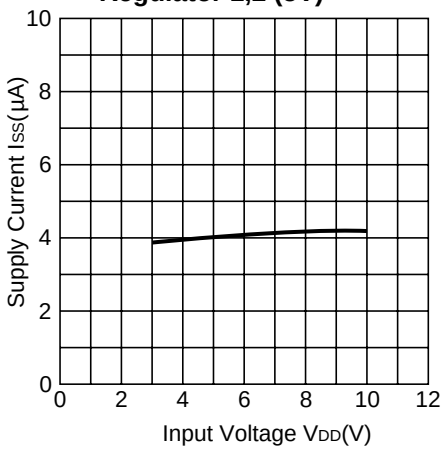




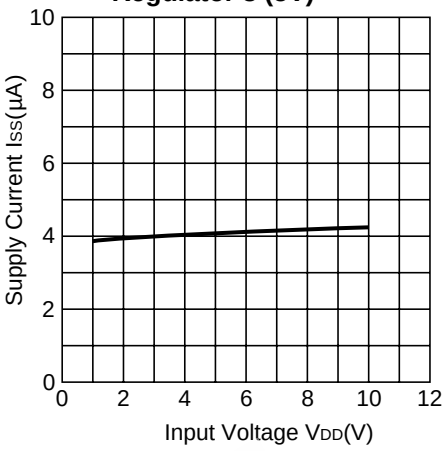


8) Supply Current vs. Input Voltage

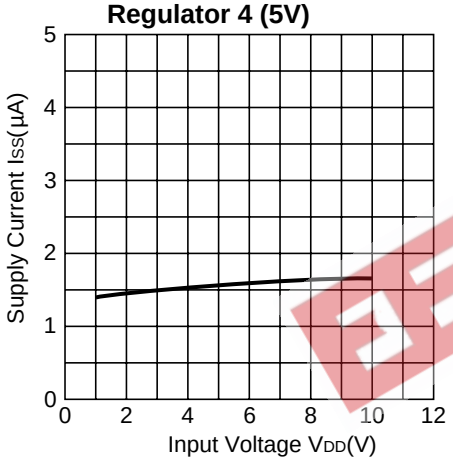
Regulator 1,2 (5V)



Regulator 3 (5V)

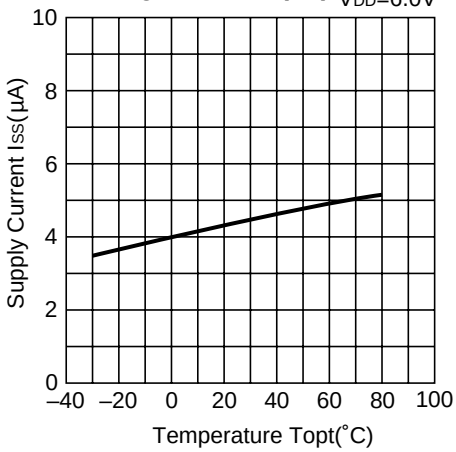


Regulator 4 (5V)

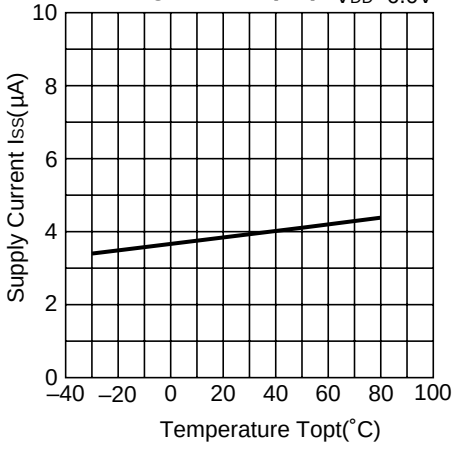


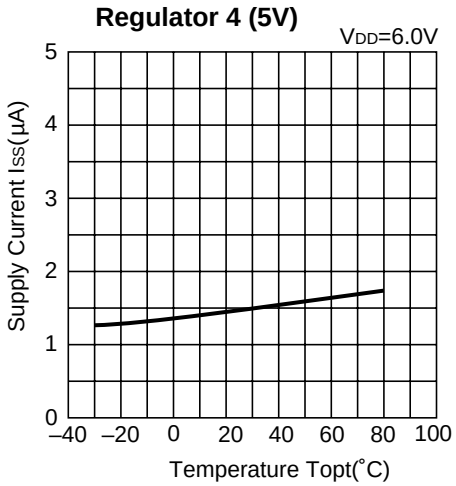
9) Supply Current vs. Temperature

Regulator 1,2 (5V) V_{DD}=6.0V

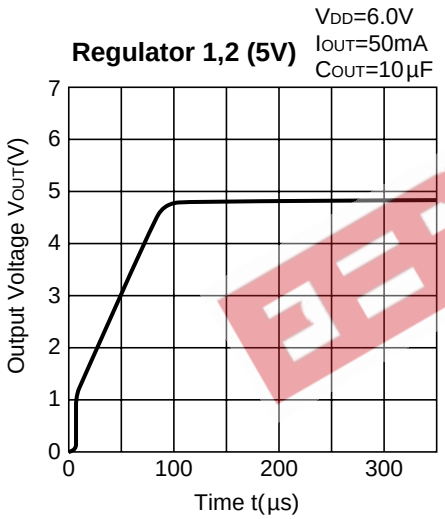


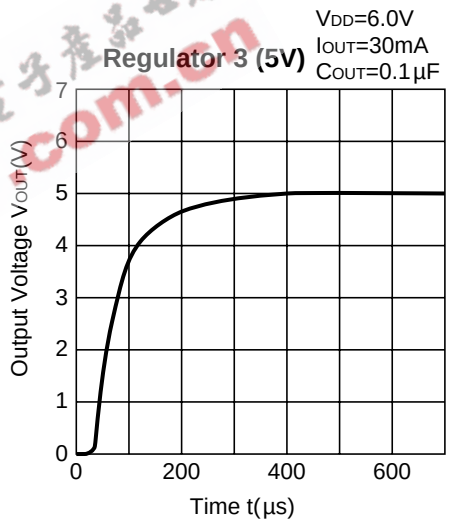
Regulator 3 (5V) V_{DD}=6.0V

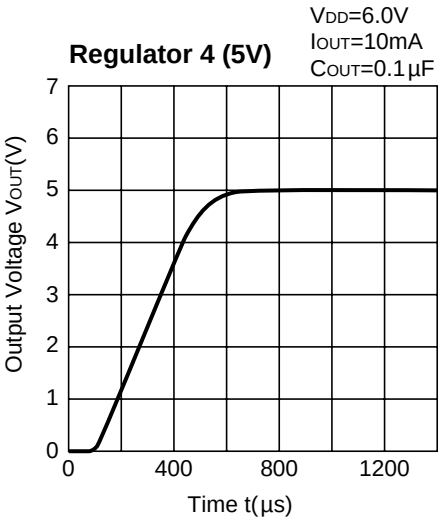




10) Output Voltage Transient Response for "CSW" Input Voltage Step



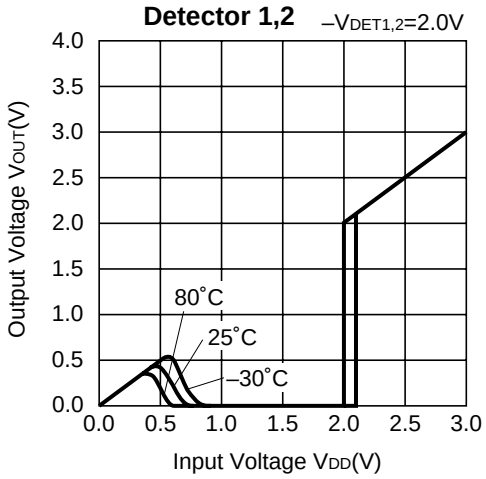




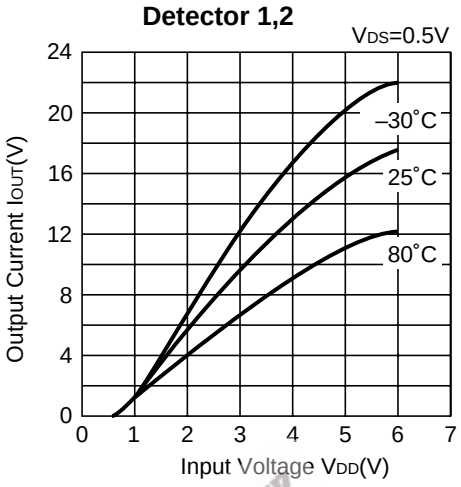
(Note) 0µs point is synchronous with being "H" state of Control Switch.

• **Detectors**

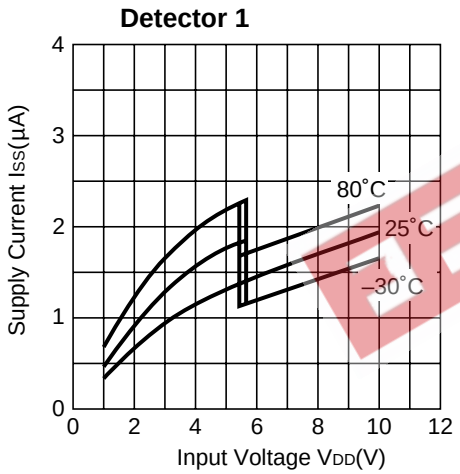
1) Output Voltage vs. Input Voltage

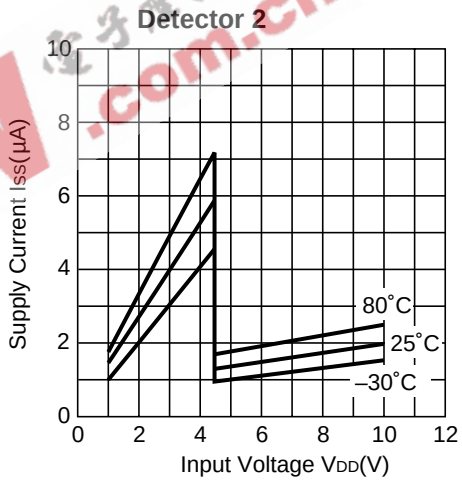


2) Output Current vs. Input Voltage

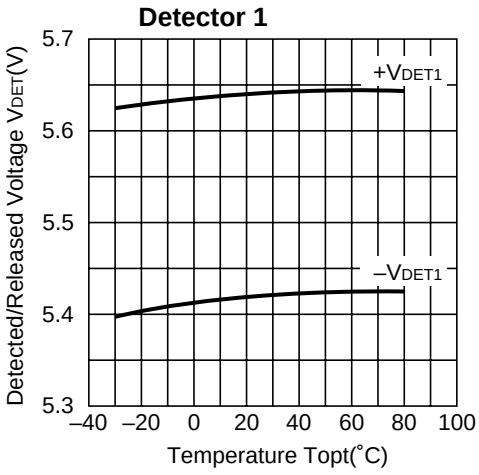


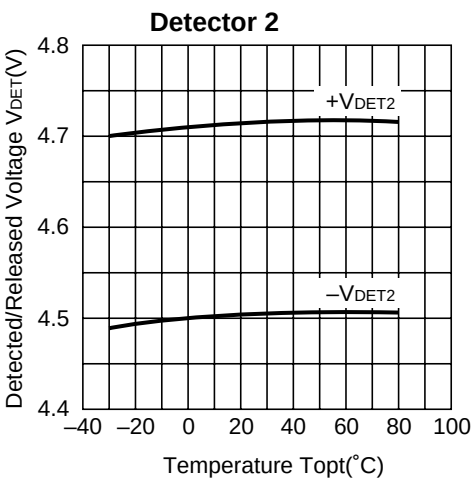
3) Supply Current vs. Input Voltage



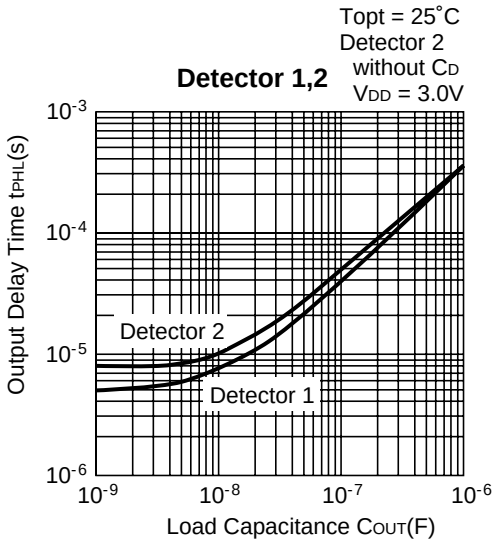


4) Detected/Released Voltage vs. Temperature

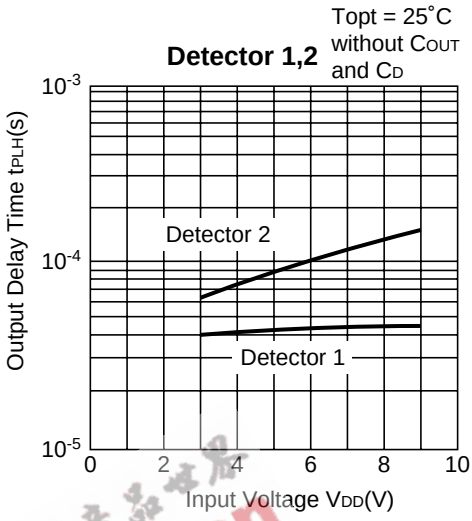




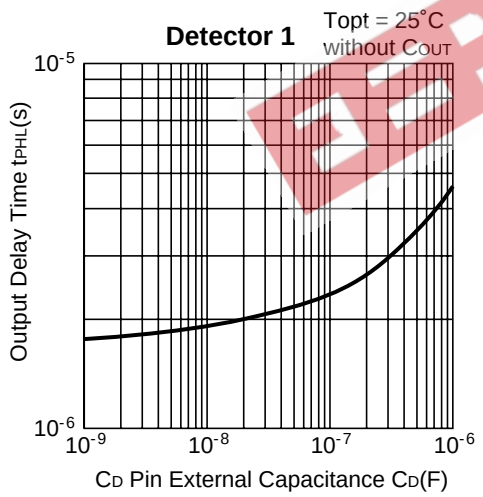
5) Output Delay Time (falling edge) vs. Load Capacitance



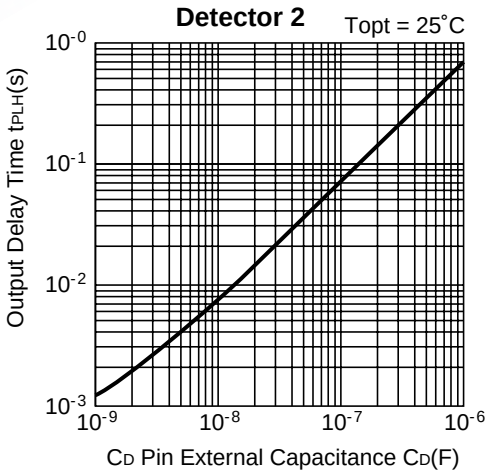
6) Output Delay Time (rising edge) vs. Input Voltage



7) Output Delay Time (falling edge) vs. CD Pin External Capacitance



8) Output Delay Time (rising edge) vs. CD Pin External Capacitance

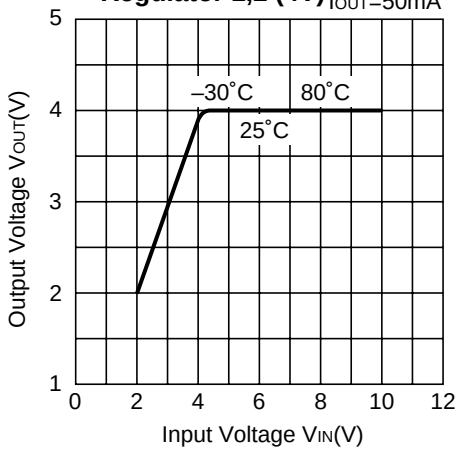


TYPICAL CHARACTERISTICS (RV5VE001B)

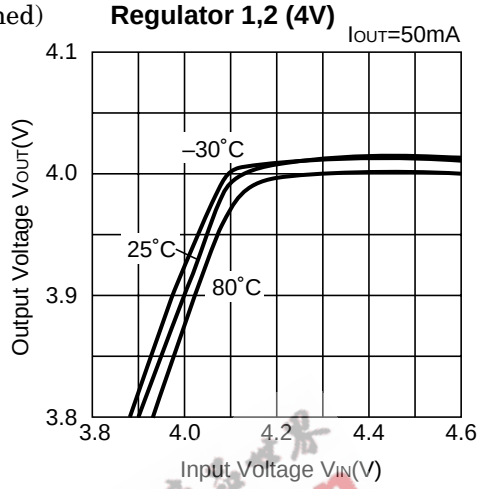
• **Regulators**

1) Output Voltage vs. Input Voltage

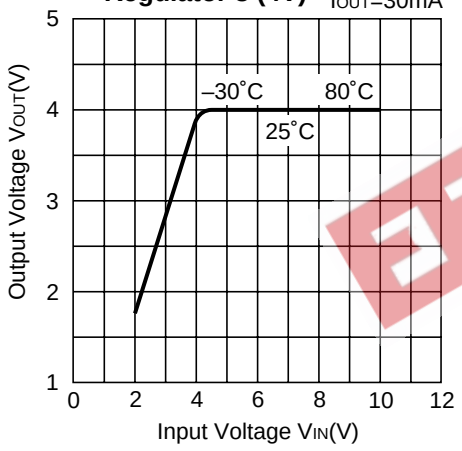
Regulator 1,2 (4V) I_{OUT}=50mA



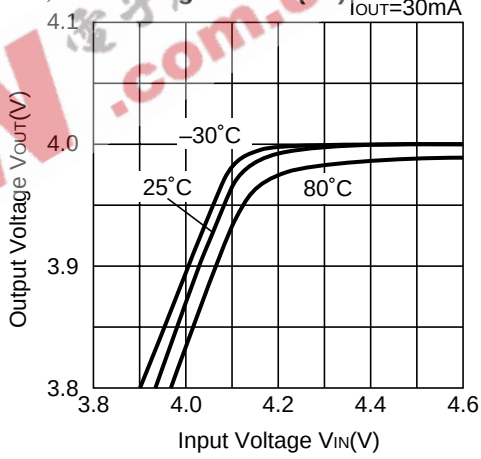
(zoomed) **Regulator 1,2 (4V)** I_{OUT}=50mA



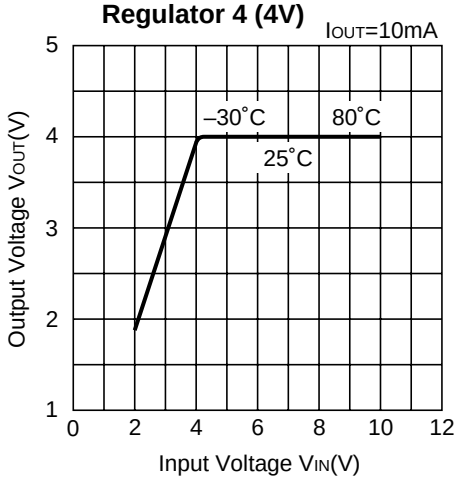
Regulator 3 (4V) I_{OUT}=30mA



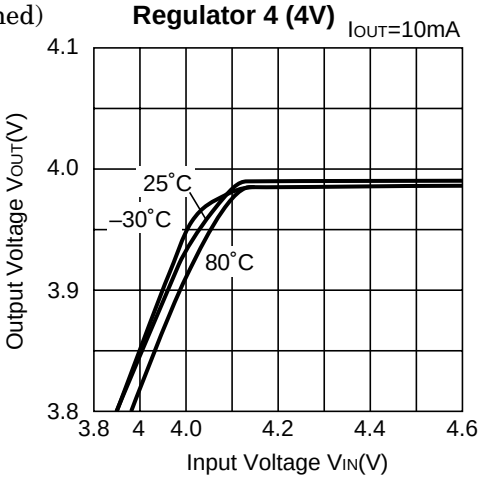
(zoomed) **Regulator 3 (4V)** I_{OUT}=30mA



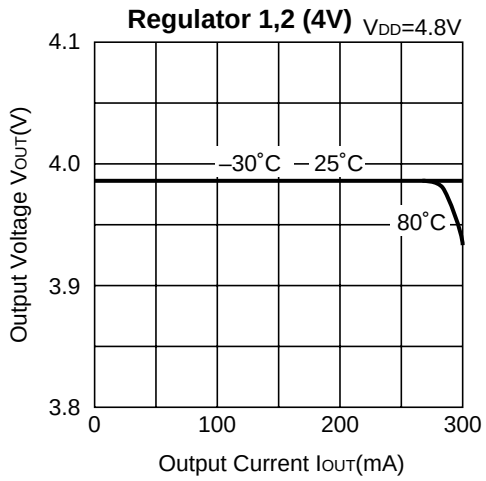
Regulator 4 (4V) I_{OUT}=10mA

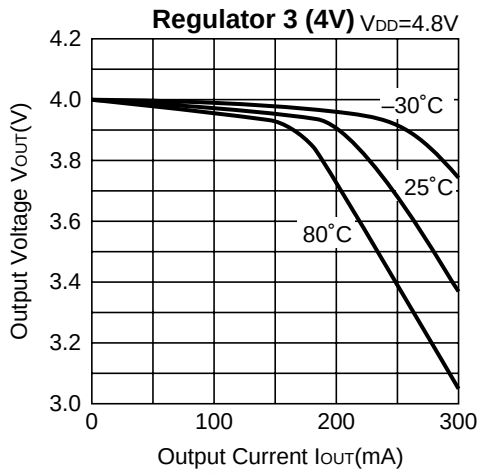


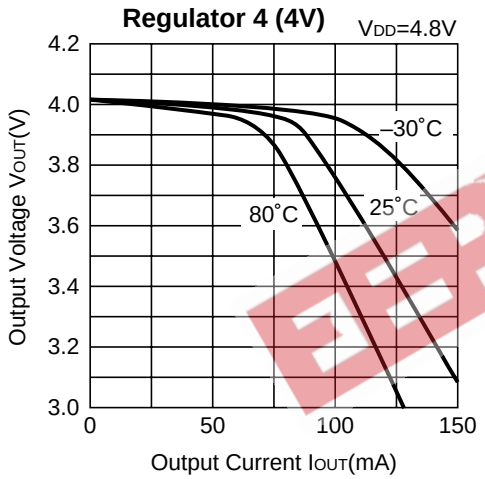
(zoomed) **Regulator 4 (4V)** I_{OUT}=10mA



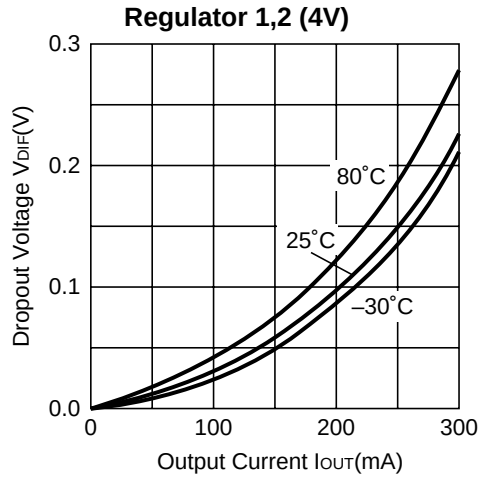
2) Output Voltage vs. Output Current

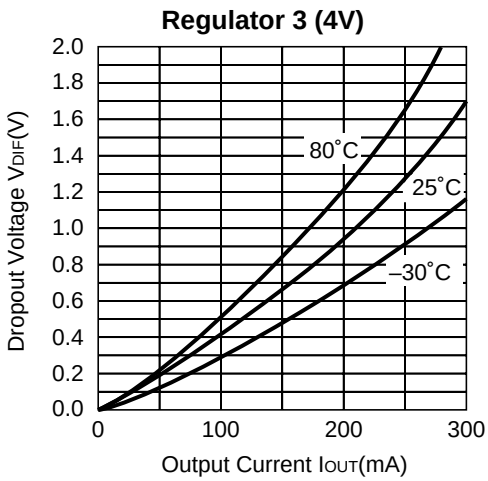


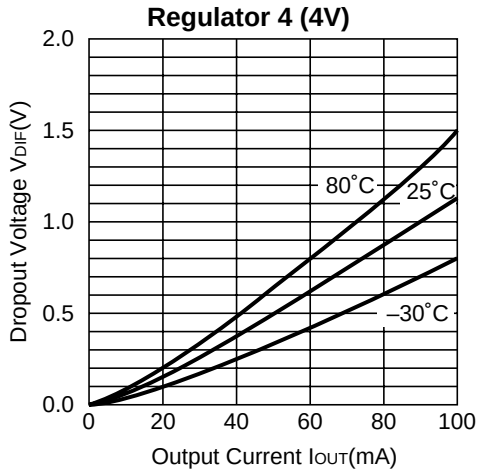




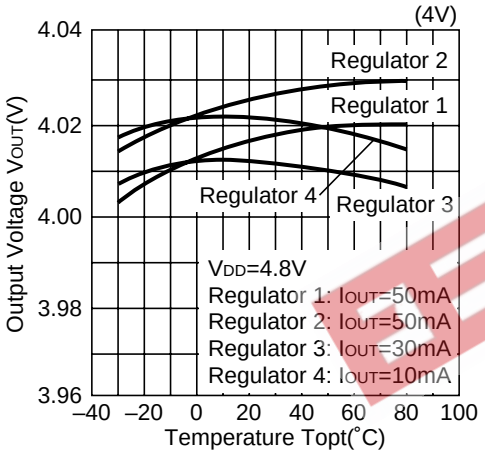
3) Dropout Voltage vs. Output Curret



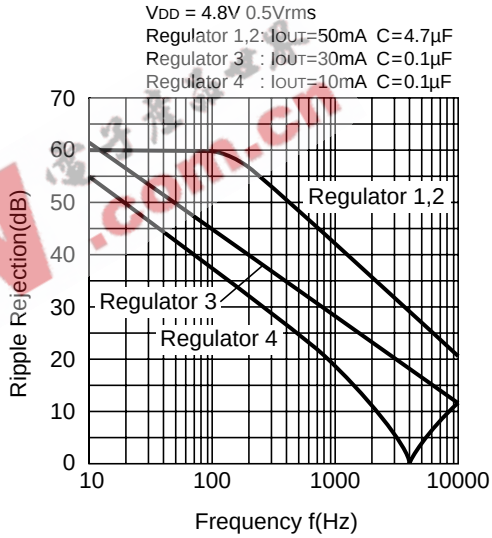




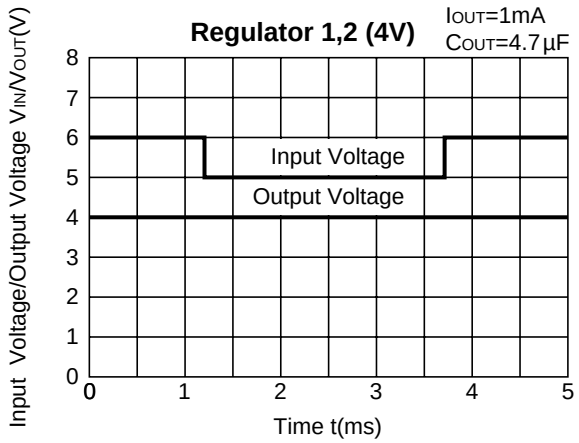
4) Output Voltage vs.Temperature

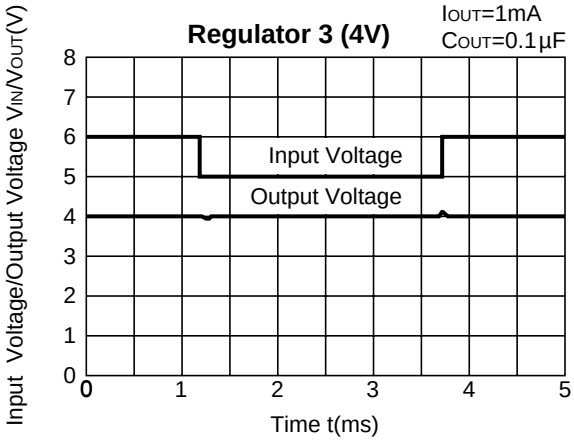


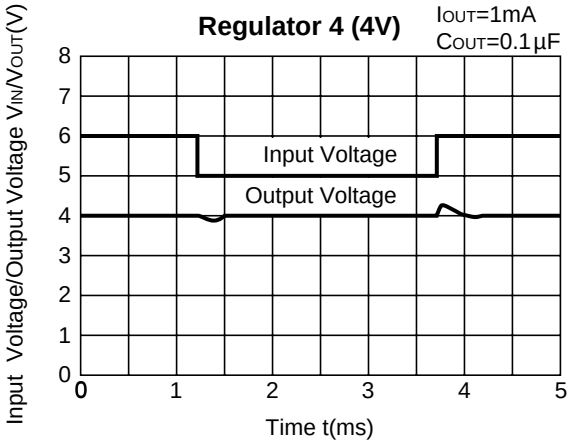
5) Ripple Rejection vs. Frequency



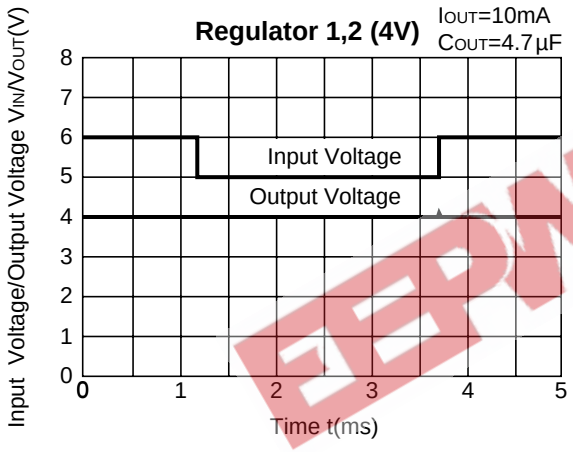
6) Line Transient Response 1

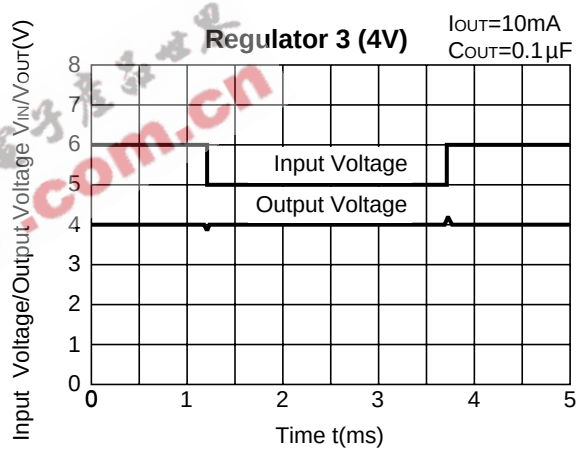


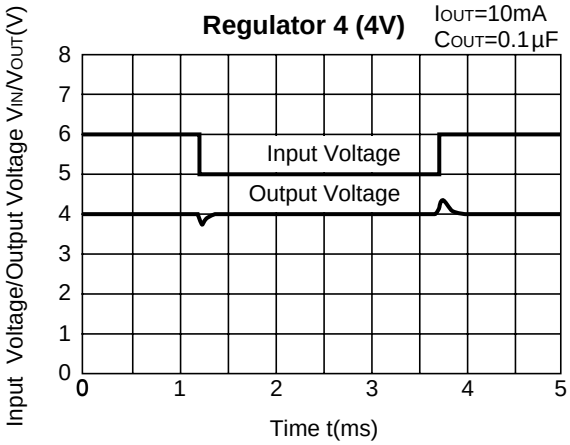




7) Line Transient Response 2

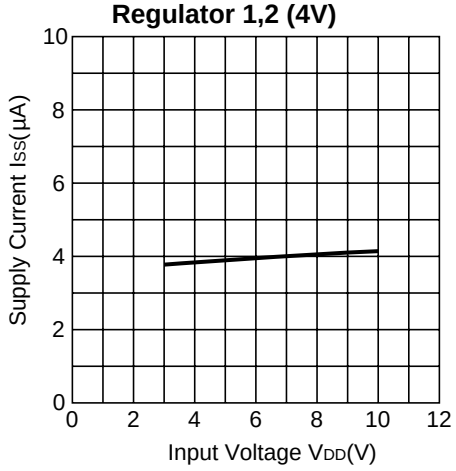




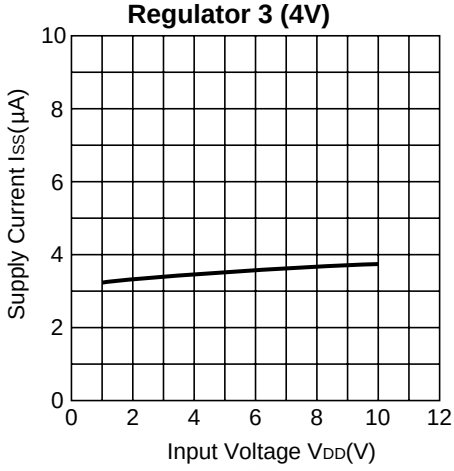


8) Supply Current vs. Input Voltage

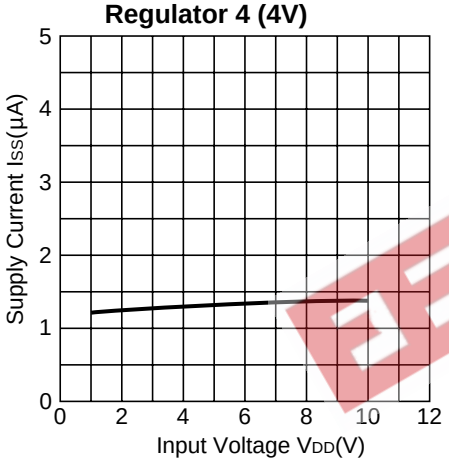
Regulator 1,2 (4V)



Regulator 3 (4V)

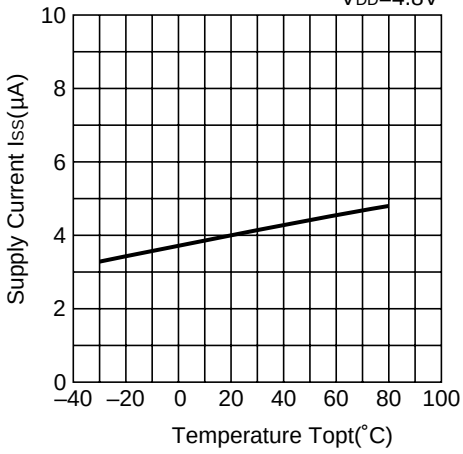


Regulator 4 (4V)

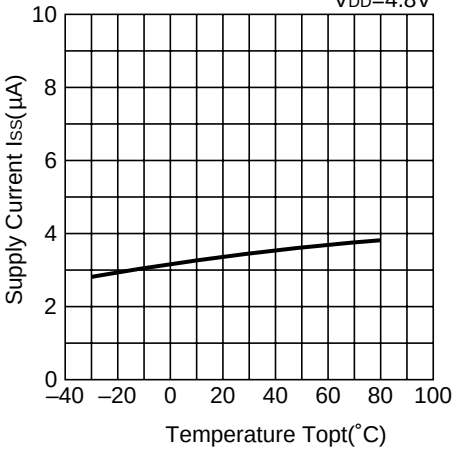


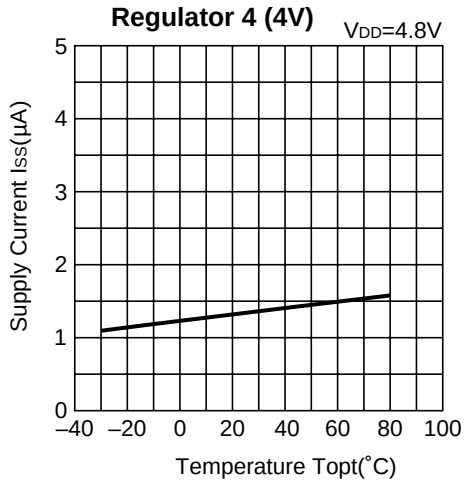
9) Supply Current vs. Temperature

Regulator 1,2 (4V) V_{DD}=4.8V

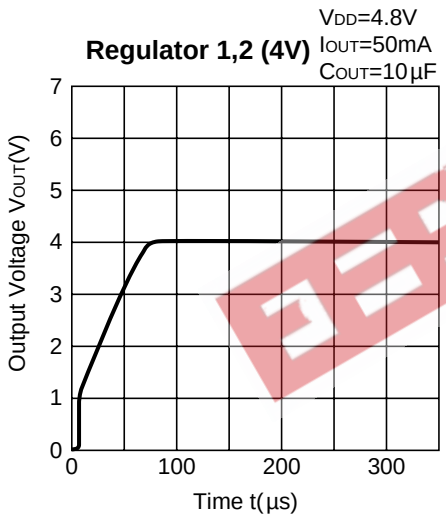


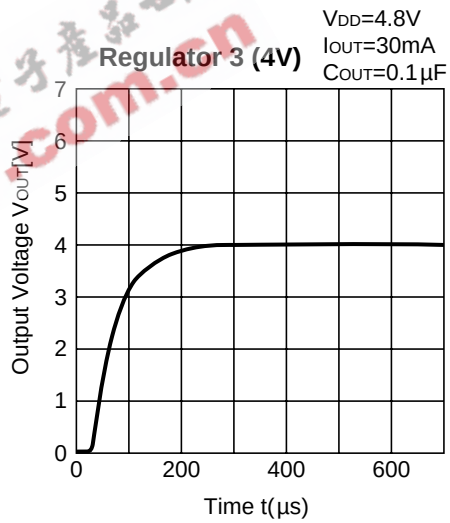
Regulator 3 (4V) V_{DD}=4.8V

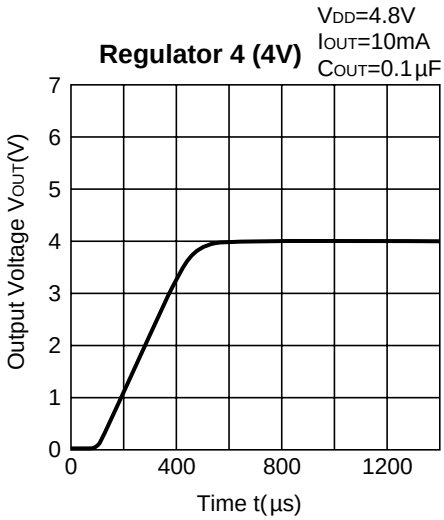




10) Output Voltage Transient Response for "CSW" Input Voltage Step



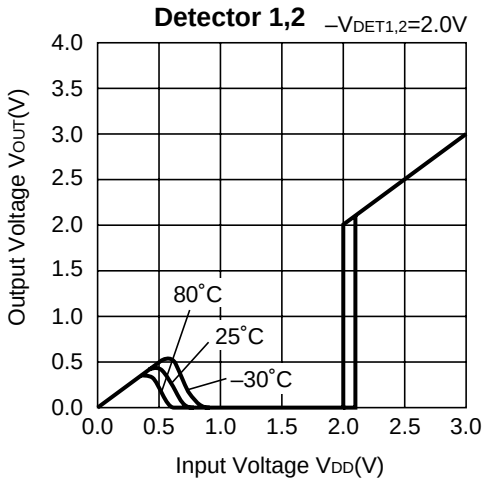




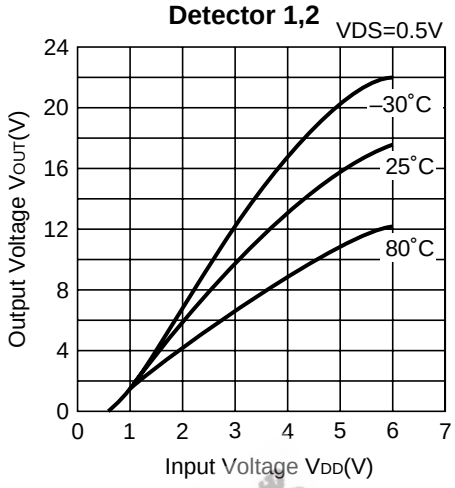
(Note) 0µs point is synchronous with being "H" state of Control Switch.

• **Detectors**

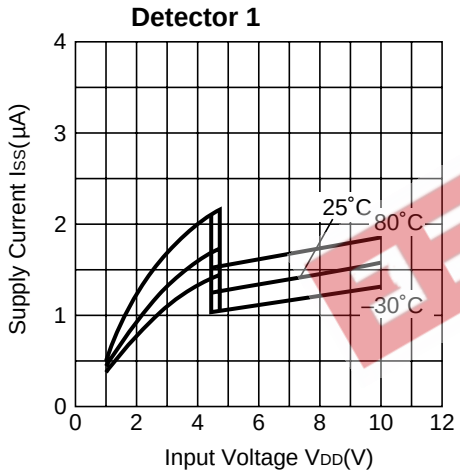
1) Output Voltage vs. Input Voltage

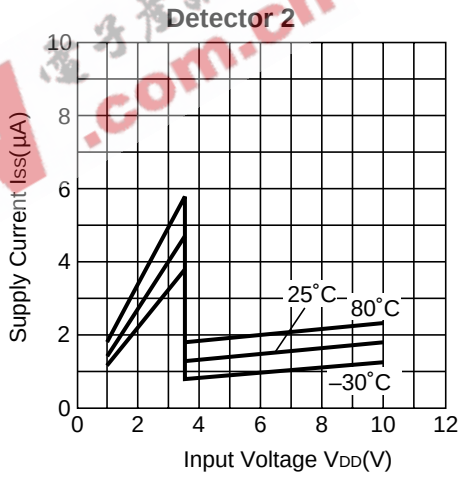


2) Output Current vs. Input Voltage

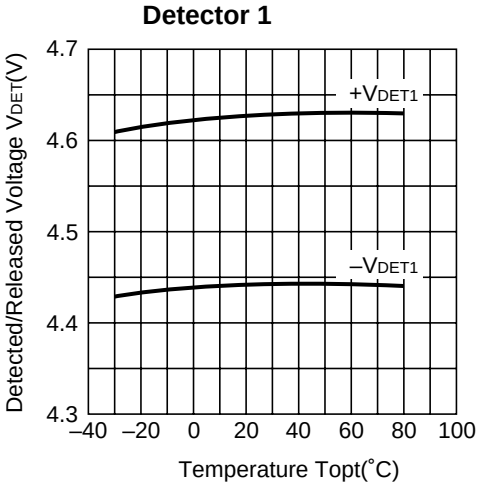


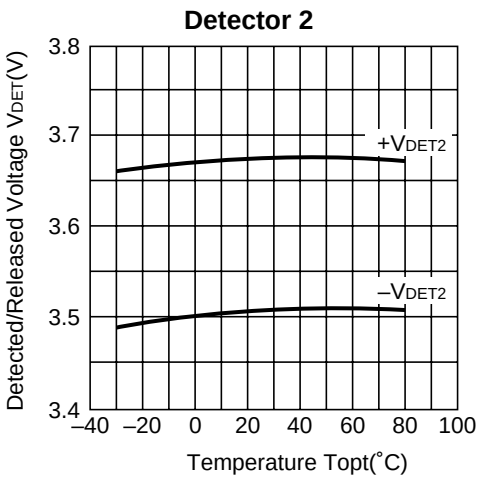
3) Supply Current vs. Input Voltage



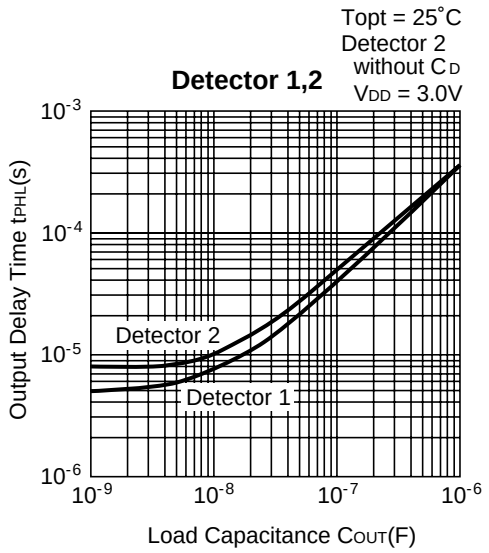


4) Detected/Released Voltage vs. Temperature

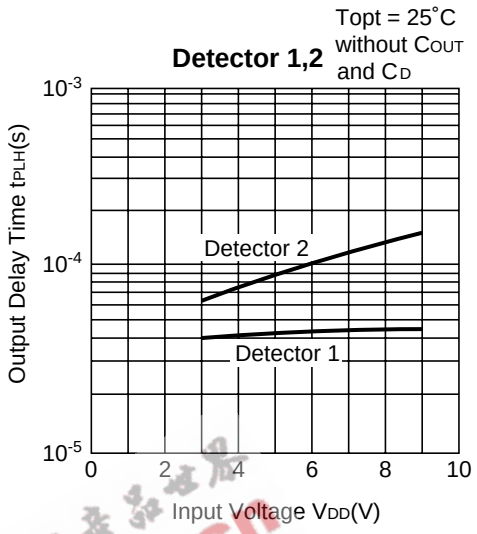




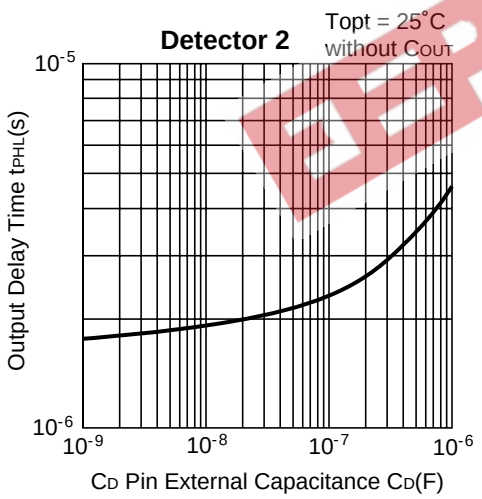
5) Output Delay Time (falling edge) vs. Load Capacitance



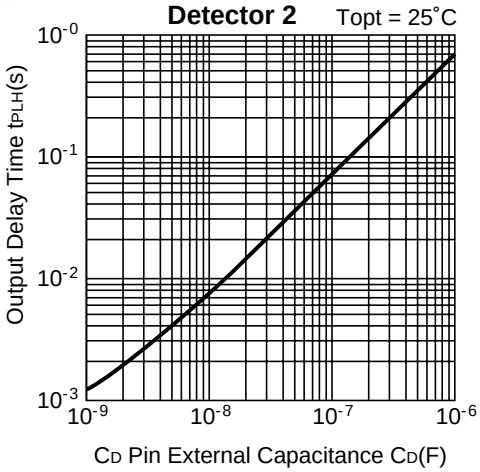
6) Output Delay Time (rising edge) vs. Input Voltage



7) Output Delay Time (falling edge) vs. CD Pin External Capacitance



8) Output Delay Time (rising edge) vs. CD Pin External Capacitance

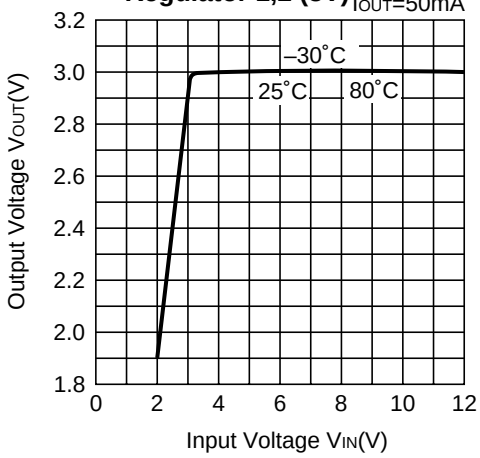


TYPICAL CHARACTERISTICS (RV5VE001C)

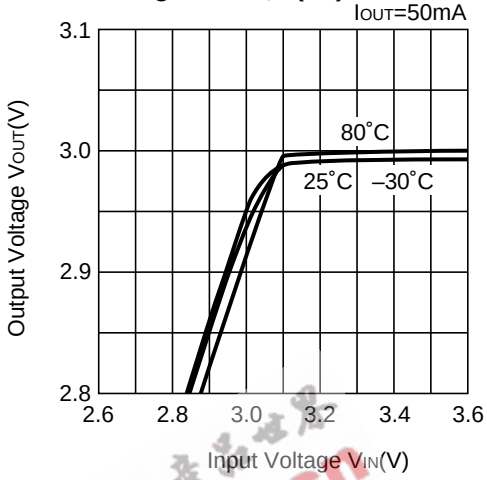
• **Regulator Section**

1) Output Voltage vs. Input Voltage

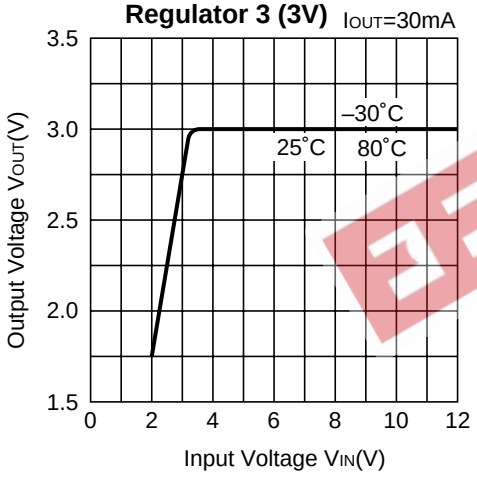
Regulator 1,2 (3V) I_{OUT}=50mA



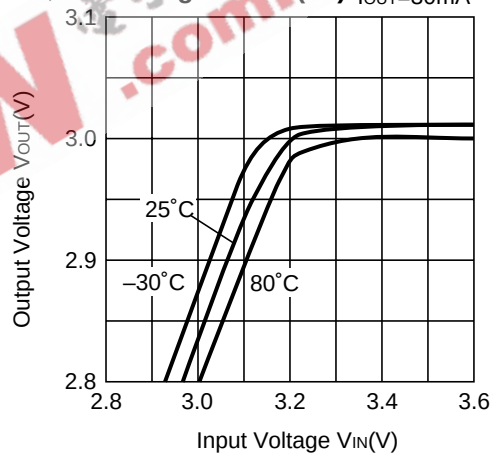
(zoomed) **Regulator 1,2 (3V)** I_{OUT}=50mA



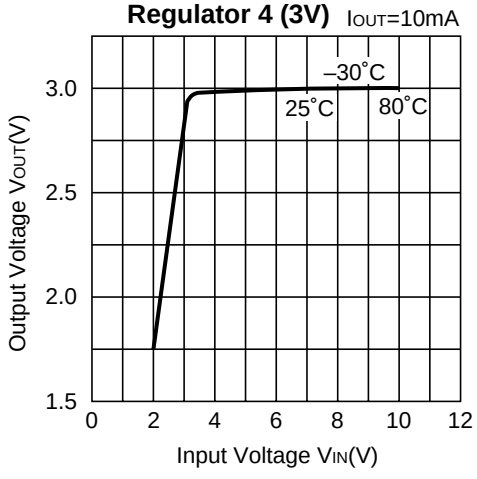
Regulator 3 (3V) I_{OUT}=30mA



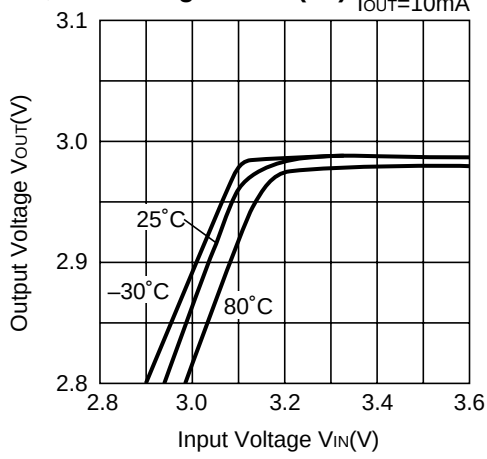
(zoomed) **Regulator 3 (3V)** I_{OUT}=30mA



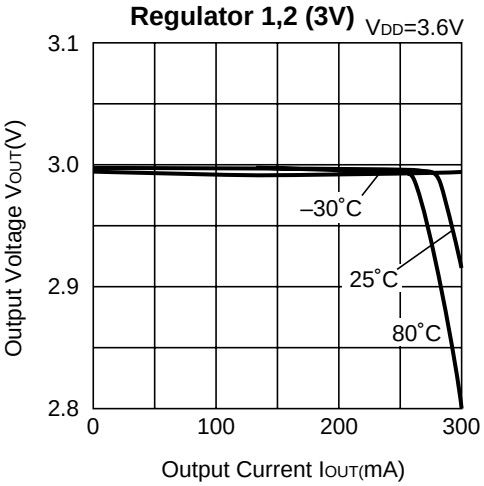
Regulator 4 (3V) I_{OUT}=10mA

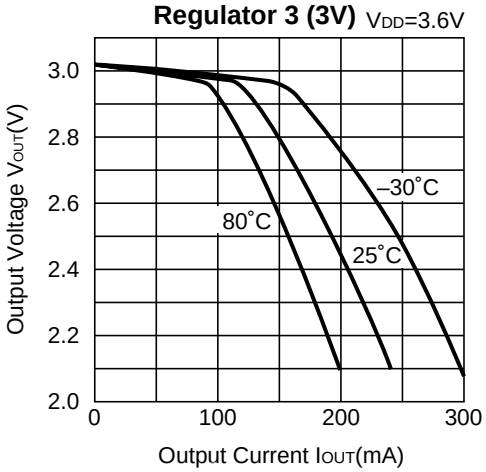


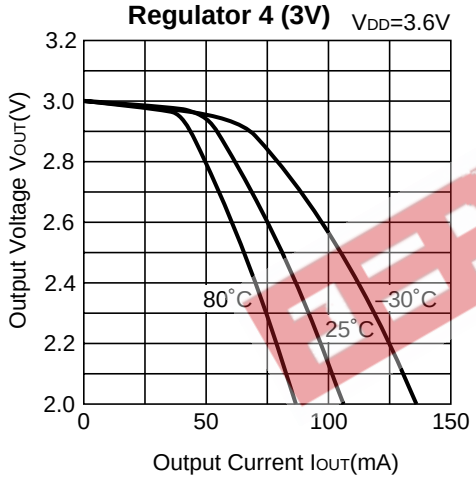
(zoomed) **Regulator 4 (3V)** I_{OUT}=10mA



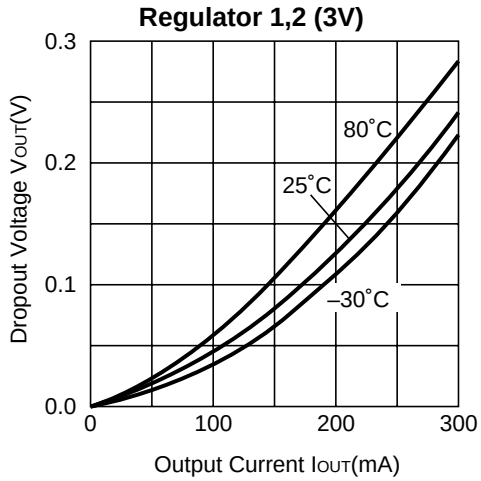
2) Output Voltage vs. Output Current

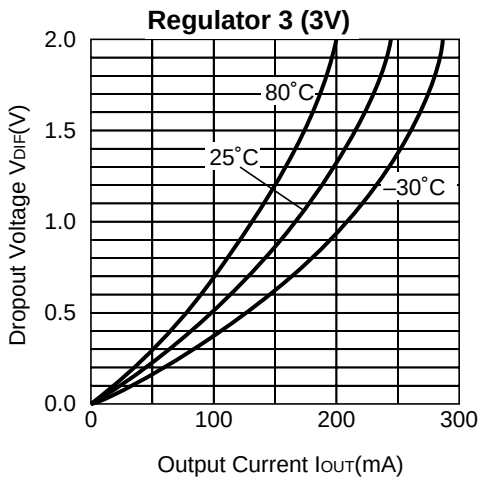


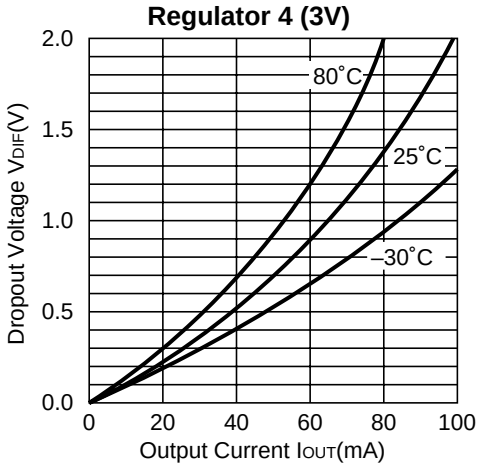




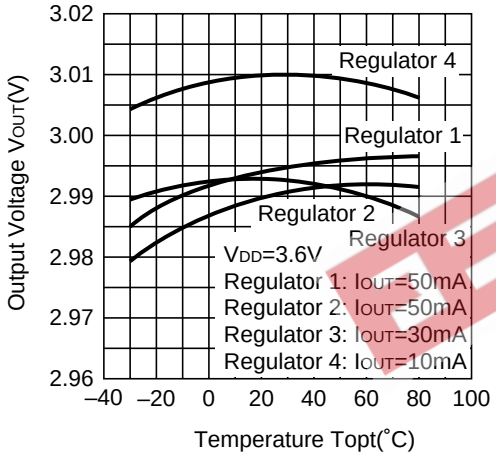
3) Dropout Voltage vs. Output Current



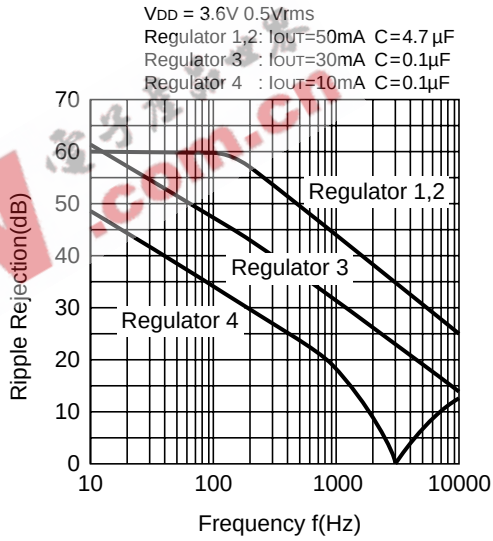




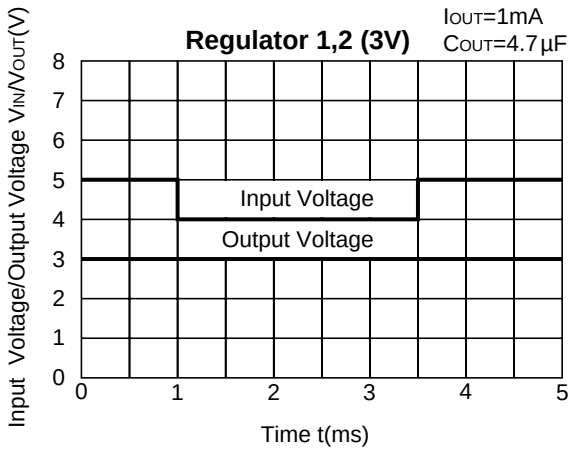
4) Output Voltage vs.Temperature

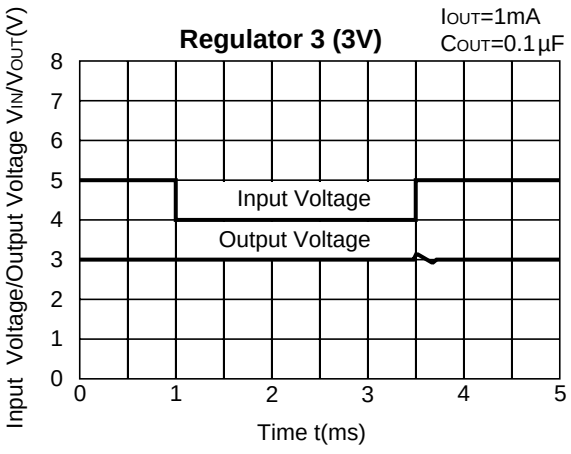


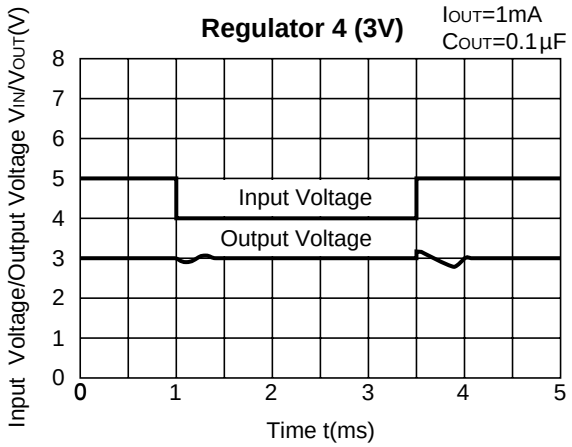
5) Ripple Rejection vs. Frequency



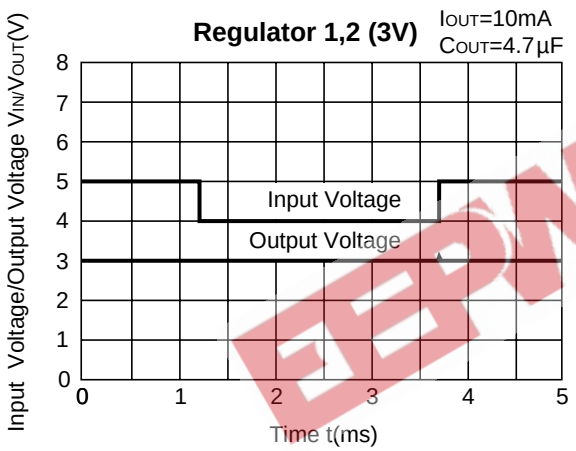
6) Line Transient Response 1

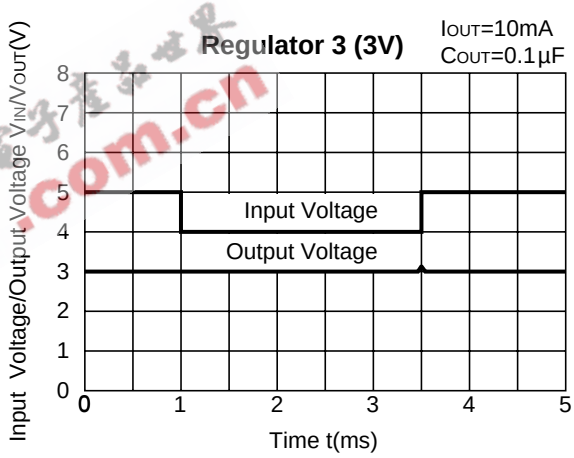


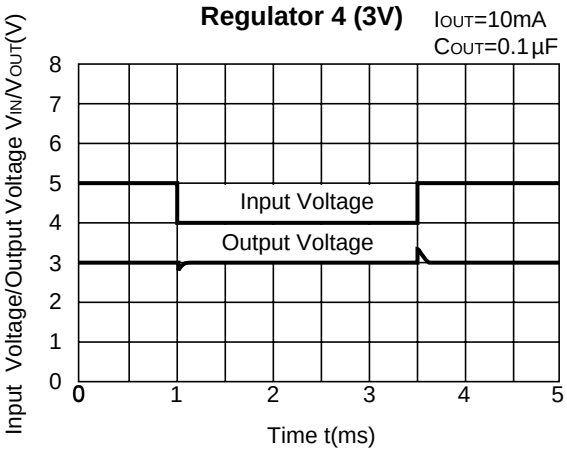




7) Line Transient Response 2

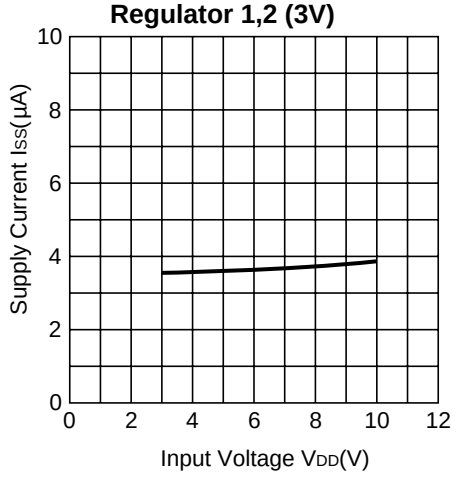




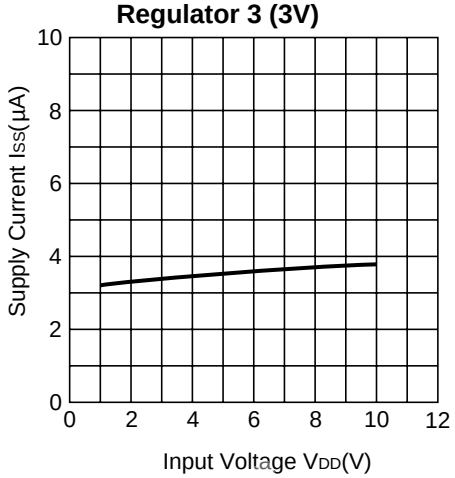


8) Supply Current vs. Input Voltage

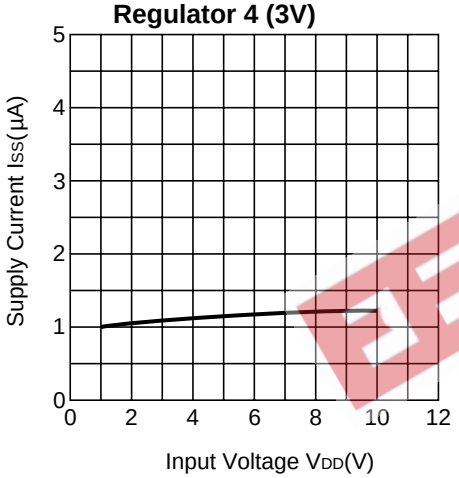
Regulator 1,2 (3V)



Regulator 3 (3V)

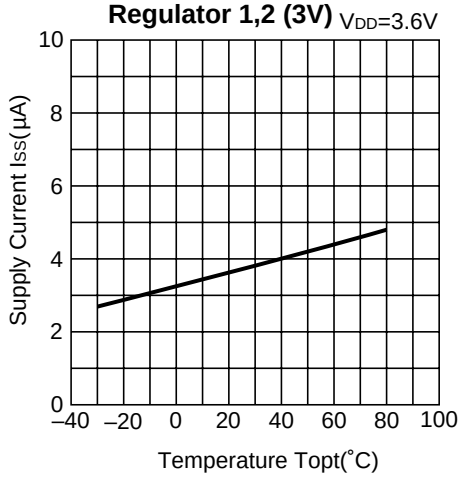


Regulator 4 (3V)

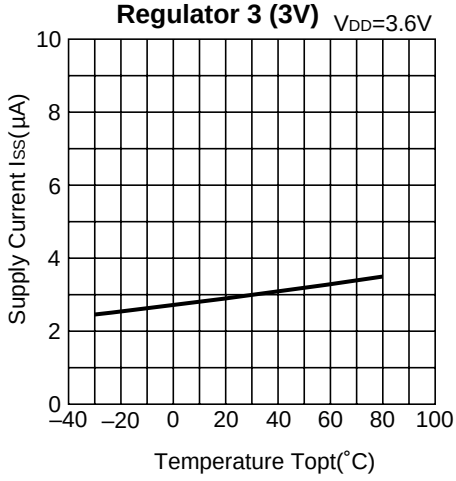


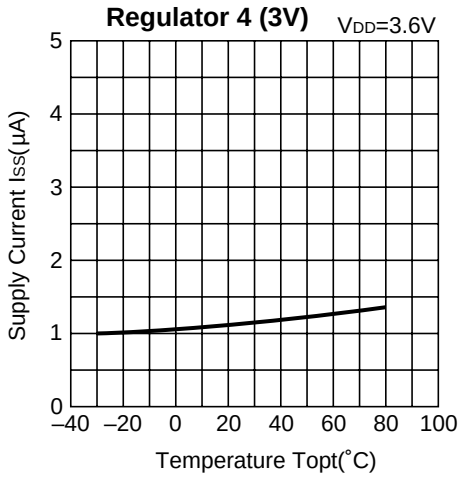
9) Supply Current vs. Temperature

Regulator 1,2 (3V) V_{DD}=3.6V

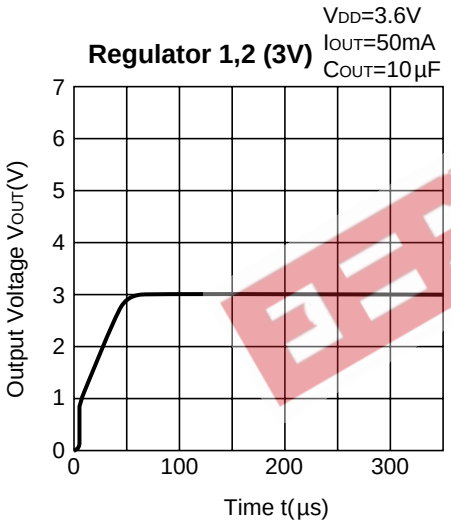


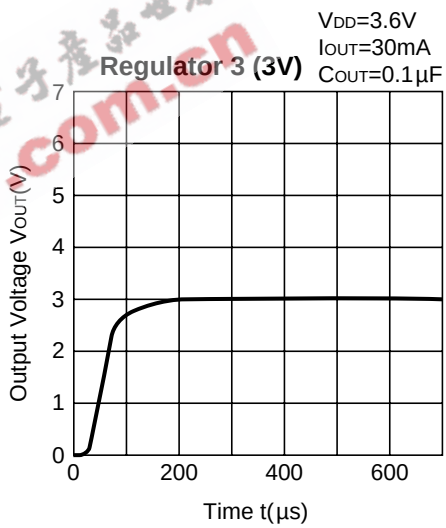
Regulator 3 (3V) V_{DD}=3.6V

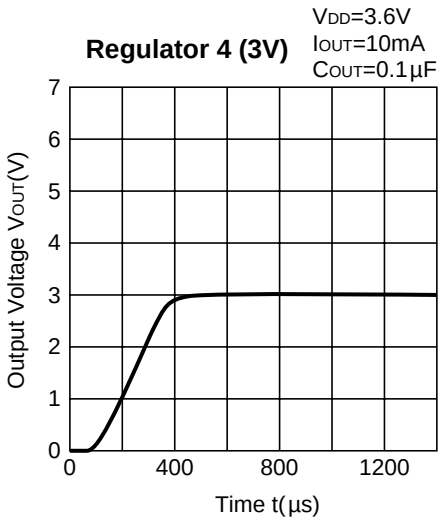




10) Output Voltage Transient Response for "CSW" Input Voltage Step



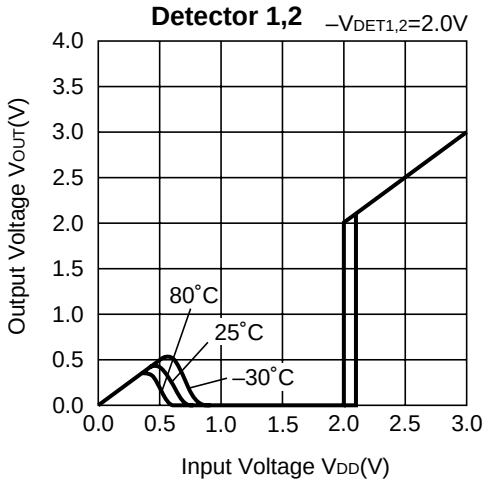




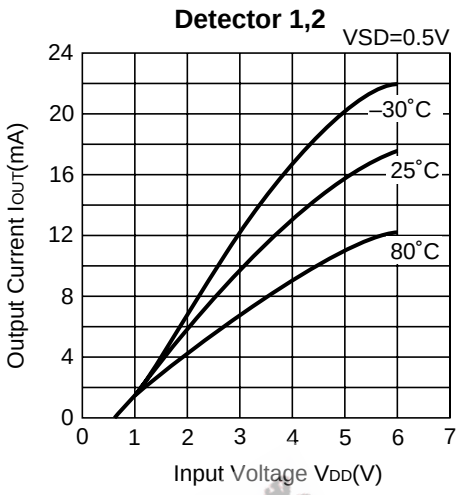
(Note) Control Switch becomes ON ("H") at 0µs.

• **Detectors**

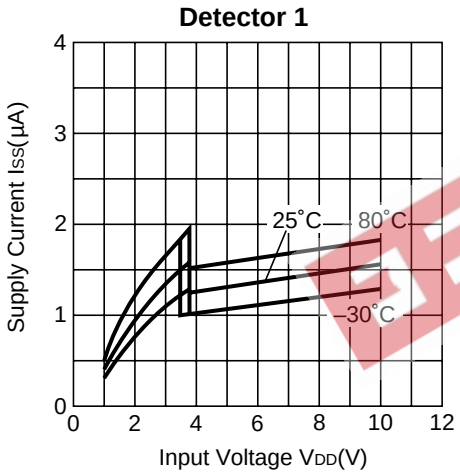
1) Output Voltage vs. Input Voltage

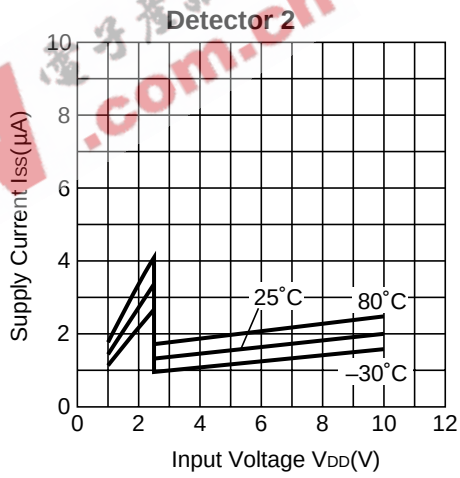


2) Output Current vs. Input Voltage

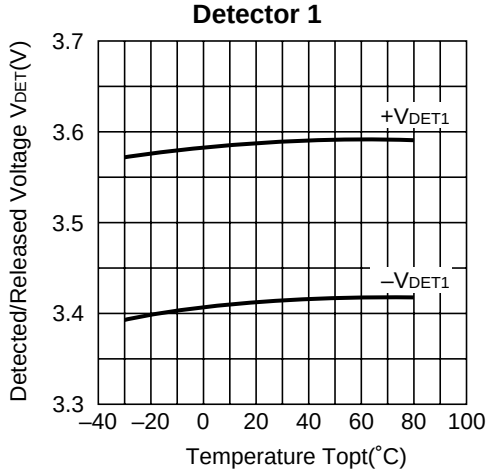


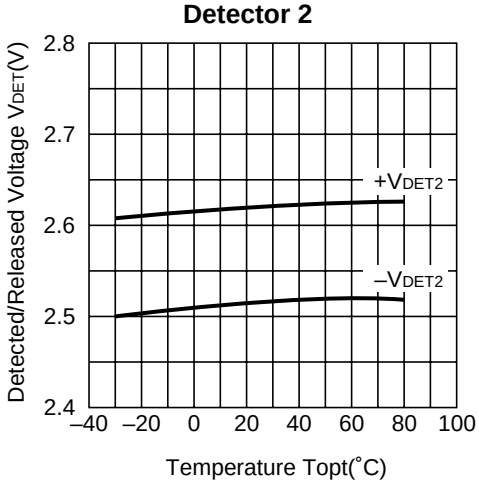
3) Supply Current vs. Input Voltage



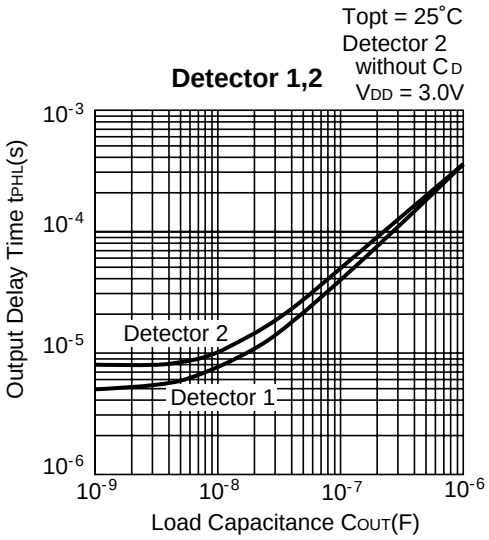


4) Detected/Released Voltage vs. Temperature

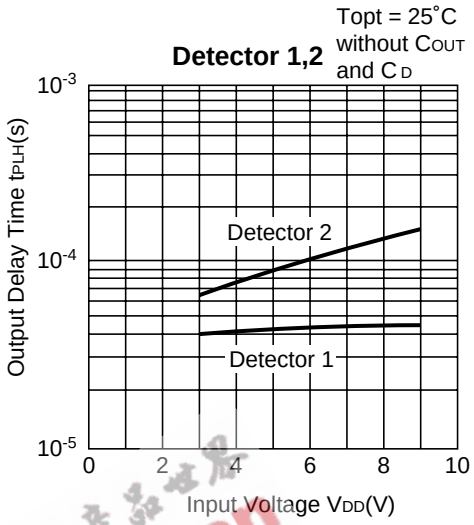




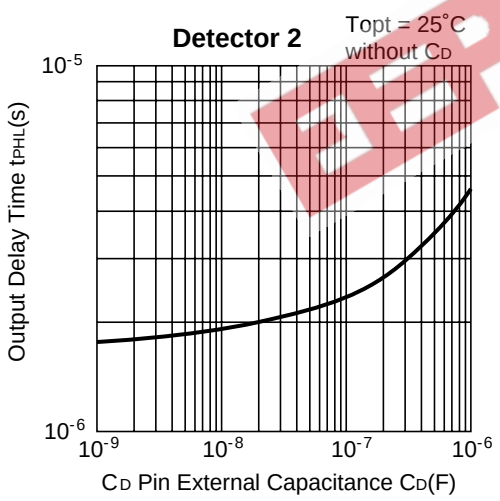
5) Output Delay Time (falling edge) vs. Load Capacitance



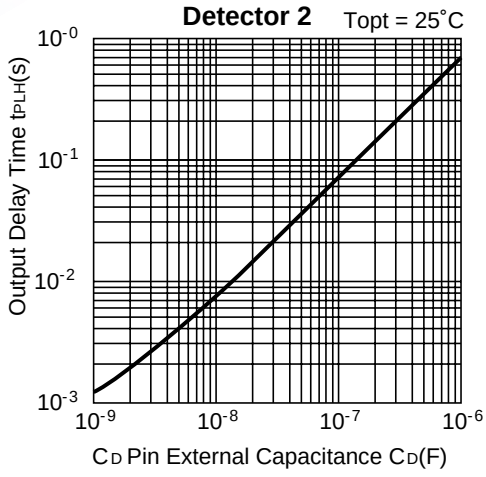
6) Output Delay Time (rising edge) vs. Input Voltage



7) Output Delay Time (falling edge) vs. CD Pin External Capacitance



8) Output Delay Time (rising edge) vs. CD Pin External Capacitance

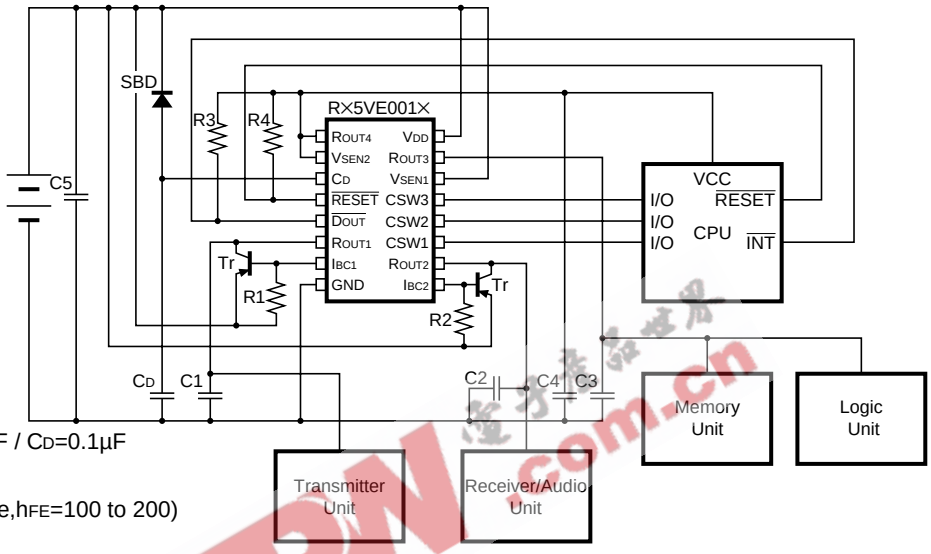


TYPICAL APPLICATION

• **RV5VE001×**

In this example of the circuit, the output of Regulator 4 is used as the power source for CPU. The voltage input to CSW 1, 2, 3 pins is subject to level shift within the IC so as to have the same level as that of the voltage of CPU. Therefore CSW 1, 2, 3 pins can be directly connected to CPU. Detector 1 monitors the voltage of the battery and Detector 2 monitors the voltage of the power source for CPU.

Application for Cellular Phones (RV5VE001×)



C1,2,5=10µF / C3,4=0.1µF / C_D=0.1µF
R1,2,3,4=100kΩ
Tr: 2SB799(NEC PNP type,h_{FE}=100 to 200)
SBD: MA717(Panasonic)

APPLICATION HINTS

When using these ICs, be sure to take care of the following points :

- Minimize the impedance of V_{DD} and GND wiring. In particular, with respect to the V_{DD} wiring, the output current of Regulators flows thereinto, so that when the wiring impedance is high, the operation of the IC tends to be unstable and is vulnerable to noise.
- Provide a capacitor with a capacitance of about 10µF between V_{DD} pin and GND pin with a minimum wiring length.
- Rush current flows into the capacitor connected to the output of Regulators at the start of the operation of the Regulators. In particular, Regulators 1, 2 are equipped with External PNP Transistor and accordingly have excellent drive performance. Therefore, when Regulators 1, 2 start to operate, for example, under the conditions that h_{FE} of External PNP Transistor is 100 and the base current of the limiter is 5mA, a rush current of 500mA flows into the regulators. When the wiring impedance is high, the Power Source Voltage applied to IC tends to be varied by the rush current, so that the operation of IC may be adversely affected by the variation of the Power Source Voltage.
- In these ICs phase compensation is made for securing stable operation even when the load current is varied. Select the capacitors C1 to C4 conecting the Pin V_{OUT1} to V_{OUT4} with good frequency characteristics and small ESR.
- Be sure to connect a resistor with a resistance of about 100kΩ between the base and the emitter for preventing the oscillation.
- Set external parts as close as possible to the IC and minimize the connection between the parts and the IC.
- When using a capacitor connected to C_D pin, use a Schottky Barrier Diode (SBD) to discharge C_D capacitor at the time of abrupt fluctuation of power source voltage.

APPLICATION FOR CELLULAR PHONES (RV5VE0×××:Optional Mask Version)

This Optional Mask Version's application operates as follows.

Regulator 1, 2 : Regulator 1 and 2 can be enabled and disabled through Toggle Input and CPU signal CSW1.

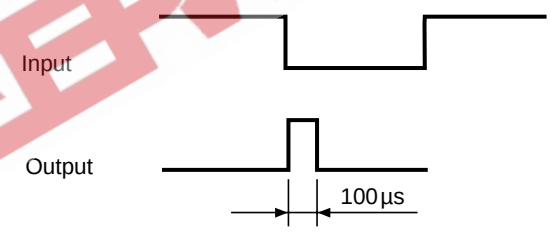
Regulator 3 : Regulator 3 can be enabled and disabled through Toggle Input and CPU signal CSW2.

Regulator 4 : Regulator 4 is always enabled by dry cells (when the V_{DD} voltage is maintained higher than minimum operating voltage). The output of Regulator 4 is not only the power source for CPU but also the level shift voltage of CSW 1, 2 pins. Therefor CSW1, 2 pins can be directly connected to CPU.

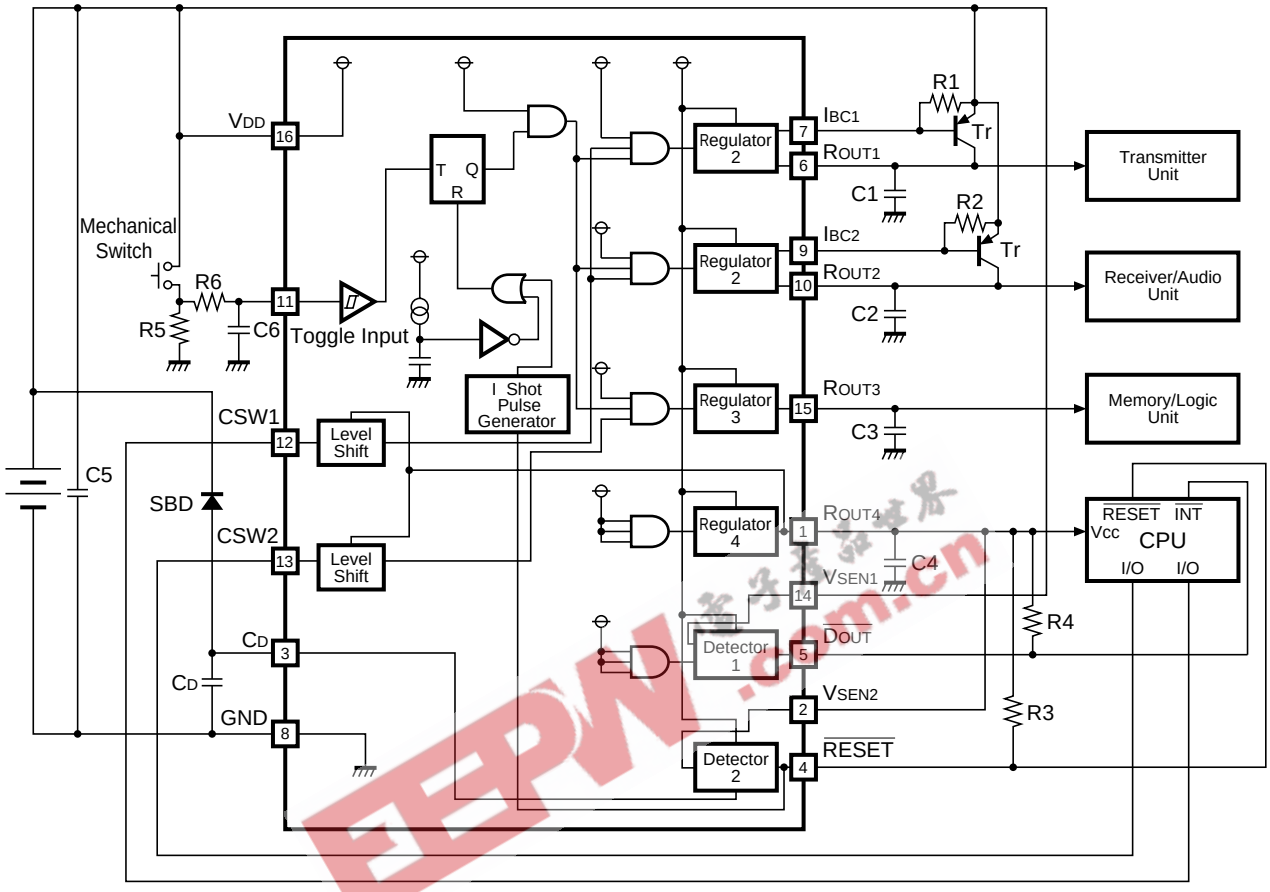
Detector 1, 2 : Detector 1 and 2 monitor the V_{DD} level and the output of Regulator 4 respectively. Furthermore Detector 2 can generate the output-delay time (time delay to output rising edge) by connecting a capacitor to C_D pin.

TFF : TFF can be reset by the output of power-on-reset and Detector 2 (through one shot pulse generator), while TFF is in the reset state Regulator 1, Regulator 2 and Regulator 3 are disabled.

one shot pulse generator operation



Application for Cellular Phones (RV5VE0×××)



C1,2,5=10µF/C3,4=0.1µF/C6=1µF/C_D=0.1µF
R1,2,3,4=100kΩ/R5=10kΩ/R6=47Ω
Tr: 2SB799(NEC PNP type,h_{FE}=100 to 200)
SBD: MA717(Panasonic)