Dot Matrix 48x4 LCD Controller / Driver

■ Features

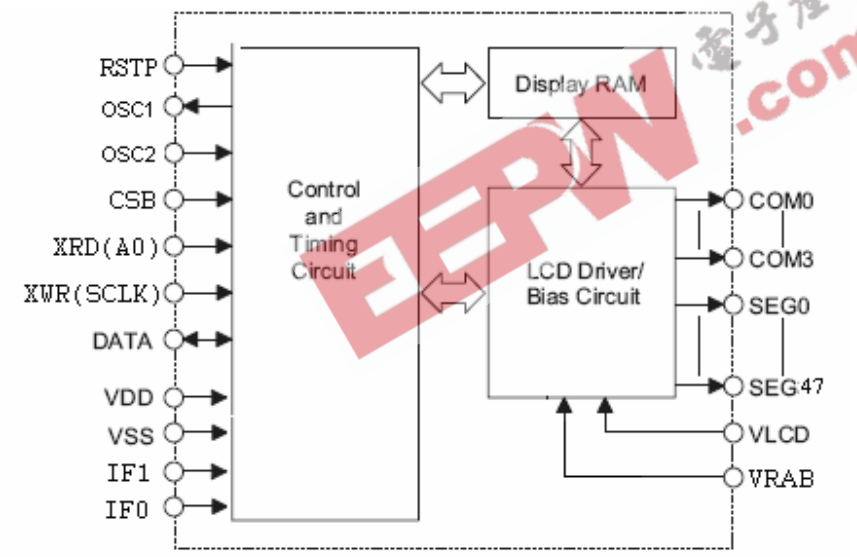
- Operating voltage: 2.4V~5.2V
- External resistor CR oscillator
- External 256k Hz frequency source input
- Selection of 1/2 or 1/3 bias, and selection of 1/2or 1/3 or 1/4 duty LCD applications
- Power down command reduces power consumption
- 48 x 4 LCD driver
- Built-in 48 x 4 bit display RAM
- IIC serial interface
- 3-line/4-line (type A & type B) serial interface (SPI)
- Internal LCD driving frequency source
- Software configuration feature
- Data mode and command mode instructions
- R/W address auto increment
- VRAB pin for adjusting VLCD operating voltage

■ General Description

The RW1026 is a 192 patterns (48x4), memory mapping, and multi-function LCD driver. The S/W configuration feature of the RW1026 makes it suitable for multiple LCD applications including LCD modules and display subsystems.

Only two or three or four lines are required for the serial interface between the host controller and the RW1026. The RW1026 contains a power down command to reduce power consumption.

■ Block Diagram



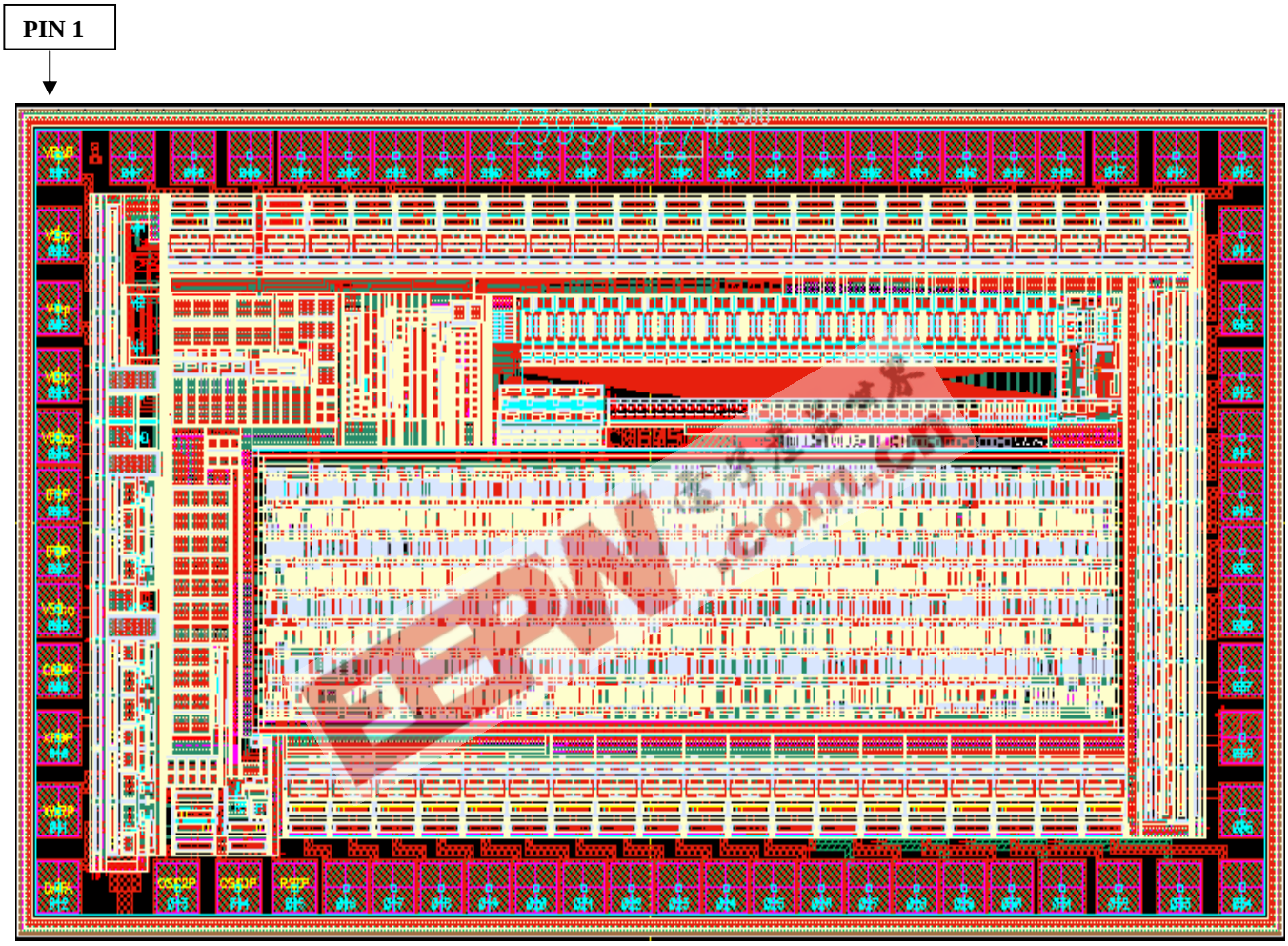
Note : CSB: Chip selection
XWR,XRD,DATA: Serial Interface
COM0~COM3, SEG0~SEG47: LCD outputs
IF1 ,IF0 : interface select pin

■ Pad Assignment

Chip size: 2463 x 1344 um
Pad Size: 89.5 x 88.5 um
Pad Pitch: 92.5~231.4 um
Chip thickness: 482.6 um

- **The IC substrate should be connected to VSS in the PCB layout artwork.**

■ CHIP LAYOUT



■ Pad Description

Pad	I/O	Function
CSB	I	Chip selection input for 3-SPI, 4-SPIwith pull-high resistor. When CSB is login high, the data and command read from or written to the RW1026 are disabled. The serial interface circuit is also reset. But if CSB is at logic low level and is input to the CSB pad, the data and command transmission between the host controller and the RW1026 are all enabled.
XRD(A0)	I	READ clock input for 4-SPI (type B) with pull-high resistor. Data in the RAM of RW1026 are clocked out on the falling edge of the XRD signal. The clocked out data will appear on the DATA line. The host controller can use the next rising edge to latch the clocked out data. A0 pin for 4-line(type A)serial interface. A0=1: DATA A0=0: Command
XWR(SCLK)	I	WRITE clock input for 4-SPI (type B) with pull-high resistor. Data on the DATA line are latched into the RW1026 on the rising edge of the XWR signal. Serial clock input (SCLK) pin for 3-line, 4-line (type A), and IIC interface.
DATA	I/O	Serial data input/output with pull-high resistor.
VSS	-	Negative power supply. Ground
OSC1	I	The OSC1 and OSC2 pads are connected to a external resistor if an RC oscillator is selected. If the system clock comes from an external clock source, the external clock source should be connected to the OSC1 pad.
OSC2	O	
VLCD	I	LCD power input.
VDD	-	Positive power supply.
COM0-COM3	O	LCD common output.
SEG0-SEG47	O	LCD segment output.
RSTP	I	Reset pin with pull-up resistor, Initialized by setting RSTP to "L". Reset operation is performing at RSTP signal level.
VRAB	I	LCD voltage adjusting pin. Applies voltage between V0 and VSS using a split resistor.
IF1,IF0	I	Interface selection pins with pull-up resistor IF1,IF0 (0 , 0) : IIC Interface (0 , 1) : 3-line Interface (1 , 0) : 4-line Interface (Type A) (1 , 1) : 4-line Interface (Type B)