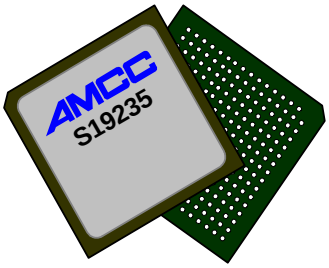

Description

The S19235 SONET/SDH/FEC and 10 Gigabit Ethernet (GbE) transceiver is one of the latest additions to AMCC's SuperPHY™ product family. The S19235 device provides fully integrated serialization/de-serialization capabilities for low power Intermediate and long Reach OC-192 applications. The device performs all necessary parallel-to-serial and serial-to-parallel functions in conformance with SONET/SDH and 10GbE transmission standards. The standard operating range is from 9.953 Gbps to 11.1 Gbps. Figure 1, *System Block Diagram*, shows a typical network application.

Overview

The S19235 can be used to implement the front end of SONET/SDH/FEC/10GbE equipment which consists primarily of the serial transmit interface and the serial receive interface. The system timing circuitry consists of a high-speed phase detector, clock dividers, and clock distribution. The device utilizes on-chip clock synthesis PLL components that allow the use of a slower external clock reference, 155.52 MHz or 622.08 MHz (or equivalent FEC/10GbE rate), in support of existing system clocking schemes. The low-jitter, 16-bit, Low Voltage Differential Signaling (LVDS) interfaces guarantee compliance with the bit-error rate requirements of the Telecordia and ITU-T standards.

AMCC Suggested Interface Devices

VERRAZANO (S2509)	Quad STS-48 SONET/SDH/ Digital Wrapper Backplane SERDES
GANGES (S19202)	STS-192 POS/ATM SONET/ SDH Mapper
GANGES II (S19202)	STS-192 POS/ATM SONET/ SDH Mapper
HUDSON (S19203)	Variable Rate Digital Wrapper Framer/Deframer, Performance Monitor, and FEC Device
MEKONG (S19204)	STS-192 Pointer Processor
KHATANGA (S19205)	STS-192c SONET/SDH Framer/Mapper with Integrated MAC
S3390	10 Gbps TIA

– At a Glance –

General Features

- Operational from 9.953 Gbps to 11.1 Gbps
- Low Power (1100 mW Typical)
- 1.2 V and 1.8/2.5/3.3 V Power Supply
- Built-In Self Test (BIST) Feature with error counter
- On-chip High-Frequency PLL for Clock Generation and Clock Recovery
- 16-bit LVDS Parallel Data Path
- TX and RX Lock Detect Indication
- Serial and Reference Loop Timing Modes
- Line and Diagnostic Loopback Mode for Faulty Node Identification
- Operational Temperature Range Up to 85°C
- Supports Management Data Bus for Control I/O
- Complies with OIF SFI-4/ Telecordia/ITU-T Specifications
- 255 PBGA package

Transmitter Features

- Reference frequency of 155.52 or 622.08 MHz (or equivalent FEC/ 10GbE rate)

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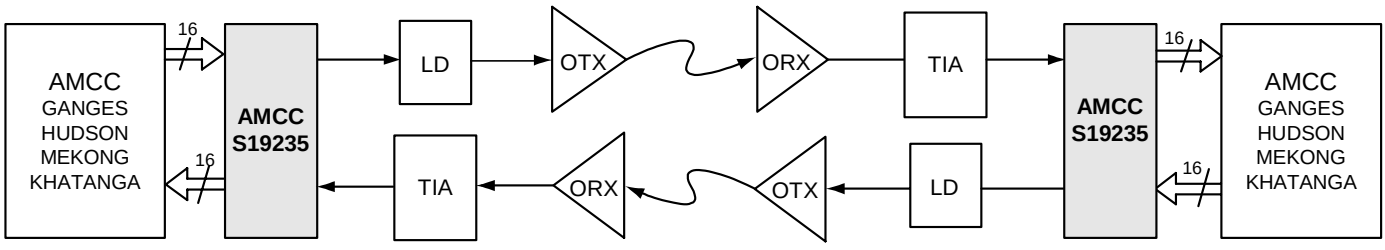

Figure 1. System Block Diagram

The sequence of operations is as follows:

Transmitter Operations

1. 16-bit parallel input
2. Parallel-to-serial conversion
3. Serial data output

Receiver Operations

1. Serial input to limiting post-amp
2. Clock and Data recovery
3. Serial-to-parallel conversion
4. 16-bit parallel data and clock output

Internal clocking and control functions are transparent to the user.

Prefix	Device	Package
S – Integrated Circuit	19235	PB11

X	XXXXX	XX
Prefix	Device	Package

Figure 2. S19235 Ordering Information

Transmitter Features *(cont.)*

- 155.52 MHz and 622.08 MHz (or equivalent FEC/10GbE rate) clock outputs
- Internal, self-initializing FIFO to decouple transmit clocks
- Programmable TSD output differential swing (for XFP and other applications)

Receiver Features

- Recovers clock from 9.953 to 11.1 Gbps
- Adaptive Post-Amplifier offset adjust for duty cycle distortion correction
- Post-Amplifier equalization adjust for 10 GbE jitter tolerance
- Reference frequency of 155.52 MHz (or equivalent FEC/ 10GbE rate)

Applications

- SONET/SDH-based transmission systems
- SONET/SDH modules
- 10GbE based transmission systems
- Section repeaters
- Add Drop Multiplexers (ADM)
- Broad-band cross-connects
- Fiber Optic Terminators
- Fiber Optic Test Equipment

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