# Features

- **Saifun NROM™ Flash Cell**
- **Serial Peripheral Interface (SPI) Compatible**
- **Supports SPI Modes 0 (0,0) and 3 (1,1)**
- **Byte and Page Write Modes (up to 128 bytes)**
- **Single Supply Voltage:**
  - **2.7V to 3.6V (L)**
  - **4.5V to 5.5V (H)**
- **10MHz Clock Rate**
- **Block Write Protection:**
  - **Protect ¼, ½, or Entire Array**
- **Write Protect Pin and Write Disable Instructions of both Hardware and Software Data Protection**
- **Self-timed Write Cycle (10mS max)**
- **100,000 Write Cycles (Minimum)**
- **20 Year Data Retention**
- **Low-power Standby Current (less than 1µA)**
- **8-SOIC Narrow Package (0.150" Wide Body, JEDEC SOIC)**
- **Temperature Range:**
  - **Industrial: -40°C to +85°C**
  - **Commercial: 0°C to +70°C**

# General Description

SA25C1024 is a 1Mb CMOS non-volatile serial EEPROM, organized as a 128K x 8-bit memory. The SA25C1024 is available in a space-saving, 8-lead narrow SOIC package. In addition, it is available in a wide range of voltages – 2.7-3.6 V and 4.5-5.5 V.

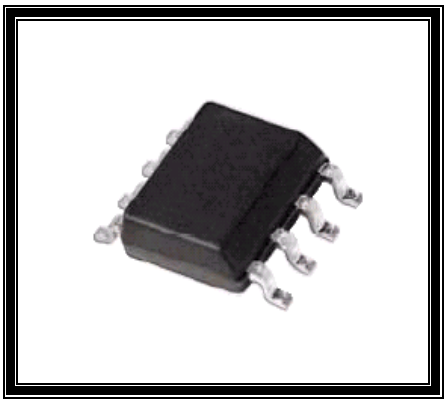
The SA25C1024 is enabled through the Chip Select (CSb) pin and is accessed via a 3-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO) and Serial Data Clock (SCK). All write cycles are completely self-timed, and no separate ERASE cycle is required before write.

(continued)

SAIFUN SEMICONDUCTORS LTD.

# SA25C1024 Data Sheet

## 1Mb EEPROM SPI with 10MHz and Low Standby





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# General Description

(continued)

Programming the status register with top ¼, top ½ or entire array write protection enables BLOCK WRITE protection. Separate program enable and program disable instructions are provided for additional data protection. Hardware data protection is provided via the WPb pin to protect against inadvertent write attempts to the status register. The HOLDb pin may be used to suspend any serial communication without resetting the serial sequence.

# Connection Diagrams

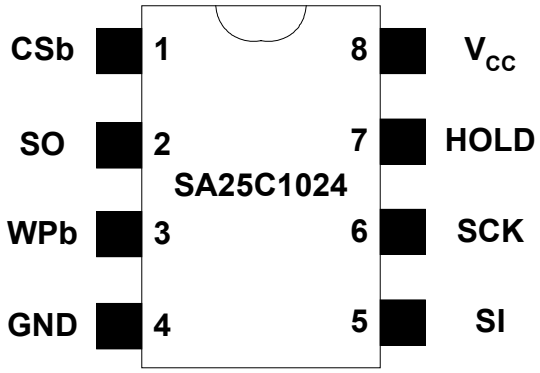



**Figure 1. SOIC 8 – Narrow/PDIP Package (Top View)**

**Table 1. Pin Names**

| Pin Name | Function |
|---|---|
| CSb | Chip Select |
| SCK | Serial Data Clock |
| SI | Serial Data Input |
| SO | Serial Data Output |
| GND | Ground |
| $V_{CC}$ | Power Supply |
| WPb | Write Protect |
| HOLDb | Suspend Serial Input |

# Ordering Information

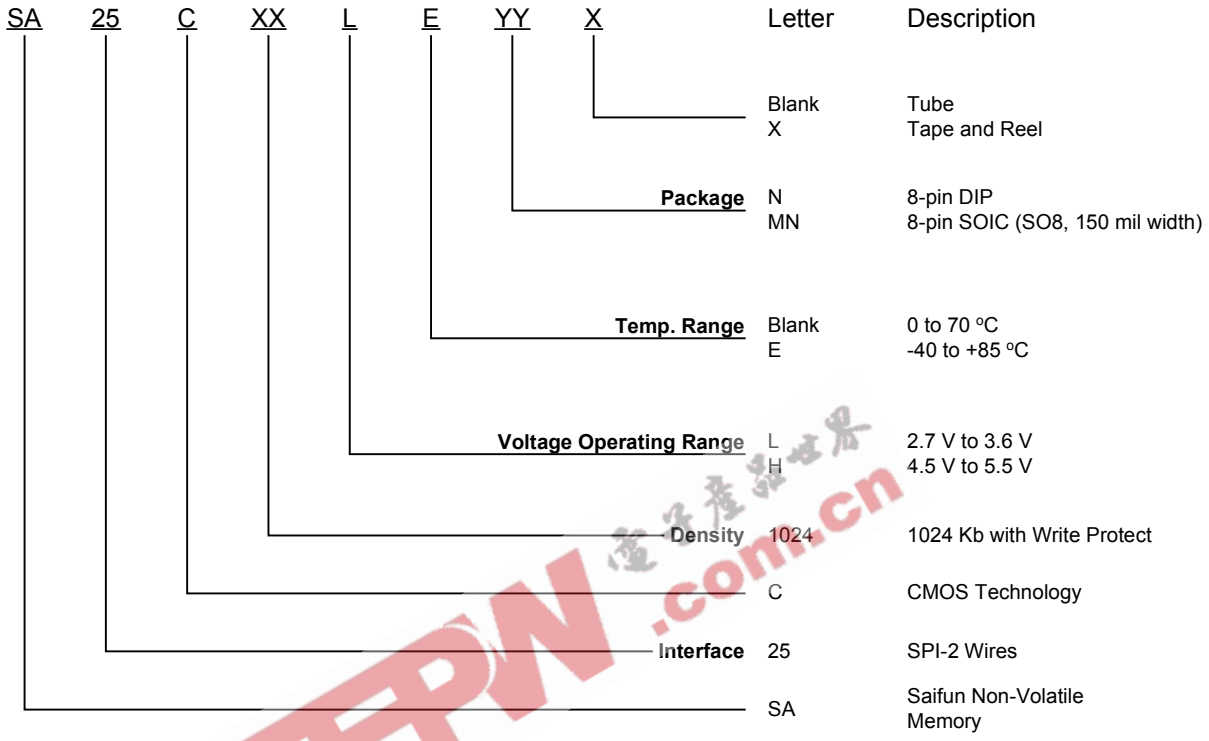



**Figure 2: SA25C1024 Ordering Information**

# Product Specifications

## Absolute Maximum Ratings

| | |
|---|---|
| Ambient Storage Temperature | -65 °C to +150 °C |
| All input or output voltages with respect to Ground | 4.5 V to -0.3 V (L)<br>6.5 V to -0.3 V (H) |
| Lead Temperature (Soldering, 10 seconds) | +235 °C |

## Latch Up Specifications

| | |
|---|---|
| Latch Up | 100 mA on all pins, +125°C |

## ESD Specifications

| | |
|---|---|
| Human Body Model | Per MIL-STD 883 Method 3015.7 |
| Voltage Levels | 500 V to 5 KV, in increments of 500 V; proceed to 8000 V or until failure |
| Machine Model | Per JEDEC standard JESD22-A115 |
| Voltage levels | 50 V to 300 V, in increments of 50 V; proceed to 500 V or until failure |

## Operating Conditions

| | |
|---|---|
| Ambient Operating Temperature: | |
| SA25C1024 | 0 °C to +70 °C |
| SA25C1024E | -40 °C to +85 °C |
| Positive Power Supply: | |
| SA25C1024L | 2.7 V to 3.6 V |
| SA25C1024H | 4.5 V to 5.5 V |

# DC Characteristics

Applicable over recommended operating range from:

- $T_{AI}$ = -40 ºC to 85 ºC, $V_{CC}$ = 2.7-3.6 V/4.5-5.5 V
- $T_{AC}$ = 0 ºC to 70 ºC, $V_{CC}$ = 2.7-3.6 V/4.5-5.5 V

**Table 2. DC Characteristics**

| Symbol | Parameter | Test Conditions | | Limits | | | Unit | Comments |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ* | Max | | |
| $V_{CC}$ | Supply Voltage | | | 2.7 | 3 | 3.6 | V | L |
| | | | | 4.5 | 5 | 5.5 | V | H |
| $I_{CC1}$ | Active Power Supply Current (Read) | $F_{SCK}$ = 5 MHz, $V_{CC}$ = 5.0 V | | | 4 | 8 | mA | L |
| | | $F_{SCK}$ = 2 MHz, $V_{CC}$ = 5.0 V | | | 4 | | mA | L |
| | | $F_{SCK}$ = 5 MHz, $V_{CC}$ = 3.0 V | | | 4 | 8 | mA | H |
| | | $F_{SCK}$ = 2 MHz, $V_{CC}$ = 3.0 V | | | 4 | | mA | H |
| $I_{CC2}$ | Active Power Supply Current (Write) | Fwrite = 5 MHz, Twrite = 10 ms | | | 10 | 15 | mA | L |
| | | Fwrite = 2 MHz, Twrite = 10 ms | | | 10 | | mA | L |
| | | Fwrite = 5 MHz, Twrite = 10 ms | | | 10 | 15 | mA | H |
| | | Fwrite = 2 MHz, Twrite = 10 ms | | | 10 | | mA | H |
| $I_{SB}$ | Standby Current | $V_{CC}$ = 3.0 V, CSb = $V_{CC}$ | | | | 1 | µA | L |
| | | $V_{CC}$ = 5.0 V CSb = $V_{CC}$ | | | | 10 | µA | H |
| $I_{IL}$ | Input Leakage Current | $V_{IN}$ = GND to $V_{CC}$ | | | | 1 | µA | |
| $I_{OL}$ | Output Leakage Current | $V_{IN}$ = GND to $V_{CC}$ | | | | 1 | µA | |
| $V_{IL}$ | Input Low Voltage | | | -0.3 | | 0.3 $V_{CC}$ | V | |
| $V_{IH}$ | Input High Voltage | | | 0.7 $V_{CC}$ | | $V_{CC}$ + 0.5 | V | |
| $V_{OL}$ | Output Low Voltage | | IOL = 0.15 mA | | | 0.2 | V | L |
| $V_{OH}$ | Output High Voltage | | IOH = -0.1 mA | $V_{CC}$ - 0.2 | | | V | L |
| $V_{OL}$ | Output Low Voltage | | IOL = 3.0 mA | | | 0.4 | V | H |
| $V_{OH}$ | Output High Voltage | | IOH = -1.6 mA | $V_{CC}$ - 0.8 | | | V | H |

*Typical values are at $T_{AI}$ = 25 ºC and 3 V/5 V.

# AC Test Conditions

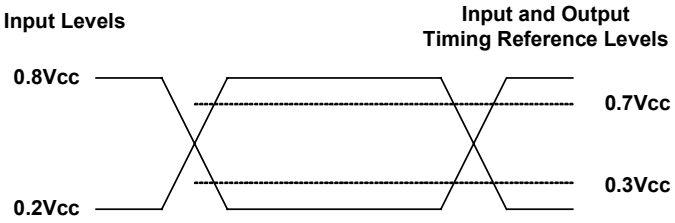



**Figure 3. AC Measurements I/O Waveform**

**Table 3. AC Measurements**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $C_L$ | Load Capacitance | 30 | | PF |
| | Input Rise and Fall Times | | 5 | NS |
| | Input Pulse Voltage | 0.2 $V_{CC}$ to 0.8 $V_{CC}$ | | V |
| | Input and Output Timing Reference Voltages | 0.3 $V_{CC}$ to 0.7 $V_{CC}$ | | V |

**Table 4. AC Characteristics**

| Symbol | Parameter | 10 MHz | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $F_{SCK}$ | SCK Clock Frequency | | | 10 | MHz |
| $t_{WH}$ | SCK High Time | 40 | | | ns |
| $t_{WL}$ | SCK Low Time | 40 | | | ns |
| $t_{CS}$ | CSb High Time | 50 | | | ns |
| $t_{CSS}$ | CSb Setup Time | 50 | | | ns |
| $t_{CSH}$ | CSb HOLD Time | 50 | | | ns |
| $t_{HD}$ | HOLD Time | 25 | | | ns |
| $t_{CD}$ | HOLDB HOLD Time | 25 | | | ns |
| $t_V$ | Output Valid | 0 | | 40 | ns |
| $t_{HO}$ | Output HOLD Time | 0 | | | ns |
| $t_{HD:DAT}$ | Data in HOLD Time | 15 | | | ns |
| $t_{SU:DAT}$ | Data in Setup Time | 12 | | | ns |
| $t_R$ | Input Rise Time | | | 2 | ns |
| $t_F$ | Input Fall Time | | | 2 | ns |
| $t_{LZ}$ | HOLDb to Output Low Z | | | 100 | ns |
| $t_{HZ}$ | HOLDb to Output High Z | | | 100 | ns |
| $t_{DIS}$ | Output Disable Time | | | 100 | ns |
| $t_{WC}$* | 128-byte Page | | 8 | | ms |
| Endurance | | 100K | | | Write cycles |

* 128 bytes in the checkerboard programming formation; a maximum of 50% of the array is programmed.

# Serial Interface Description

## Master

The device that generates the SCK.

## Slave

As the SCK pin is always an input, the SA25C1024 always operates as a slave.

## Transmitter/Receiver

The SA25C1024 has separate pins designated for data transmission and reception.

## Serial Opcode

The first byte is received after the device is selected. This byte contains the opcode that defines the operation to be performed (for more details, refer to Table 5, page 10).

## Invalid Opcode

If an invalid opcode is received, no data is shifted into the SA25C1024, and the serial output pin remains in a high impedance state until a CSb falling edge is detected again, which reinitializes the serial communication.

## Chip Select (CSb)

The SA25C1024 is selected when the CSb pin is low. When the device is not selected, data is not accepted via the SI pin, and the SO pin remains in a high impedance state.

## HOLDb

The HOLDb pin is used in conjunction with the CSb pin to select the SA25C1024. When the device is selected and a serial sequence is underway, HOLDb can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the HOLDb pin must be brought low while the SCK pin is low. To resume serial communication, the HOLDb pin is brought high while the SCK pin is low (SCK may still toggle during HOLDb). Inputs to the SI pin are ignored while the SO pin is in the high impedance state.

## Write Protect

The WPb pin enables write operations to the Status register when held high. When the WPb pin is brought low and the WPBEN bit is 1, all write operations to the status register are inhibited (for more details, refer to Table 8, page 11). If WPb goes low while CSb is still low, the write to the status register is interrupted. If the internal write cycle has already been initiated, WPb going low has no effect on any write operation to the status register. The WPb pin function is blocked when the WPBEN bit in the status register is 0, which enables the user to install the SA25F020 in a system with the WPb pin tied to ground but still able to write to the status register. All WPb pin functions are enabled when the WPBEN bit is set to 1.

# Functional Description

Figure 4 presents a schematic diagram of the SPI serial interface.

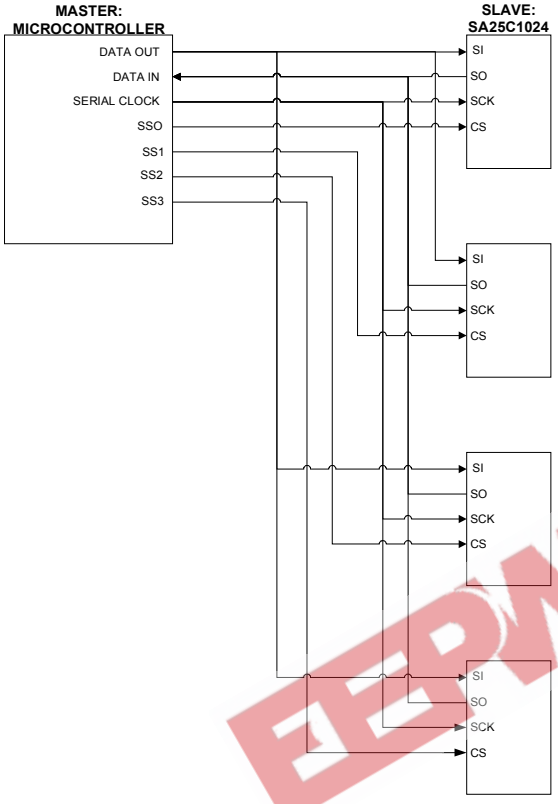



**Figure 4. SPI Serial Interface**

The SA25C1024's SPI consists of an 8-bit instruction register that decodes a specific instruction to be executed. Six different instructions (called *opcodes*) are incorporated in the device for various operations. Table 5 lists the instructions set and the format for proper operation. All opcodes, array addresses and data are transferred in an MSB-first-LSB-last fashion. Detailed information about each of these opcodes is provided under individual instruction descriptions in the sections that follow.

**Table 5. Instruction Set**

| Instruction Name | Instruction Format | Operation |
|---|---|---|
| WREN | 0000X110 | Set Write Enable Latch |
| WRDI | 0000X100 | Reset Write Enable Latch |
| RDSR | 0000X101 | Read Status Register |
| WRSR | 0000X001 | Write Status Register |
| READ | 0000X011 | Read Data from Memory Array |
| WRITE | 0000X010 | Write Data to Memory Array |

In addition to the instruction register, the device also contains an 8-bit status register that can be accessed by RDSR and WRSR instructions. The byte defines the Block Write Protection (BP1 and BP0) levels, Write Enable (WEN) status, Busy/Rdy (/RDY) status and Hardware Write Protect (WPBEN) status of the device. Table 6 illustrates the format of the status register.

**Table 6. Status Register Format**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| WPBEN | X | X | X | BP1 | BP0 | WEN | /RDY |

## Write Enable (WREN)

The device powers up in the Write Disable state when $V_{CC}$ is applied. All programming instructions must be preceded by a WREN instruction.

## Write Disable (WRDI)

To protect the device against inadvertent writes, the WRDI instruction disables all programming modes. The WRDI instruction is independent of the WP pin's status.

## Read Status Register (RDSR)

The RDSR instruction provides read access to the status register. The BUSY/RDY and WREN statuses of the device can also be determined by this instruction. In addition, the Block Write Protection bits indicate the extent of protection employed. In order to determine the status of the device, the value of the /RDY bit can be continuously polled before sending any write instruction.

## Write Status Register (WRSR)

The WRSR instruction enables the user to select one of four levels of protection. The SA25C1024 is divided into four array segments. The top quarter, top half or all of the memory segments can be protected (for more details, refer to Table 7). The data within a selected segment is therefore read-only.

**Table 7. Block Write Protect Bits**

| Level | Status Register Bits | | Array Addresses Protected |
|---|---|---|---|
| | BP1 | BP0 | |
| 0 | 0 | 0 | None |
| 1/4 | 0 | 1 | 18000 - 1FFFF |
| 1/2 | 1 | 0 | 10000 - 1FFFF |
| All | 1 | 1 | 00000 - 1FFFF |

The WRSR instruction (as shown in Table 8) also allows the user to enable or disable the WPb pin via the WPBEN bit. Hardware write protection is enabled when the WPb pin is low and the WPBEN bit is 1, and disabled when either the WP pin is high or the WPBEN bit is 0. When the device is hardware write protected, writes to the status register are disabled.

**NOTE:**

When the WPBEN bit is hardware write protected, it cannot be changed back to 0 as long as the WPb pin is held low.

**Table 8. WPBEN Operation**

| WPb | WPBEN | WEN | Protected Blocks | Un-protected Blocks | Status Register |
|---|---|---|---|---|---|
| X | 0 | 0 | Protected | Protected | Protected |
| X | 0 | 1 | Protected | Writable | Writable |
| Low | 1 | 0 | Protected | Protected | Protected |
| Low | 1 | 1 | Protected | Writable | Protected |
| High | X | 0 | Protected | Protected | Protected |
| High | X | 1 | Protected | Writable | Writable |

## Read Sequence (READ)

Reading the SA25C1024 via the SO pin requires the following sequence (for more details, see Table 9, page 12):

1. After the CSb line is pulled low to select the device, the READ opcode is transmitted via the SI line, followed by the byte address to be read. Upon completion, any data on the SI line is ignored.
2. The data (D7-D0) at the specified address is then shifted out onto the SO line.

If only one byte is to be read, the CSb line should be driven high after the data comes out. The READ sequence can be continued, as the byte address is automatically incremented and data continues to shift out. When the highest address is reached, the address counter rolls over to the lowest address, enabling the entire memory to be read in one continuous READ cycle.

**Table 9. Read Status Register Definition**

| Bit | Definition |
|---|---|
| Bit 0 (/RDY) | Bit 0 = 0 (/RDY) indicates that the device is READY.<br>Bit 0 = 1 indicates that a write cycle is in progress. |
| Bit 1 (WEN) | Bit 1 = 0 indicates that the device is not write enabled.<br>Bit 1 = 1 indicates that the device is write enabled. |
| Bit 2 (BP0) | Block Write Protect Bit 0 |
| Bit 3 (BP1) | Block Write Protect Bit 1 |
| Bit 7 (WPBEN) | Write Protect Mode Enable Bit |

Bits 4-6 are 0s when the device is not in an internal write cycle; bits 0-7 are 1s during an internal write cycle.

## Write Sequence (WRITE)

Two separate instructions must be executed in order to write to the SA25C1024. The device must first be write enabled via the WREN instruction, and then a WRITE instruction may be executed. The address of the memory locations to be written must be outside the protected address field location selected by the Block Write Protection level. During an internal write cycle, all commands are ignored except the RDSR instruction.

A WRITE instruction requires the following sequence:

1. After the CSb line is pulled low to select the device, the WRITE opcode is transmitted via the SI line, followed by the byte address and the data (D7-D0) to be written.
2. Programming starts after the CSb pin is brought high. The CSb pin's low-to-high transition must occur during the SCK low time, immediately after clock in the D0 (LSB) data bit.

The SA25C1024 is capable of up to a 128-byte (from 1 to 128 bytes) PAGE write operation. After each byte is received, the eight low-order address bits are internally incremented by one. If more than 128 bytes of data are transmitted, the address counter rolls over and the previously written data is overwritten. The SA25C1024 is automatically returned to the write disable state at the completion of a write cycle.

**NOTE:**

If the device is not write enabled, the device ignores the WRITE instruction and returns to the standby state when CSb is brought high. A new CSb falling edge is required to re-initiate the serial communication.

# Timing Diagrams

All timing diagrams are based on SPI protocol modes 0 and 1.

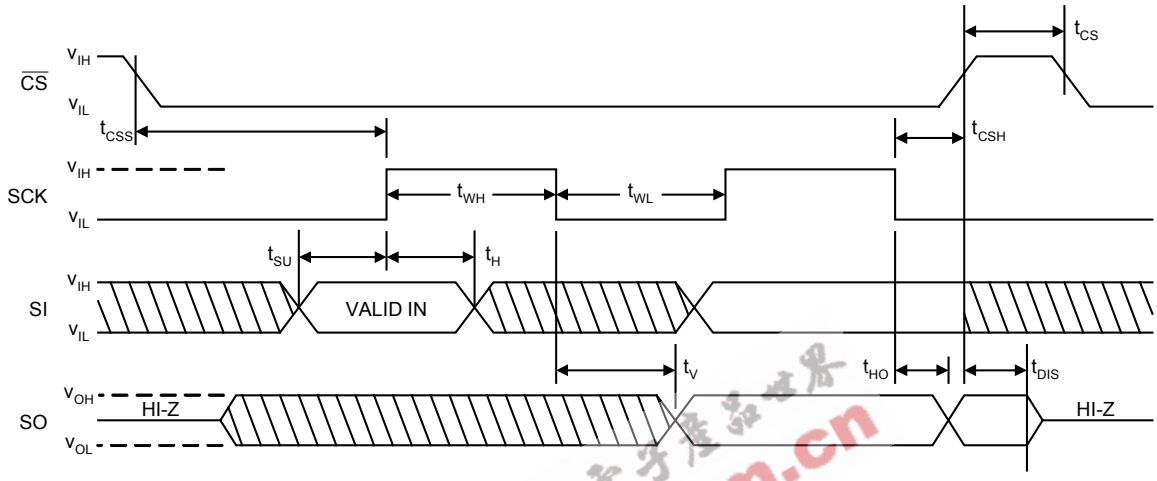



**Figure 5. SPI Mode 0 (0,0) Timing**

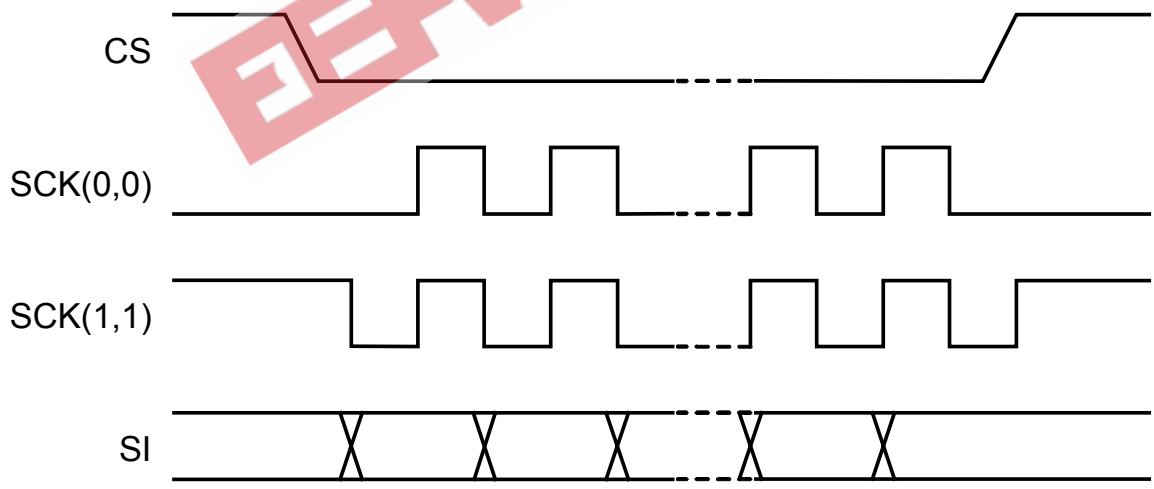



**Figure 6. SPI Mode 0 (0,0) and 3 (1,1) Timing**

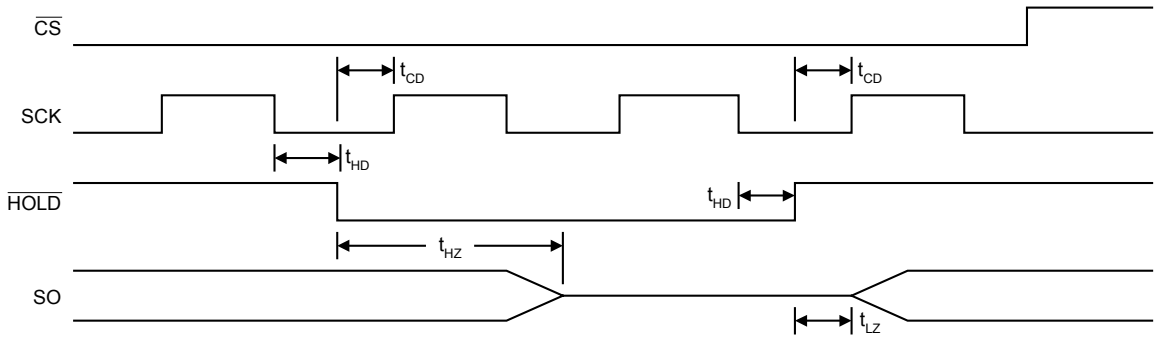



**Figure 7. HOLDb Timing**

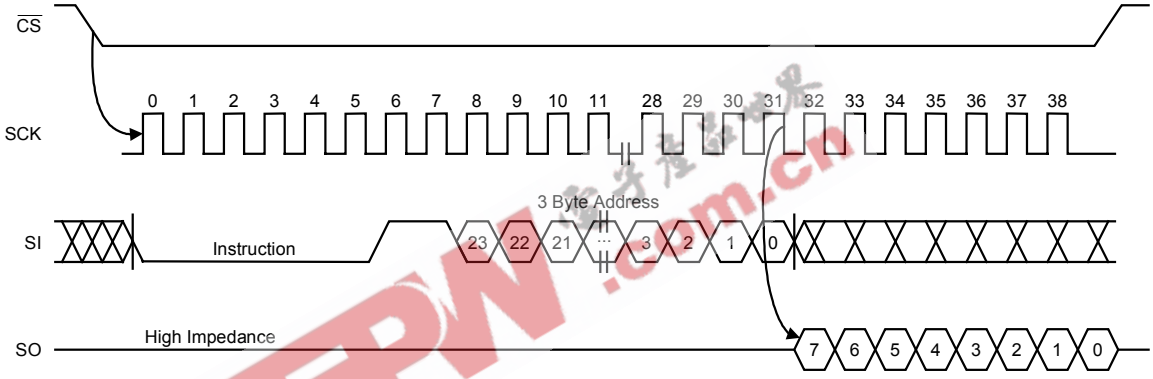



**Figure 8. Read Timing**

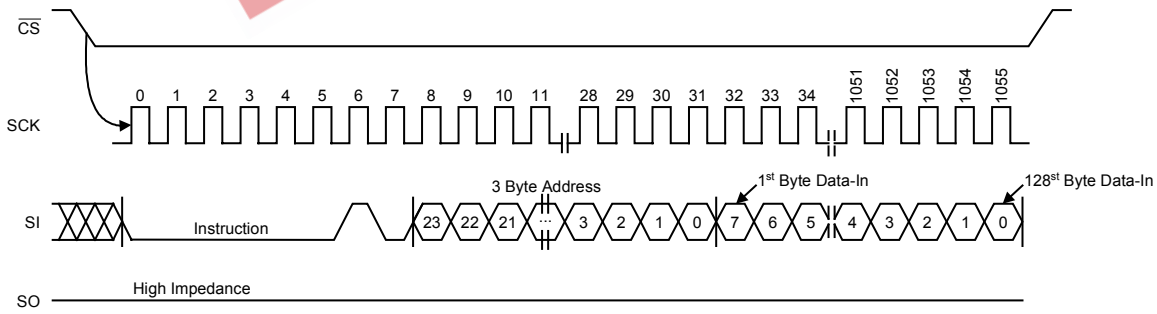



**Figure 9. Write Timing**

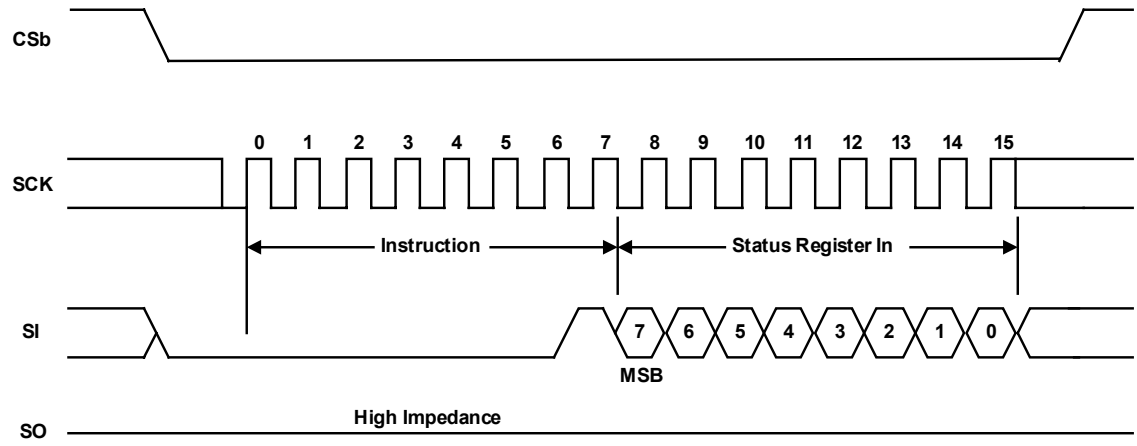



**Figure 10. Write Status Register Timing**

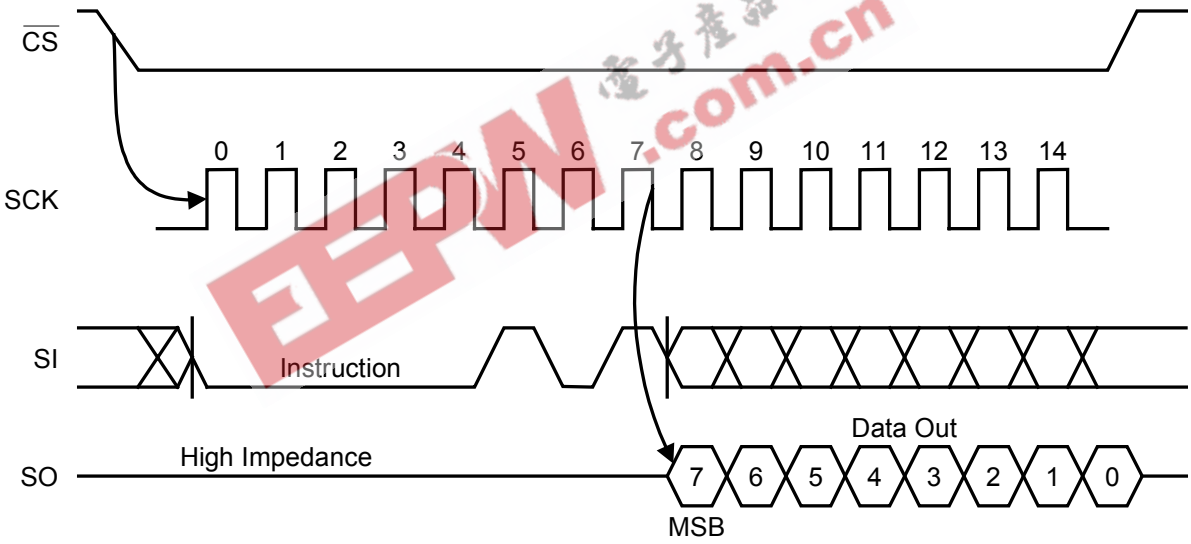
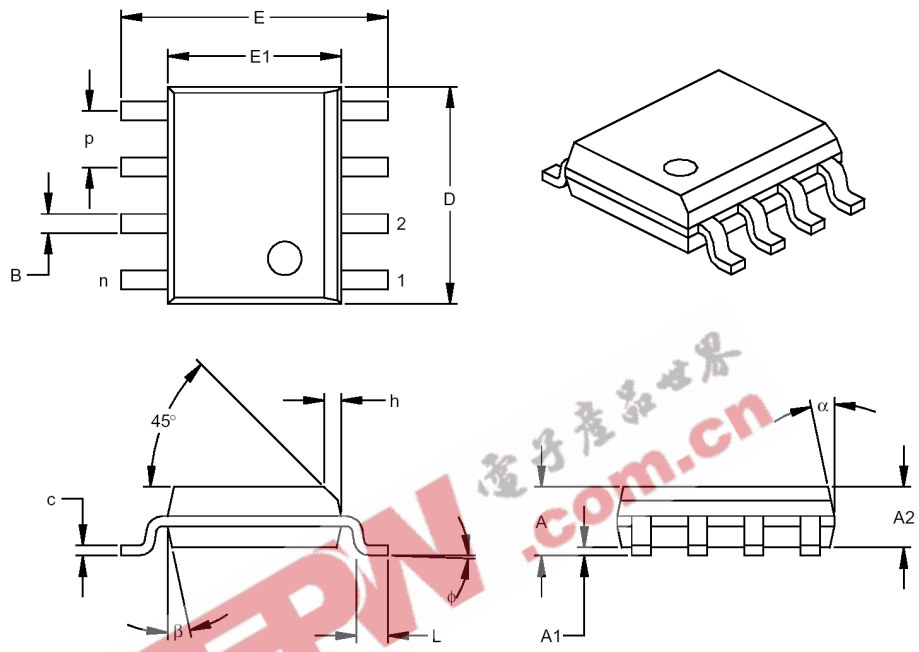



**Figure 11. Read Status Register Timing**

# Physical Dimensions

All measurements are in inches (millimeters), unless otherwise specified.




| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 8 | | | 8 | |
| Pitch | p | | .050 | | | 1.27 | |
| Overall Height | A | .053 | .061 | .069 | 1.35 | 1.55 | 1.75 |
| Molded Package Thickness | A2 | .052 | .056 | .061 | 1.32 | 1.42 | 1.55 |
| Standoff § | A1 | .004 | .007 | .010 | 0.10 | 0.18 | 0.25 |
| Overall Width | E | .228 | .237 | .244 | 5.79 | 6.02 | 6.20 |
| Molded Package Width | E1 | .146 | .154 | .157 | 3.71 | 3.91 | 3.99 |
| Overall Length | D | .189 | .193 | .197 | 4.80 | 4.90 | 5.00 |
| Chamfer Distance | h | .010 | .015 | .020 | 0.25 | 0.38 | 0.51 |
| Foot Length | L | .019 | .025 | .030 | 0.48 | 0.62 | 0.76 |
| Foot Angle | φ | 0 | 4 | 8 | 0 | 4 | 8 |
| Lead Thickness | c | .008 | .009 | .010 | 0.20 | 0.23 | 0.25 |
| Lead Width | B | .013 | .017 | .020 | 0.33 | 0.42 | 0.51 |
| Mold Draft Angle Top | α | 0 | 12 | 15 | 0 | 12 | 15 |
| Mold Draft Angle Bottom | β | 0 | 12 | 15 | 0 | 12 | 15 |

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

**Figure 12. 8-pin SOIC Package**

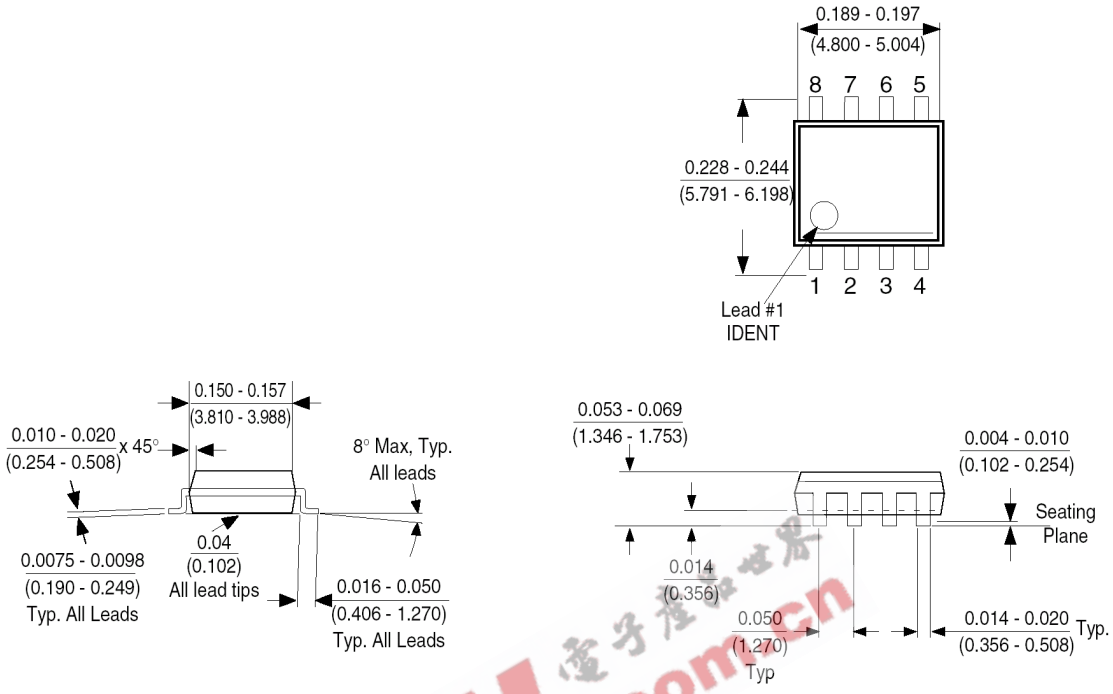



**Figure 13. 8-pin Molded Small Outline Package (MN), 0.150" Wide Body, JEDEC SOIC**

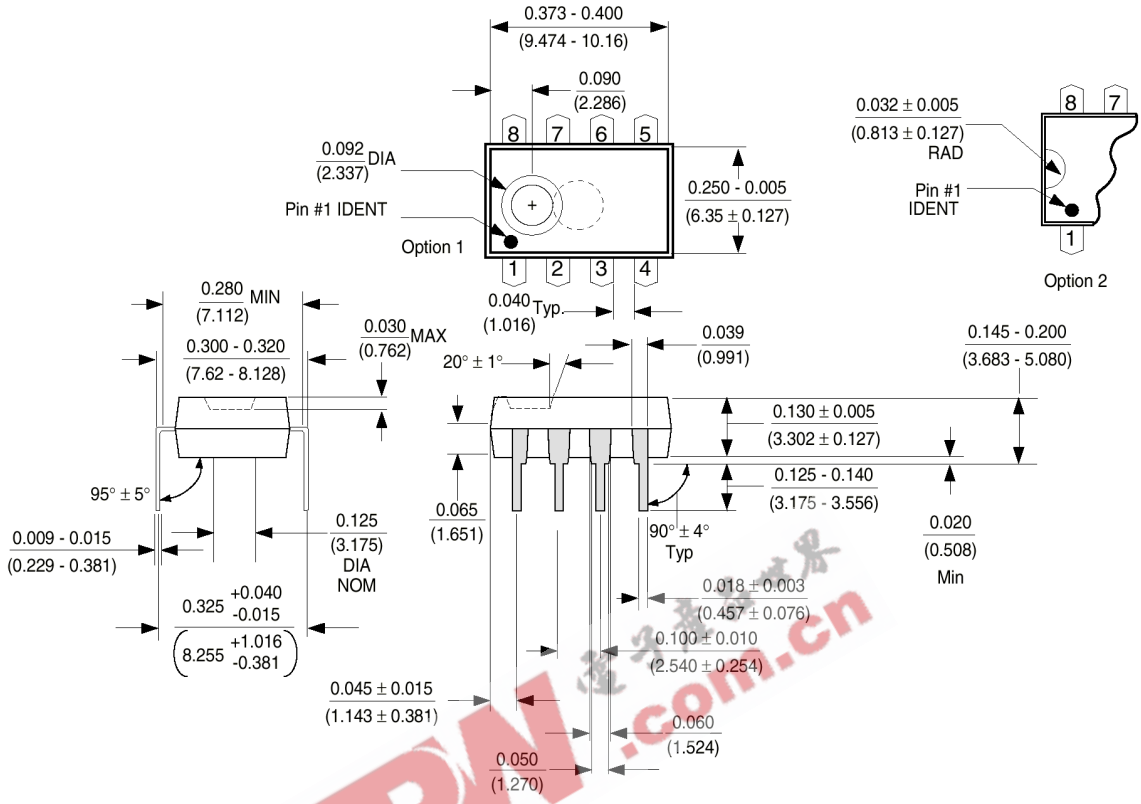



**Figure 14. Molded Dual-in-line Package (N) Package Number N08E**

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## Revision History

| Rev | Date | Description of Change | Amendment |
|---|---|---|---|
| 1.0 | 1-Sep-02 | Initial Release | 0 |
| 1.1 | 27-Jan-03 | ESD scheme modification | 1 |

| Prepared by | Approved by | Approved by | Signature | Date |
|---|---|---|---|---|
| Golan M. Shalhov<br>Product Line Manager | Shai Eisen<br>Design Project Manager | Doron Vertesh<br>Director EEPROM SBU | | 27-Jan-03 |



# Life Support Policy

Saifun's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Saifun Semiconductors Ltd. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.