## Product List

SM89S16R1L25, 25MHz 64KB internal flash MCU
SM89S16R1C25, 25MHz 64KB internal flash MCU
SM89S16R1C40, 40MHz 64KB internal flash MCU

## General Description

The SM89S16R1 is a single-chip 8-bits micro-controller manufactured in an advanced CMOS process with on chip flash memory. It supports a derivative of the 80C51 microcontroller family. The SM89S16R1 has the same instructions set as the 80C51.
The SM89S16R1 contains a 64K x 8 bits on chip program flash, a volatile 1024 x 8 bits data RAM, four 8-bits I/O ports, one 4-bits I/O port, two 16-bits timer/event counters, and an additional 16-bits timer coupled to capture and compare latches, a two-priority-level, nested interrupt structure, two PWM clock outputs, one serial interfaces (UART bus). For system that requires extra capability the SM89S16R1 can be expanded using standard TTL and LVTTL compatible memory and logic.
In addition, The SM89S16R1 has two software selectable modes of power saving – IDLE mode and POWER-DOWN mode. The IDLE mode freezes the CPU while allowing the RAM, timer, serial ports, and interrupt system to continue functioning. The POWER-DOWN mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

## Feature

- Working Voltage: 3.3V or 5.0V.
- 80C51 Central Processor Unit (CPU).
- 64K x 8 bits on chip flash memory.
- 1024 x 8 bits RAM, expandable externally to 64KB.
- Two standard 16-bits timers/counters
- An additional 16-bits timer/counter coupled to a capture and compare register.
- Two 8-bits / 5-bits resolution Pulse-Width-Modulation (PWM) outputs
- Four 8-bits I/O ports.(For PDIP package)
- Four 8-bits I/O ports plus one 4-bits I/O port. (For PLCC or QFP package)
- Full-duplex UART
- 8 interrupt sources with 2 priority levels
- Extended temperature range (-40℃ to +85℃)
- Software enable/disable ALE output pulse
- Wake-up from POWER-DOWN mode by INT0/INT1, RTCI or H/W RESET.
- RTC (Real Time Clock) function.
- Four channels 6-bits Analog to Digital Converter (ADC).

## Ordering Information

SM89S16R1ihhk
yymmv

i: process identifier {L=3.0V~3.6V,C=4.5V~ 5.5V}
hh: working clock in MHz {25, 40}
k: package type postfix {as below table}
yy: year mm: month
v: version identifier { , A, B, ...}

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**Package Spec.**

| Package | Pin / PAD | Frequency |
|---|---|---|
| 44L PQFP | Figure 1 | 25 MHz at 3.3V and 40MHz at 5V |
| 44L PLCC | Figure 2 | 25 MHz at 3.3V and 40MHz at 5V |
| 40L PDIP | Figure 3 | 25 MHz at 3.3V and 40MHz at 5V |

## Pin Configuration

Figure 1 44L PQFP Package

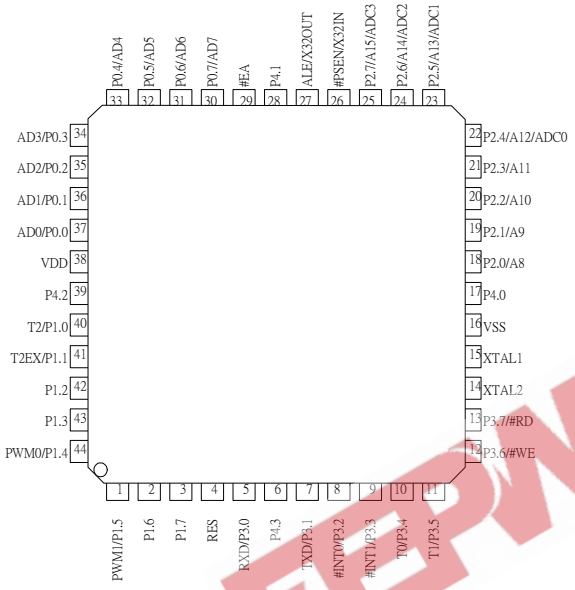



Figure 2 44L PLCC Package

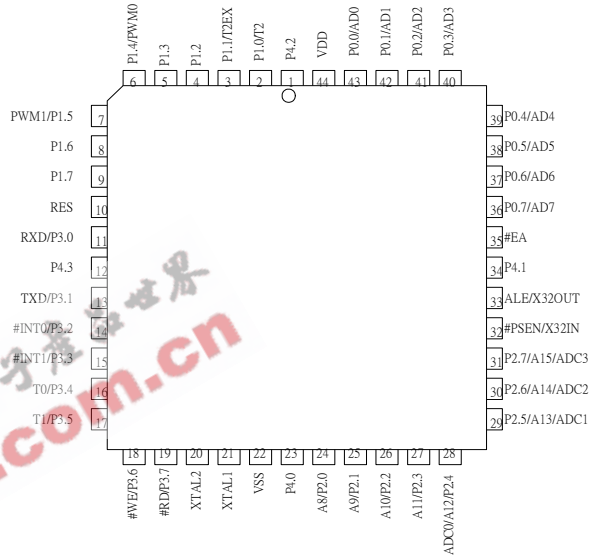
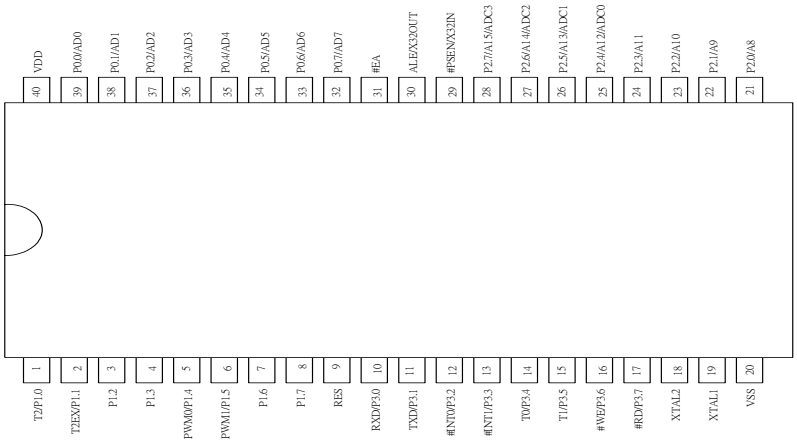



Figure 3 40L PDIP Package



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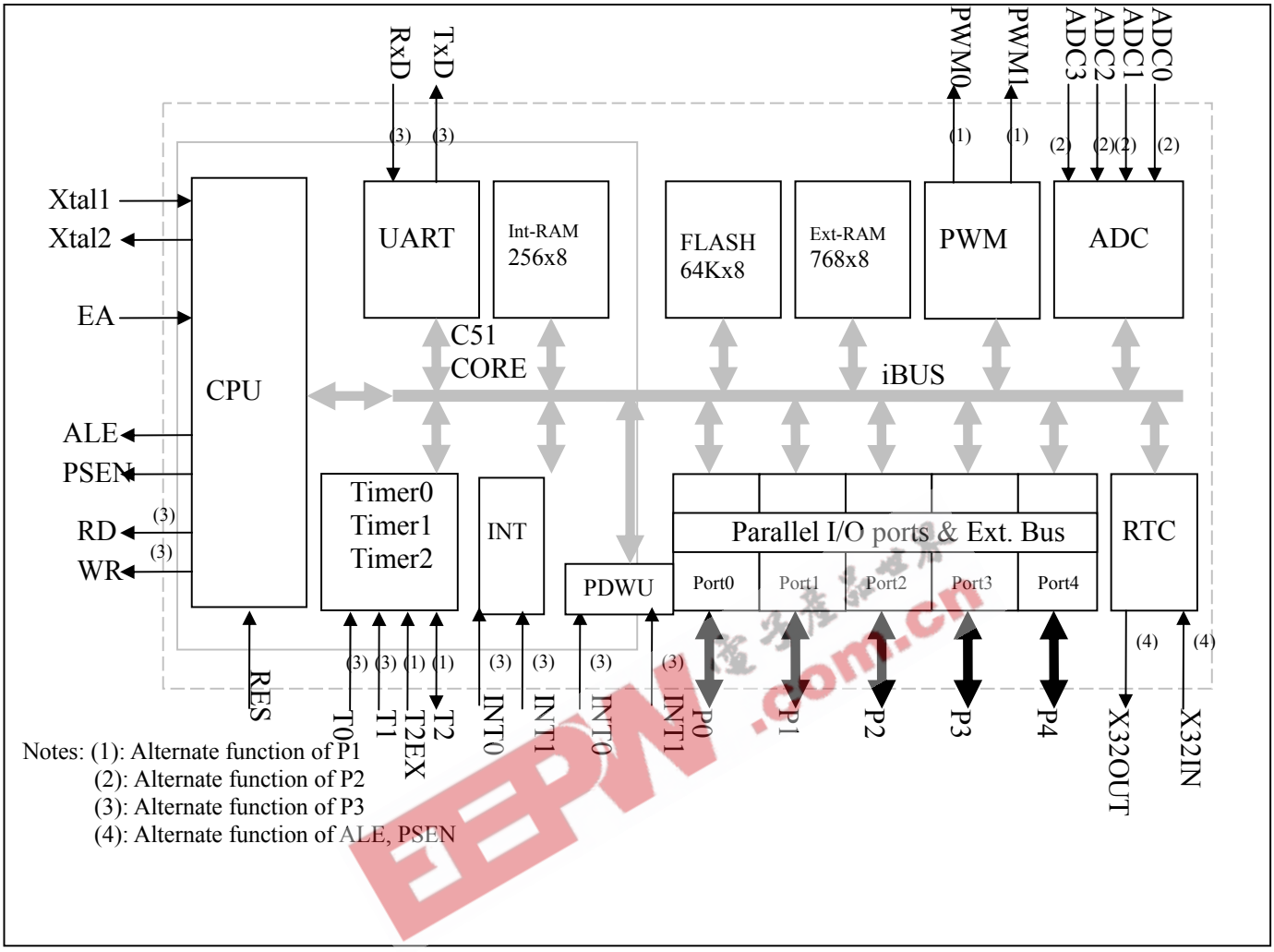
## Block Diagram




Notes: (1): Alternate function of P1
(2): Alternate function of P2
(3): Alternate function of P3
(4): Alternate function of ALE, PSEN

# Pin Description

| MNEMONIC | PDIP 40 pin | PQFP 44 Pin | PLCC 44 pin | Names and Functions |
|---|---|---|---|---|
| VDD | 40 | 38 | 44 | **Power supply:**<br>+5V or +3.3V power supply pin during normal operations and power saving modes. |
| P0.0 – P0.7 | 39,38,37,36<br>35,34,33,32 | 37,36,35,34<br>33,32,31,30 | 43,42,41,40<br>39,38,37,36 | **Port 0**:<br>Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them become floating and can be used as high- impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s.<br>Port Pin Alternative function<br>P0.0 AD0<br>P0.1 AD1<br>P0.2 AD2<br>P0.3 AD3<br>P0.4 AD4<br>P0.5 AD5<br>P0.6 AD6<br>P0.7 AD7 |
| P1.0 – P1.7 | 1,2,3,4,<br>5,6,7,8 | 40,41,42,43,<br>44,1,2,3 | 2,3,4,5,<br>6,7,8,9 | **Port 1**:<br>An 8-bits bidirectional I/O port with internal pull-ups on all pins. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: IIL).<br>Port Pin Alternative function<br>P1.0 T2: TIMER2 clock output<br>P1.1 T2EX: TIMER2 reload/capture DIR.<br>P1.4 PWM0: PWM channel 0 output<br>P1.5 PWM1: PWM channel 1 output |
| RST | 9 | 4 | 10 | **Reset**:<br>A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal resistor to VSS permits a power-on reset using only an external capacitor to VCC. |
| P2.0 – P2.7 | 21,22,23,24,<br>25,26,27,28 | 18,19,20,21<br>22,23,24,25 | 24,25,26,27,<br>28,29,30,31 | **Port 2:**<br>Port 2 is an 8-bits bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: IIL). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that uses 16-bits addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that uses 8-bits addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.<br>Port Pin Alternative function<br>P2.0 A8<br>P2.1 A9<br>P2.2 A10<br>P2.3 A11<br>P2.4 A12/ADC0<br>P2.5 A13/ADC1<br>P2.6 A14/ADC2<br>P2.7 A15/ADC3 |

| MNEMONIC | PDIP 40 pin | PQFP 44 Pin | PLCC 44 pin | Names and Functions |
|---|---|---|---|---|
| P3.0 – P3.7 | 10,11,12,13<br>14,15,16,17 | 5,7,8,9,<br>10,11,12,13 | 11, 13,14,15,<br>16,17,18,19 | **Port 3**:<br>Port 3 is an 8-bits bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: IIL). Port 3 also serves the special features.<br>Port Pin Alternative function<br>P3.0 RxD UART input<br>P3.1 TxD UART output<br>P3.2 #EX0 external interrupt 0<br>P3.3 #EX1 external interrupt 1<br>P3.4 T0: Timer 0 external input<br>P3.5 T1: Timer 1 external input<br>P3.6 #WR External data memory write strobe<br>P3.7 #RD External data memory read strobe |
| ALE/X32OUT | 30 | 27 | 33 | **Address Latch Enable**:<br>Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted twice every machine cycle, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. Setting SFR SCONF.0 can disable ALE. With this bits set, ALE will be active only during a MOVX instruction.<br>X32OUT: The 32.768KHz crystal output for RTC function. |
| #PSEN/X32IN | 29 | 26 | 32 | **Program Store Enable**:<br>The read strobe to external program memory. When executing code from the external program memory, #PSEN is activated twice each machine cycle, except that two #PSEN activations are skipped during each access to external data memory. #PSEN is not activated during fetches from internal program memory.<br>X32IN: The 32.768KHz crystal input for RTC function. |
| #EA | 31 | 29 | 35 | **External Access Enable:**<br>#EA must be externally held low to enable the device to fetch code from external program memory locations. If #EA is held high, the device executes from internal program memory. |
| X1 | 19 | 15 | 21 | **Crystal 1**:<br>Input to the inverting oscillator amplifier and input to the internal clock generator circuits. |
| X2 | 18 | 14 | 20 | **Crystal 2**:<br>Output from the inverting oscillator amplifier. |

## SFR Mapping

The special function register of SM89S16R1 fall into the following categories

- C51 CORE register: ACC, B, DPL, DPH, PSW, SP
- I/O ports: P0,P1, P2, P3, P4
- Timer/Counter register: T2CON, T2MOD, TCON, TMOD, TH0, TH1, TH2, TL0, TL1, TL2, RCAP2L, RCAP2H
- UART I/O register: SBUF, SCON
- Power and system control register: PCON, SCONF
- Interrupt system register: IP, IE, IP1, IE1, IFR
- PWM output register: PWMC0, PWMC1, PWMD0, PWMD1, P1CON
- ADC register: ADCSC, ADCD, P2CON
- RTC register: RTCC, RTCS
- LED Driving Capability Control: LEDP0, LEDP1, LEDP2, LEDP3, LEDP4

Table 1 SFR Map

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $F8 | | | | | | | | | $FF |
| $F0 | B<br>0000 0000 | | | | | | | | $F7 |
| $E8 | | | | | | | | | $EF |
| $E0 | ACC<br>0000 0000 | | | | | | | | $E7 |
| $D8 | **P4**<br>xxxx 1111 | | | | | | | | $DF |
| $D0 | PSW<br>0000 0000 | | | **PWMC0**<br>0000 0000 | **PWMC1**<br>0000 0000 | | | | $D7 |
| $C8 | T2CON<br>0000 0000 | **T2MOD**<br>xxxx xx00 | RCAP2L<br>0000 0000 | RCAP2H<br>0000 0000 | TL2<br>0000 0000 | TH2<br>0000 0000 | | | $CF |
| $C0 | | | | | | | | | $C7 |
| $B8 | IP<br>0000 0000 | **IP1**<br>0000 0000 | | | | | | **SCONF**<br>0000 0000 | $BF |
| $B0 | P3<br>1111 1111 | | | **PWMD0**<br>0000 0000 | **PWMD1**<br>0000 0000 | | | | $B7 |
| $A8 | IE<br>0000 0000 | **IE1**<br>0000 0000 | **IFR**<br>0000 0000 | | | | | | $AF |
| $A0 | P2<br>1111 1111 | **RTCS**<br>0000 0000 | **RTCC**<br>0000 0000 | | | | | | $A7 |
| $98 | SCON<br>0000 0000 | SBUF<br>xxxx xxxx | | **P1CON**<br>0000 0000 | **P2CON**<br>0000 0000 | | | | $9F |
| $90 | P1<br>1111 1111 | | **LEDP0**<br>0000 0000 | **LEDP1**<br>0000 0000 | **LEDP2**<br>0000 0000 | **LEDP3**<br>0000 0000 | **LEDP4**<br>0000 0000 | | $97 |
| $88 | TCON<br>0000 0000 | TMOD<br>0000 0000 | TL0<br>0000 0000 | TL1<br>0000 0000 | TH0<br>0000 0000 | TH1<br>0000 0000 | **ADCSC**<br>0000 0000 | **ADCD**<br>0000 0000 | $8F |
| $80 | P0<br>1111 1111 | SP<br>0000 0111 | DPL<br>0000 0000 | DPH<br>0000 0000 | | | | PCON<br>0000 0000 | $87 |

Table 2 : All SFR list (8051, I/O, Timer, UART, System, Interrupt, RAM Control, PWM, RTC, ADC)

| Symbol | Description | Direct | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | RESET |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 8051 Core | | | | | | | | | | | |
| ACC* | Accumulator | E0 | | | | | | | | | 00H |
| B | B register | F0 | | | | | | | | | 00H |
| SP | Stack Pointer | 81H | | | | | | | | | 07H |
| PSW* | Process Status | D0H | CY | AC | F0 | RS1 | RS0 | OV | | P | 00H |
| DPTR | Data Pointer (2 Bytes) | | | | | | | | | | |
| DPH | Data Pointer High | 82H | | | | | | | | | 00H |
| DPL | Data Pointer Low | 83H | | | | | | | | | 00H |
| I/O PORT | | | | | | | | | | | |
| P0* | Port 0 | 80H | P0.7 | P0.6 | P0.5 | P0.4 | P0.3 | P0.2 | P0.1 | P0.0 | FFH |
| P1* | Port 1 | 90H | P1.7 | P1.6 | P1.5 | P1.4 | P1.3 | P1.2 | P1.1 | P1.0 | FFH |
| P2* | Port 2 | A0H | P2.7 | P2.6 | P2.5 | P2.4 | P2.3 | P2.2 | P2.1 | P2.0 | FFH |
| P3* | Port 3 | B0H | P3.7 | P3.6 | P3.5 | P3.4 | P3.3 | P3.2 | P3.1 | P3.0 | FFH |
| P4* | Port 4 | D8H | | | | | P4.3 | P4.2 | P4.1 | P4.0 | XFH |
| P1CON | P1 Control | 9BH | | | | | PWM1E | PWM0E | - | - | 00H |
| P2CON | P2 Control | 9CH | ADC3E | ADC2E | ADC1E | ADC0E | | | - | - | 00H |
| TIMER / Counter | | | | | | | | | | | |
| TCON* | Timer Control register | 88H | TF1 | TF1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 | 00H |
| THL0 | Timer 0 (2 Bytes) | | | | | | | | | | |
| TH0 | Timer 0 High | 8CH | | | | | | | | | 00H |
| TL0 | Timer 0 Low | 8AH | | | | | | | | | 00H |
| THL1 | Timer 1 (2 Bytes) | | | | | | | | | | |
| TH1 | Timer 1 High | 8DH | | | | | | | | | 00H |
| TL1 | Timer 1 Low | 8BH | | | | | | | | | 00H |
| T2CON* | Timer 2 Control | C8H | TF2 | EXF2 | RCLK | TCLK | EXEN2 | TR2 | CT2 | CPRL2 | 00H |
| T2MOD | Timer 2 Mode | C9H | | | | | | | T2OE | DCEN | X0H |
| RCAP2HL | Reload/Capture (2 bytes) | | | | | | | | | | |
| RCAP2H | RCAP2 High | CBH | | | | | | | | | 00H |
| RCAP2L | RCAP2 Low | CAH | | | | | | | | | 00H |
| THL2 | Time 2 (2 bytes) | | | | | | | | | | |
| TH2 | Timer 2 High | CDH | | | | | | | | | 00H |
| TL2 | Time 2 Low | CCH | | | | | | | | | 00H |
| UART | | | | | | | | | | | |
| SCON* | UART Control | 98H | SM0 | SM1 | SM2 | REN | TB8 | RB8 | TI | RI | 00H |
| SBUF | UART Buffer | 99H | | | | | | | | | XXH |
| A/D Converter | | | | | | | | | | | |
| ADSCR | ADC status & control | 8EH | COM | CON | ADCSS1 | ADCSS0 | CH1 | CH0 | | | 00H |
| ADCD | ADC data register | 8FH | AD.5 | AD.4 | AD.3 | AD.2 | AD.1 | AD.0 | | | 00H |
| Real Timer Clock (RTC) | | | | | | | | | | | |
| RTCS | RTC Status | A1H | RTCen | Stable | Sec.5 | Sec.4 | Sec.3 | Sec.2 | Sec.1 | Sec.0 | 00H |
| RTCC | RTC Control | A2H | Int_sel.1 | Int_sel.0 | Min.5 | Min.4 | Min.3 | Min.2 | Min.1 | Min.0 | 00H |
| PWM output | | | | | | | | | | | |
| PWMC0 | PWM 0 Control | D3H | | | | | | PBS | PFS1 | PFS0 | 00H |
| PWMC1 | PWM 1 Control | D4H | | | | | | PBS | PFS1 | PFS0 | 00H |
| PWMD0 | PWM 0 Data | B3H | PWMD.7 | PWMD.6 | PWMD.5 | PWMD.4 | PWMD.3 | PWMD.2 | PWMD.1 | PWMD.0 | 00H |
| PWMD1 | PWM 1 Data | B4H | PWMD.7 | PWMD.6 | PWMD.5 | PWMD.4 | PWMD.3 | PWMD.2 | PWMD.1 | PWMD.0 | 00H |
| Power and System | | | | | | | | | | | |
| PCON | Power Control register | 87H | SMOD | | | | | | PD | IDLE | 00H |
| SCONF | System Control | BFH | | | | PDWUE | | | OME | ALEI | 00H |
| Interrupt system | | | | | | | | | | | |
| IE* | Interrupt Enable | A8H | EA | | ET2 | ES0 | ET1 | EX1 | ET0 | EX0 | 00H |
| IE1 | Interrupt Enable 1 | A9H | | | | | EADC | ERTC | | | 00H |
| IFR | Interrupt Flag 1 | AAH | | | | | ADCIF | RTCIF | | | 00H |
| IP* | Interrupt Priority | B8H | | | PT2 | PS0 | PT1 | PX1 | PT0 | PX0 | 00H |
| IP1 | Interrupt Priority 1 | B9H | | | | | PADC | PRTC | | | 00H |
| LED Driving Capability Control | | | | | | | | | | | |
| LEDP 0 | LED output in P0 | 92H | | | | | | | | | 00H |
| LEDP 1 | LED output in P1 | 93H | | | | | | | | | 00H |
| LEDP 2 | LED output in P2 | 94H | | | | | | | | | 00H |
| LEDP 3 | LED output in P3 | 95H | | | | | | | | | 00H |
| LEDP 4 | LED output in P4 | 96H | | | | | | | | | 00H |

# Target Spec.

## Absolute Rating

| Symbol | Description | Min. | Typ. | Max. | Unit. | Remarks |
|---|---|---|---|---|---|---|
| TA | Operating temperature | -40 | 25 | 85 | ℃ | Ambient temperature under bias |
| TS | Storage temperature | -55 | 25 | 155 | ℃ | Damage to devices could occur |
| VCC5 | Supply voltage | 4.5 | 5.0 | 5.5 | V | |
| VCC3.3 | Supply voltage | 3.0 | 3.3 | 3.6 | V | |
| Fosc 25 | Oscillator Frequency | | | 25 | MHz | For 3.3V application |
| Fosc 40 | Oscillator Frequency | | | 40 | MHz | For 5.0V application |

## DC Characteristic

VCC = 5V (±10%), VSS=0V TA= -40℃ to 85℃

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| VCC | Supply Voltage | | 4.5 | 5.5 | V |
| ICC | Supply current operating | See notes 1<br>$f_{CLK}$ = 12MHz VCC = 5.5V | | 20 | mA |
| IID | Supply current IDLE Mode | See note 2<br>$f_{CLK}$ = 12MHz VCC = 5.5V | | 6.5 | mA |
| IPD | Supply current Power-Down MODE<br>RTC Disable | See note 3；VCC (= 5.5V) | | 30 | µA |
| | Supply current Power-Down MODE<br>RTC Enable | See note 3；VCC (= 5.5V) | | 80 | µA |
| **INPUT** | | | | | |
| VIL1 | Input LOW voltage, P0, P1, P2, P3, P4, /EA | | -0.5 | 0.8 | V |
| VIL2 | Input LOW voltage, RES, XTAL1 | | 0 | 0.8 | V |
| VIH1 | Input HIGH voltage, P0, P1, P2, P3, P4, /EA | | 2.0 | Vcc+0.5 | V |
| VIH2 | Input HIGH voltage, RES, XTAL1 | | 70%VCC | Vcc+0.5 | V |
| IIL | Input current LOW level Port 1,2,3,4 | VIN = 0.45V | | -75 | µA |
| ITL | Transition current High to Low Port 1,2,3,4 | VIN = 2.0 V | | -650 | µA |
| ILI | Input leakage current ,Port 0 | 0.45V < VIN < VCC-0.3V | | ±10 | µA |
| **OUTPUT** | | | | | |
| VOL1 | Output LOW voltage, Port 0,ALE, /PSEN | IOL = 8mA，VCC=5.0V | | 0.45 | V |
| VOL2 | Output LOW voltage, Port 1, 2, 3, 4 | IOL = 6.5mA，VCC =5.0V | | 0.45 | V |
| VOH1 | Output High voltage Port0 ALE, /PSEN | IOH = -800uA，VCC =5.0V | 2.4 | | V |
| VOH2 | Output High voltage Port 1,2,3,4 | IOH = -60µA，VCC =5.0V | 2.4 | | V |
| RRST | Internal RESET pull-down resistor | | 50 | 300 | kΩ |
| CIO | Pin capacitance | Test freq=1MHz, TA=25℃ | | 10 | pF |

VCC = 3.3V (±10%), VSS=0V , TA= -40℃ to 85℃

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| VCC | Supply Voltage | | 3.0 | 3.6 | V |
| ICC | Supply current operating | See note 1<br>$f_{CLK}$ = 12MHz VCC = 3.6V | | 10 | mA |
| IID | Supply current IDLE Mode | See note 2<br>$f_{CLK}$ = 12MHz VCC = 3.6V | | 5 | mA |
| IPD | Supply current Power-Down MODE<br>RTC Disable | See note 3；VCC (= 3.6V) | | 20 | µA |
| | Supply current Power-Down MODE<br>RTC Enable | See note 3；VCC (= 3.6V) | | 30 | µA |
| **INPUT** | | | | | |

Specifications subject to change without notice contact your sales representatives for the most recent information.

| | | | | | |
|---|---|---|---|---|---|
| VIL1 | Input LOW voltage, P0, P1, P2, P3, P4, /EA | VCC = 3.6V | 0 | 0.2 VCC -0.2 | V |
| VIL2 | Input LOW voltage, RST | VCC = 3.6V | 0 | 0.2 VCC -0.2 | V |
| VIL3 | Input LOW voltage, XTAL1 | VCC = 3.6V | 0 | 0.2 VCC -0.2 | V |
| VIH1 | Input HIGH voltage, P0, P1, P2, P3, P4, /EA | VCC = 3.6V | 0.6 VCC -0.4 | VCC + 0.2 | V |
| VIH2 | Input HIGH voltage, RST | VCC = 3.6V | 0.6 VCC -0.4 | VCC + 0.2 | V |
| VIH3 | Input HIGH voltage, XTAL1 | VCC = 3.6V | 0.8 VCC | VCC + 0.2 | V |
| IIN1 | Input current LOW level Port 1,2,3,4 | VCC = 3.0V ~3.6V, VIN = 0.45V. | -10 | 50 | µA |
| ITL | Transition current High to Low Port 1,2,3,4 | See note 4 VCC = 3.6V, VIN = 2.0 V | -75 | 400 | µA |
| ILI | Input leakage current P0, /EA | VCC = 3.0V ~3.6V, 0.45V<VIN<VCC | -10 | 10 | µA |
| | | **OUTPUT** | | | |
| VOL1 | Output LOW voltage, Port 0,ALE, /PSEN | IOL = 6mA，VCC =3.3V | | 0.4 | V |
| VOL2 | Output Low voltage Port 1,2,3,4 | IOL = 5mA，VCC =3.3V | | 0.4 | V |
| VOH1 | Output High voltage Port0, ALE, /PSEN | IOH =-300uA，VCC =3.3V | 2.4 | | V |
| VOH2 | Output High voltage Port 1,2,3,4 | IOH =-20µA，VCC =3.3V | 2.4 | | V |
| ISK1 | Sink Current Port 1, 2, 3, 4 | VCC = 3.3V, VIN = 0.4 V | | 6 | mA |
| ISK2 | Sink Current Port 0,ALE, /PSEN | VCC = 3.3V, VIN = 0.4 V | | 8 | mA |
| ISR1 | Source Current Port 1, 2, 3, 4 | VCC = 3.3V, VIN = 2.4 V | | -80 | uA |
| ISR2 | Source Current Port 0,ALE, /PSEN | VCC = 3.3V, VIN = 2.4 V | | -8 | mA |
| RRST | Internal RESET pull-down resistor | | 50 | 300 | kΩ |
| CIO | Pin capacitance | Test freq=1MHz, TA=25℃ | | 10 | pF |

**NOTES FOR DC ELECTRICAL CHARACTERISTICS**

1. The operating supply current is measured with all output disconnected; XTAL1 driven with tr = tf = 5ns; VIL = VSS+0.5V; VIH=VCC-0.5V; XTAL2 not connect; /EA=RST=Port0=VDD;
2. The IDLE MODE supply current is measured with all output pins disconnected; XTAL1 driven with tr = tf = 5ns; VIL = VSS+0.5V; VIH=VCC-0.5V; XTAL2 not connect; /EA=Port0=VDD;
3. The POWER-DOWN MODE supply current is measured with all output pins disconnected; VIL = VSS+0.5V; VIH=VCC-0.5V; XTAL2 not connect; /EA= Port0=VDD;
4. Port 1, 2, 3, and 4 sources a transition current when they are being externally driven from HIGH to LOW. The transition current reaches its maximum value when VIN is approximately 2V.
5. Capacities loading on port 0 and 2 may cause spurious noise to be superimposed on VOL of ALE and port 1, 3, and 4. The noise is due to external bus capacitance discharging into port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt trigger STROBE input.

# AC Characteristic

VCC=3.3V±10%, VSS=0V, tclk min = 1/ fmax(maximum operating frequency)
TA= -40℃ to +85℃
$C_L$=100pF for Port0, ALE and /PSEN; $C_L$=80pF for all other outputs unless otherwise specified.

| Symbol | FIGURE | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| **External Clock drive into XTAL1** | | | | | |
| tCLK | 4 | Xtal1 Period | 40(1) | - | ns |
| tCLKH | 4 | Xtal1 HIGH time | 20 | - | ns |
| tCLKL | 4 | Xtal1 LOW time | 20 | - | ns |
| tCLKR | 4 | XTAL1 rise time | - | 10 | ns |
| tLLIV | 4 | XTAL1 fall time | - | 10 | ns |
| tCYC | 4 | Controller cycle time = tCLK / 4 | 3.33 | - | Ns |

**NOTES:**
1. Operating at 25MHz.

| Symbol | FIGURE | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| **Program Memory** | | | | | |
| 1/tCLK | 7 | System clock frequency | 3.0 | 25 | MHz |
| tLHLL | 7 | ALE pulse width | 2tCLK-40 | | ns |
| tAVLL | 7 | Address valid to ALE low | tCLK-40 | | ns |
| tLLAX | 7 | Address hold after ALE low | tCLK-30 | | ns |
| tLLIV | 7 | ALE LOW to valid instruction in | | 4tCLK-100 | ns |
| tLLPL | 7 | ALE LOW to /PSEN LOW | tCLK-30 | | ns |
| tPLPH | 7 | /PSEN pulse width | 3tCLK-45 | | ns |
| tPLIV | 7 | /PSEN LOW to valid instruction in | | 3tCLK-105 | ns |
| tPXIX | 7 | Input instruction hold after /PSEN | 0 | | ns |
| tPXIZ | 7 | Input instruction float after /PSEN | | tCLK -25 | ns |
| tAVIV | 7 | Address to valid instruction in | | 5tCLK-105 | ns |
| tPLAZ | 7 | /PSEN low to address float | | 10 | ns |
| **Data Memory** | | | | | |
| tAVLL | 8,9 | Address valid to ALE LOW | tCLK-40 | | ns |
| tLLAX | 8,9 | Address hold after ALE LOW | tCLK-35 | | ns |
| tRLRH | 8 | /RD pulse width | 6tCLK-100 | | ns |
| tWLWH | 9 | /WR pulse width | 6tCLK-100 | | ns |
| tRLDV | 8 | /RD LOW to valid data in | | 5tCLK-165 | ns |
| tRHDX | 8 | Data hold after /RD | 0 | | ns |
| tRHDZ | 8 | Data float after /RD | | 2tCLK-70 | ns |
| tLLDV | 8 | ALE LOW to valid data in | | 8tCLK-150 | ns |
| tAVDV | 8 | Address to valid data in | | 9tCLK-165 | ns |
| tLLWL | 8,9 | ALE LOW to /RD or /WR LOW | 3tCLK-50 | 3tCLK+50 | ns |
| tAVWL | 8,9 | Address valid to /WR or /RD LOW | 4tCLK-130 | | ns |
| tQVWX | 9 | Data valid to /WR transition | tCLK-50 | | ns |
| tQVWH | 9 | Data before /WR | 7tCLK-150 | | ns |
| tWHQX | 9 | Data hold after /WR | tCLK-50 | | ns |
| tRLAZ | 8 | /RD LOW to address float | | 0 | ns |
| tWHLH | 8,9 | /RD or /WR HIGH to ALE HIGH | tCLK-40 | tCLK+40 | ns |
| **UART** | | | | | |
| tXLXL | 10 | Serial port clock time | 12tCLK | | ns |
| tQVXH | 10 | Output data setup to clock rising edge | 10tCLK-133 | | ns |
| tXHQX | 10 | Output data hold after clock rising edge | 2tCLK-117 | | ns |
| tXHDX | 10 | Input data hold after clock rising edge | 0 | | ns |
| tXHDV | 10 | Clock rising edge to input data valid | | 10tCLK-133 | ns |

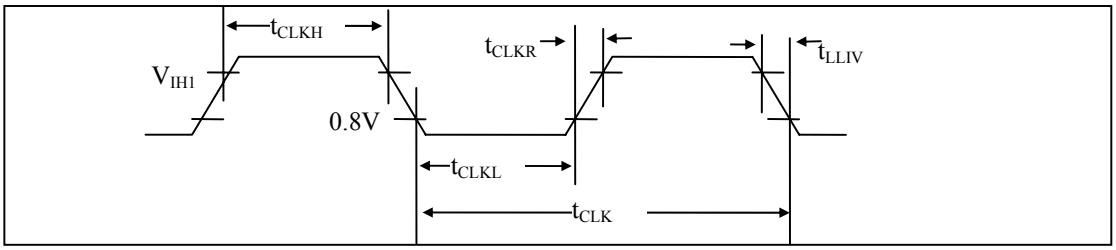



Figure 4 External Clock Drive waveform

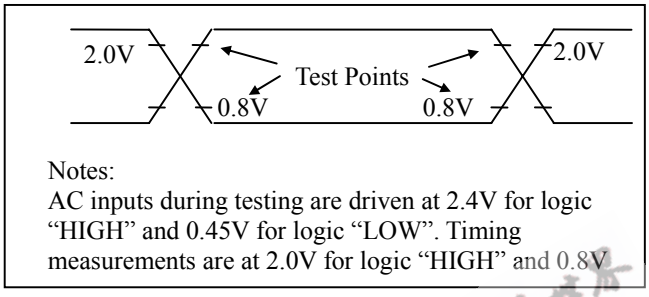



Figure 5 AC Testing Input/Output

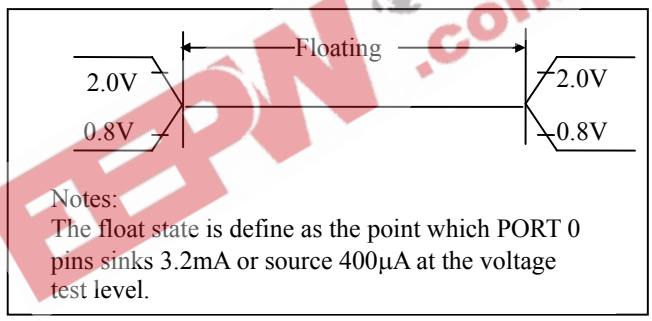



Figure 6 AC Testing, Floating Waveform

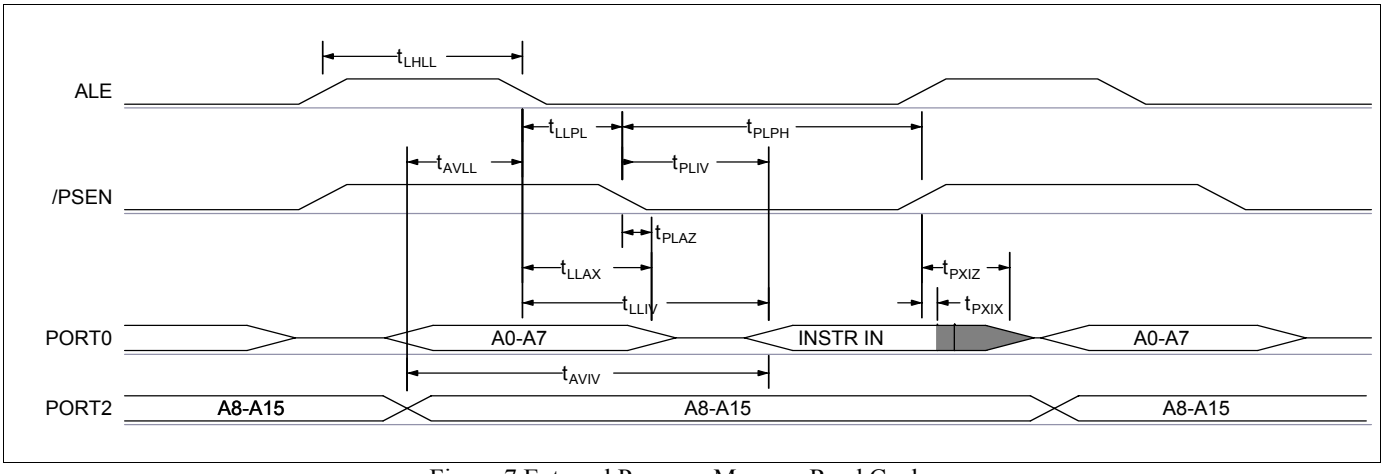



Figure 7 External Program Memory Read Cycle

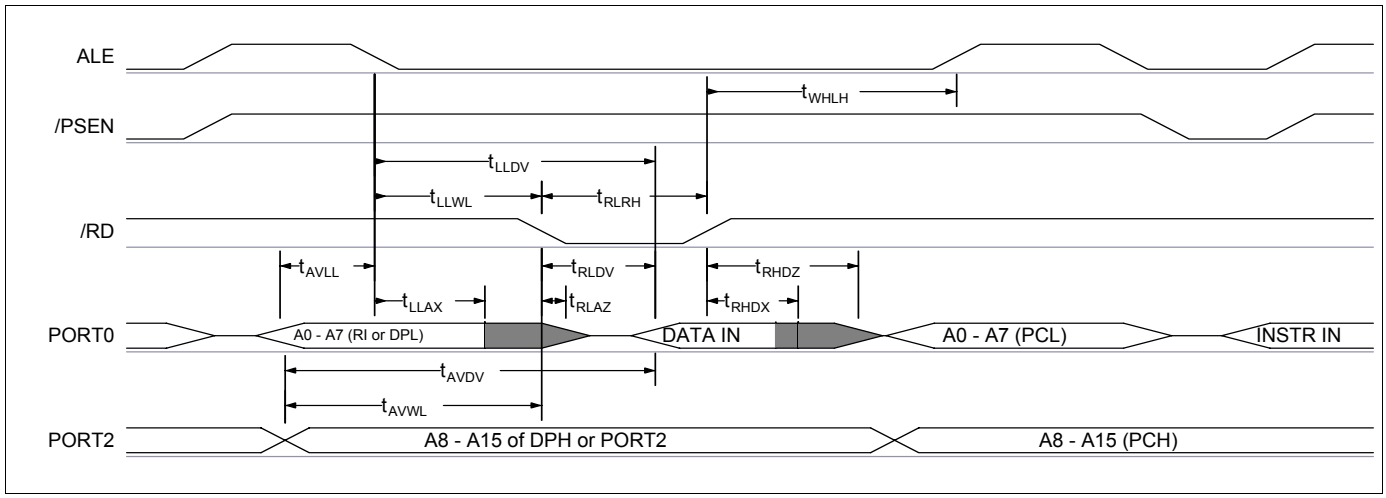



Figure 8 External Data Memory read cycle

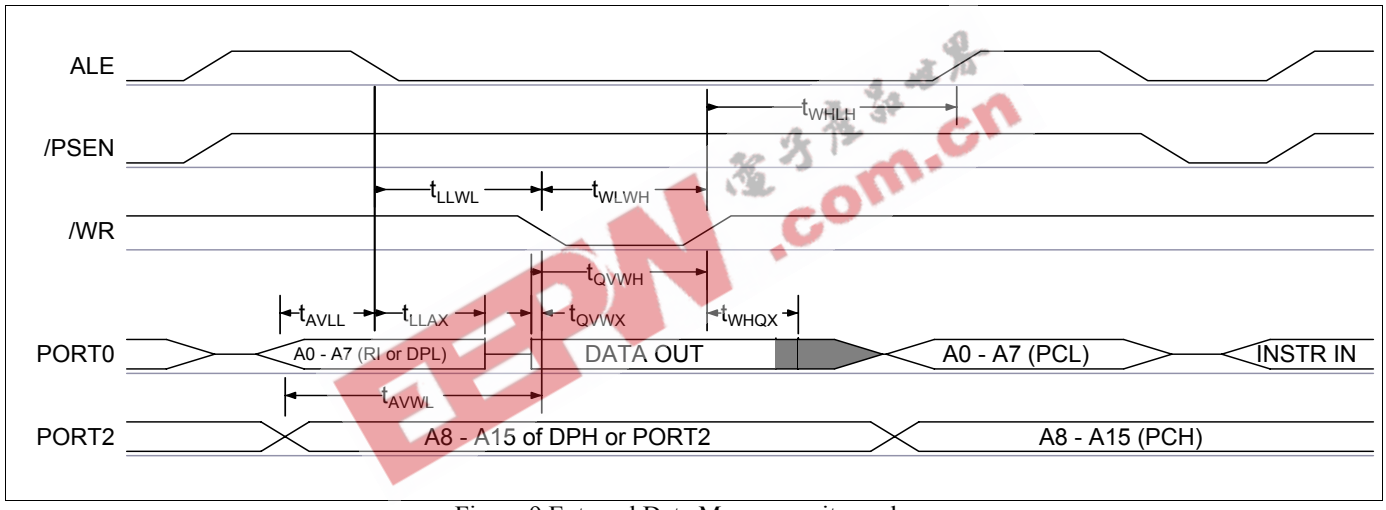



Figure 9 External Data Memory write cycle

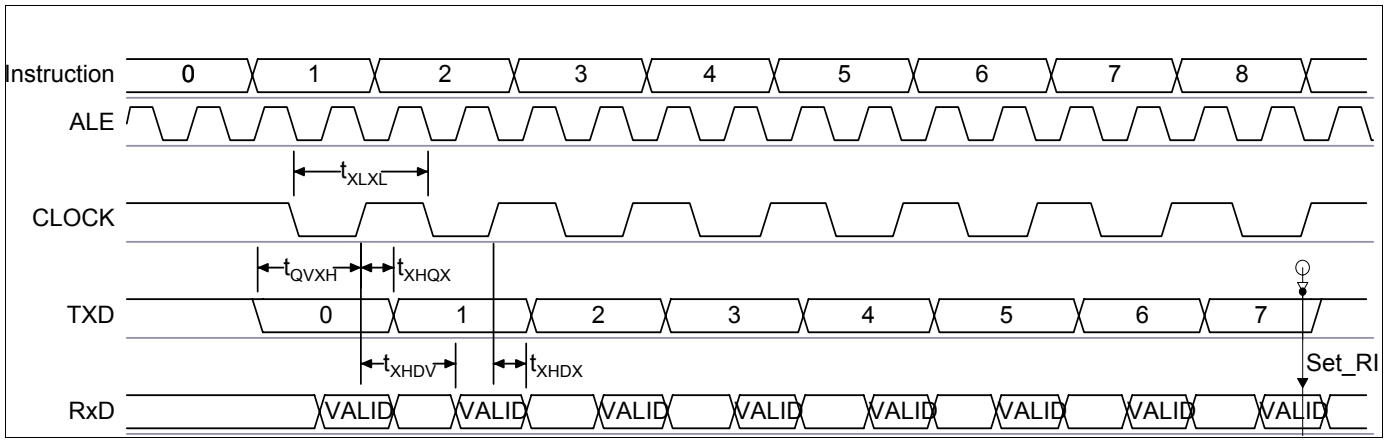



Figure10 UART waveform in Shift Register MODE

Specifications subject to change without notice contact your sales representatives for the most recent information.

## Function Description

The SM89S16R1 is a stand-alone high-performance microcontroller designed for use in many applications, such as LCD monitor, instrumentation, or high-end consumer applications.
In addition to the 80C51 standard functions, the device provides a number of dedicated hardware functions for these applications.
The SM89S16R1 is a control-oriented CPU with on-chip program and data memory. It can be extended with external data memory up to 64K bytes. For system requiring extra capability, the SM89S16R1 can be enhanced by using external memory and peripherals.
The SM89S16R1 has two software selectable modes of saving power consumption：IDLE and POWER-DOWN. The IDLE mode freezes the CPU while allowing the RAM, timer, serial ports and interrupt system to continue functioning. The POWER-DOWN mode save the RAM contents but freezes the oscillator causing all other chip functions to be inoperative. The POWER-DOWN mode can be terminated by H/W reset, or by any one of the two external interrupt or RTCI function.

## CPU

The CPU of SM89S16R1 is compatible to standard 80C51. The structure of this CPU is shown as FIGURE 11. It contains Instruction Register (IR), Instruction Decoder, and Program Counter (PC), Accumulator (ACC), B Register, and control logic. This CPU provides a 8-bits bi-direction bus to communicate with other blocks in the chip. The address and data are transferred through on the same 8-bits bus.

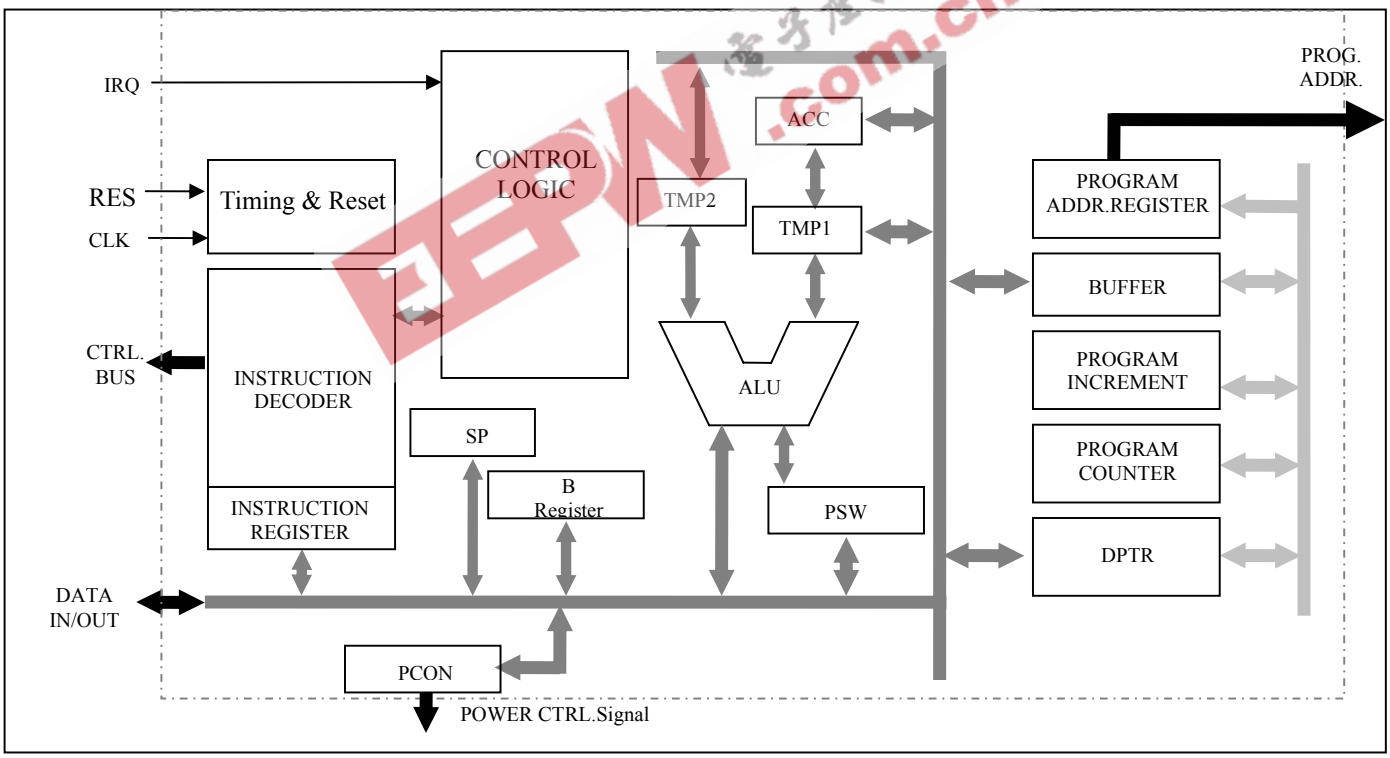



Figure 11 The CPU structure

## CPU Timing

The machine cycle consists of a sequence of 6 states, numbered S1 through S6. Each state time lasts for two oscillator periods. Thus a machine cycle takes 12 oscillator periods. Each state is divided into a PHASE 1 half and a PHASE2 half. FIGURE 12 Shows relationships between oscillator, phase, and S1-S6.

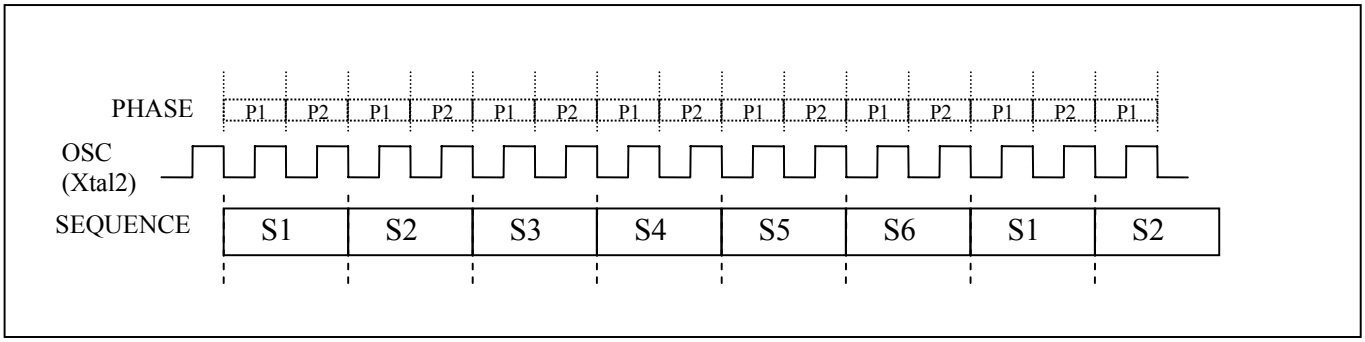
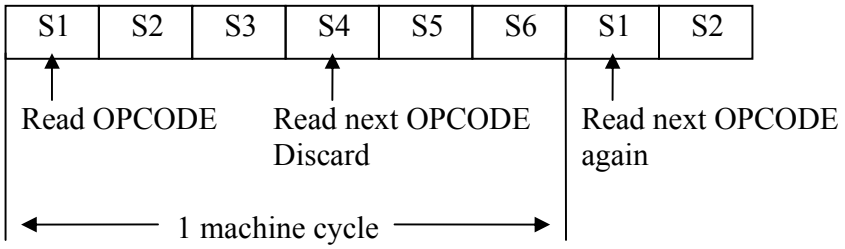



Figure 12 Sequences and Phases

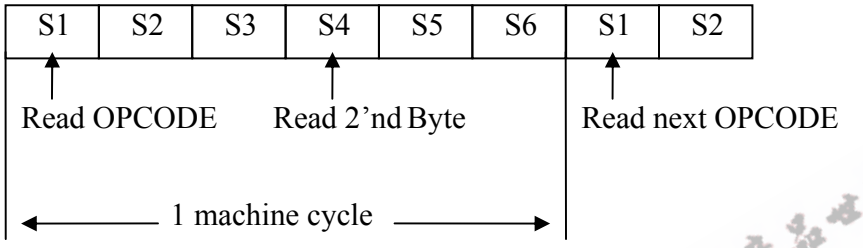
FIGURE 12 shows the fetch / execute sequences in states and phases for various kinds of instructions. Normally the program fetches are generated during each machine cycle, even if the instruction being executed doesn't require it. If the instruction being executed doesn't need more code bytes, the CPU simply ignores the extra fetch, and the PROGRAM COUNTER is incremented accordingly.
Execution of a one-cycle instruction (FIGURE 13A and B) begins during S1 of the machine cycle, when the OPCODE is latched into INSTRUCTION REGISTER. A second fetch occurs during S4 of the same machine cycle. Execution is completed at the end of S6 of this machine cycle.

The MOVX instructions take two machine cycles to execute. No program fetch is generated during the second cycle of a MOVX instruction. This is the only time program fetches are skipped. The fetch/execute sequence for MOVX instructions is shown in FIGURE13 (D)
The fetch/execute sequences are the same whether the PROGRAM MEMORY is internal or external to the chip. Execution times do not depend on whether the PROGRAM MEMORY is internal or external.
FIGURE 14 shows the signals and timing involved in program fetches when the program memory is external. If PROGRAM MEMORY is external, the PROGRAM MEMORY READ STOBE (/PSEN) is normally activated twice per machine cycle, as shown in FIGURE 14(A).
If an access external DATA MEMORY occurs, as shown in FIGURE 14(B), two (/PSEN) are SKIPPED, because the address and data bus are being used for DATA MEMORY access.
Note that a DATA MEMORY bus cycle takes twice as much time as PROGRAM MEMORY bus cycle. FIGURE 14 shows the relative time of the address begin emitted at PORT0 and PORT2, and of ALE and /PSEN. ALE is used to latch the low address byte form PORT0 into the address latch.
When CPU is executing from internal PROGRAM MEMORY, /PSEN is not activated, and program address is not emitted. However, ALE continues to be activated twice per machine cycle and so is available as clock output signal. Note, however, that ALE is skipped during the execution of the MOVX instruction.

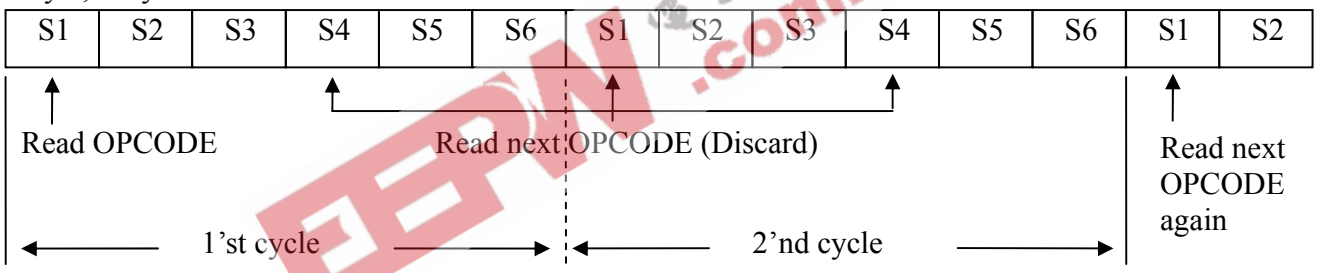
A.) 1 byte, 1 Cycle Instruction




B.) 2 byte, 1 Cycle Instruction




C.) 1 byte, 2 Cycle Instruction




D.) MOVX: 1 byte, 2 Cycle Instruction ACCESS external memory

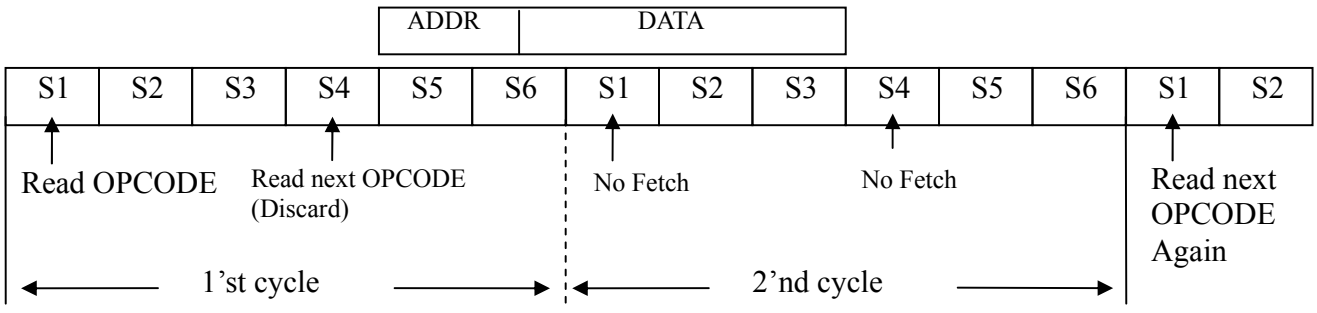



Figure 13 Timing of various instructions

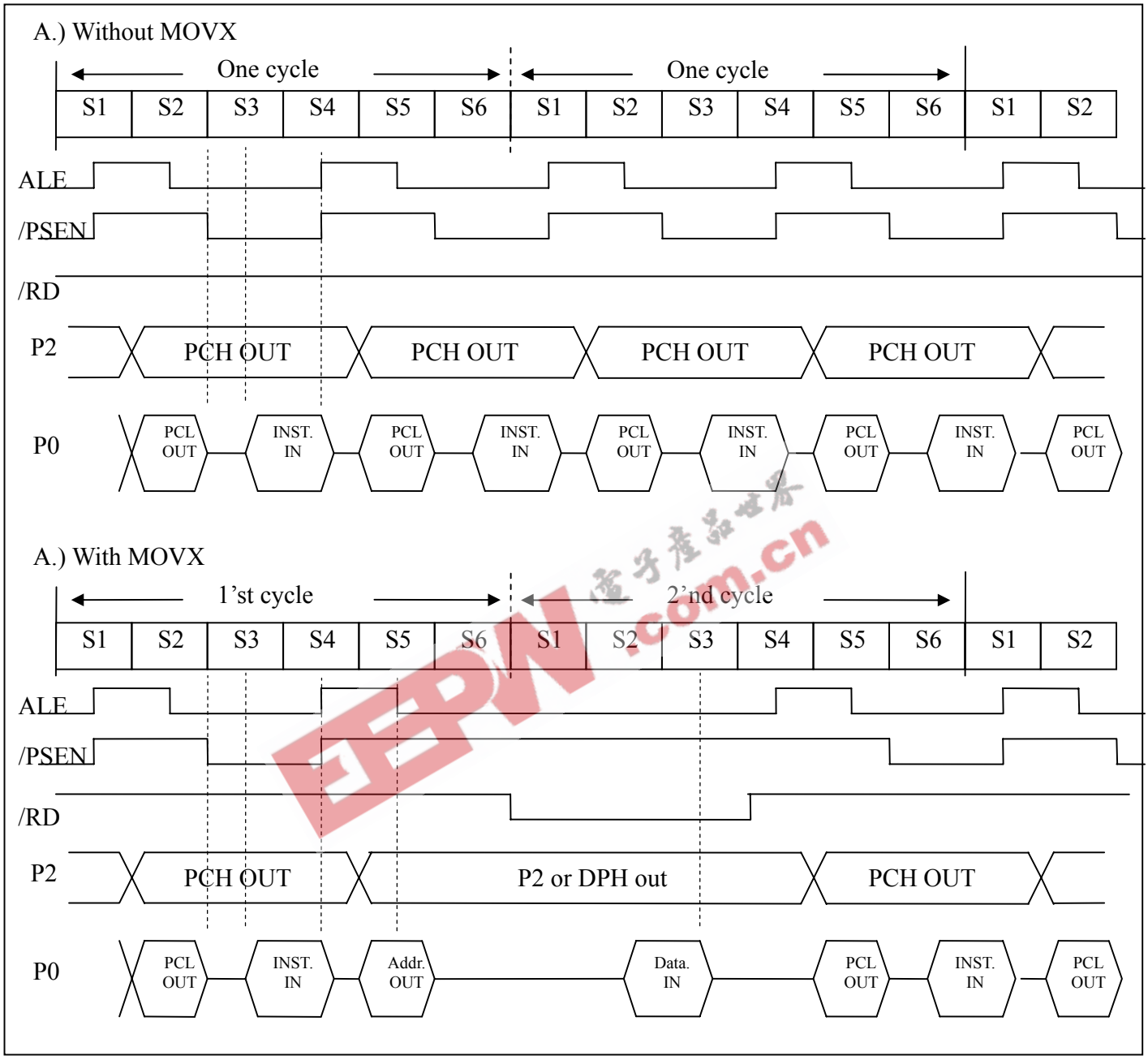



Figure 14: Bus cycle in external program memory mode

## Instruction Set

The SM89S16R1 uses the powerful instruction set of 80C51. It consists of 49 single-byte, 42 two-byte, and 15 three-byte instructions. Among them 63 instruction are executed in 1 machine-cycle, 46 instructions in 2 machine-cycles, and the multiply, 2 instructions in 4 machine-cycles.
A summary of the instruction set is given in Table 3.

# Addressing Mode

Notes on instruction set and address modes:

| | | |
|---|---|---|
| Rn | | Register R7-R0 of the currently selected register bank. |
| direct | | 8-bits internal data location's address. This could be internal DATA RAM location (0-127) or a SFR [i.e., I/O port, control register, status register, etc. (128-255)] |
| @Ri | | 8-bits RAM location addressed indirectly through register R1 or R0 of the actual register bank |
| #data | | 8-bits constant included in the instruction |
| #data16 | | 16-bits constant included in the instruction |
| addr11 | | 11-bits destination address. Used by ACALL and AJMP. The branch can be anywhere within the same 2 Kbytes page of program memory as the first byte of the following instruction. |
| rel | | Signed (2's complement) 8-bits offset byte. Used by SJMP and all conditional jumps. Range is -128 to +127 bytes relative to first byte of the following instruction. |
| bit | | Direct addressed bit in internal data RAM or SFR |

Table 3: A Summary of the instruction set

| Mnemonic | | OPERATION | BYTE | CYCLE |
|---|---|---|---|---|
| **Arithmetic Instructions** | | | | |
| ADD | A,Rn | A = A + Rn | 1 | 1 |
| ADD | A,direct | A = A + direct | 2 | 1 |
| ADD | A,@Ri | A = A + <@Ri> | 1 | 1 |
| ADD | A,#data | A = A + #data | 2 | 1 |
| ADDC | A,Rn | A = A + Rn + C | 1 | 1 |
| ADDC | A,direct | A = A + direct + C | 2 | 1 |
| ADDC | A,@Ri | A = A + @Ri + C | 1 | 1 |
| ADDC | A,#data | A = A + #data + C | 2 | 1 |
| SUBB | A,Rn | A = A − Rn − C | 1 | 1 |
| SUBB | A,direct | A = A − direct − C | 2 | 1 |
| SUBB | A,@Ri | A = A − <@Ri> − C | 1 | 1 |
| SUBB | A,#data | A = A −#data − C | 2 | 1 |
| INC | A | A = A + 1 | 1 | 1 |
| INC | Rn | Rn = Rn + 1 | 1 | 1 |
| INC | direct | direct = direct + 1 | 2 | 1 |
| INC | @Ri | <@Ri> = <@Ri> + 1 | 1 | 1 |
| DEC | A | A = A − 1 | 1 | 1 |
| DEC | Rn | Rn = Rn − 1 | 1 | 1 |
| DEC | direct | direct = direct − 1 | 2 | 1 |
| DEC | @Ri | <@Ri> = <@Ri> − 1 | 1 | 1 |
| INC | DPTR | DPTR = DPTR − 1 | 1 | 2 |
| MUL | AB | B:A = A × B | 1 | 4 |
| DIV | AB | A = INT (A/B)<br>B = MOD (A/B) | 1 | 4 |
| DA | A | Decimal adjust ACC | 1 | 1 |
| **Logical Instructions** | | | | |
| ANL | A,Rn | A .AND. Rn | 1 | 1 |
| ANL | A,direct | A .AND. direct | 2 | 1 |
| ANL | A,@Ri | A .AND. <@Ri> | 1 | 1 |
| ANL | A,#data | A .AND. #data | 2 | 1 |
| ANL | direct,A | direct .AND. A | 2 | 1 |
| ANL | direct,#data | direct .AND. #data | 3 | 2 |
| ORL | A,Rn | A .OR. Rn | 1 | 1 |
| ORL | A,direct | A .OR. direct | 2 | 1 |
| ORL | A,@Ri | A .OR. <@Ri> | 1 | 1 |
| ORL | A,#data | A .OR. #data | 2 | 1 |
| ORL | direct,A | direct .OR. A | 2 | 1 |
| ORL | direct,#data | direct .OR. #data | 3 | 2 |
| XRL | A,Rn | A .XOR. Rn | 1 | 1 |
| XRL | A,direct | A .XOR. direct | 2 | 1 |
| XRL | A,@Ri | A .XOR. <@Ri> | 1 | 1 |
| XRL | A,#data | A .XOR. #data | 2 | 1 |
| XRL | direct,A | direct .XOR. A | 2 | 1 |
| XRL | direct,#data | direct .XOR. #data | 3 | 2 |

| | | | | |
|---|---|---|---|---|
| CLR | A | A = 0 | 1 | 1 |
| CPL | A | A = /A | 1 | 1 |
| RL | A | Rotate ACC Left 1 bit | 1 | 1 |
| RLC | A | Rotate Left through Carry | 1 | 1 |
| RR | A | Rotate ACC Right 1 bit | 1 | 1 |
| RRC | A | Rotate Right through Carry | 1 | 1 |
| SWAP | A | Swap Nibbles in A | 1 | 1 |
| **Data Transfers Instructions** | | | | |
| MOV | A,Rn | A = Rn | 1 | 1 |
| MOV | A,direct | A = direct | 2 | 1 |
| MOV | A,@Ri | A = <@Ri> | 1 | 1 |
| MOV | A,#data | A = #data | 2 | 1 |
| MOV | Rn,A | Rn = A | 1 | 1 |
| MOV | Rn,direct | Rn = direct | 2 | 2 |
| MOV | Rn,#data | Rn = #data | 2 | 1 |
| MOV | direct,A | direct = A | 2 | 1 |
| MOV | direct,Rn | direct = Rn | 2 | 2 |
| MOV | direct,direct | direct = direct | 3 | 2 |
| MOV | direct,@Ri | direct = <@Ri> | 2 | 2 |
| MOV | direct,#data | direct = #data | 2 | 1 |
| MOV | @Ri,A | <@Ri> = A | 1 | 1 |
| MOV | @Ri,direct | <@Ri> = direct | 2 | 2 |
| MOV | @Ri,#data | <@Ri> = #data | 2 | 1 |
| MOV | DPTR,#data16 | DPTR = #data16 | 3 | 2 |
| MOVC | A,@A+DPTR | A = code memory[A+DPTR] | 1 | 2 |
| MOVC | A,@A+PC | A = code memory[A+PC] | 1 | 2 |
| MOVX | A,@Ri | A = external memory[Ri] (8-bits address) | 1 | 2 |
| MOVX | A,@DPTR | A = external memory[DPTR] (16-bits address) | 1 | 2 |
| MOVX | @Ri,A | external memory[Ri] = A (8-bits address) | 1 | 2 |
| MOVX | @DPTR,A | external memory[DPTR] = A (16-bits address) | 1 | 2 |
| PUSH | direct | INC SP: MOV "@'SP', < direct > | 2 | 2 |
| POP | direct | MOV < direct >, "@SP": DEC SP | 2 | 2 |
| XCH | A,Rn | ACC and < Rn > exchange data | 1 | 1 |
| XCH | A,direct | ACC and < direct > exchange data | 2 | 1 |
| XCH | A,@Ri | ACC and < Ri > exchange data | 1 | 1 |
| XCHD | A,@Ri | ACC and @Ri exchange low nibbles | 1 | 1 |
| **Boolean Instructions** | | | | |
| CLR | C | C = 0 | 1 | 1 |
| CLR | bit | bit = 0 | 2 | 1 |
| SETB | C | C = 1 | 1 | 1 |
| SETB | bit | bit = 1 | 2 | 1 |
| CPL | C | C = /C | 1 | 1 |
| CPL | bit | bit = /bit | 2 | 1 |
| ANL | C,bit | C = C .AND. bit | 2 | 2 |
| ANL | C,/bit | C = C .AND. /bit | 2 | 2 |
| ORL | C,bit | C = C .OR. bit | 2 | 2 |
| ORL | C,/bit | C = C .OR. /bit | 2 | 2 |
| MOV | C,bit | C = bit | 2 | 1 |
| MOV | bit,C | bit = C | 2 | 2 |
| JC | rel | Jump if C= 1 | 2 | 2 |
| JNC | rel | Jump if C= 0 | 2 | 2 |
| JB | bit,rel | Jump if bit = 1 | 3 | 2 |
| JNB | bit,rel | Jump if bit = 0 | 3 | 2 |
| JBC | bit,rel | Jump if C = 1 | 3 | 2 |
| **Jump Instructions** | | | | |
| ACALL | addr11 | Call Subroutine only at 2k bytes Address | 2 | 2 |
| LCALL | addr16 | Call Subroutine in max 64K bytes Address | 3 | 2 |
| RET | | Return from subroutine | 1 | 2 |
| RETI | | Return from interrupt | 1 | 2 |
| AJMP | addr11 | Jump only at 2k bytes Address | 2 | 2 |
| LJMP | addr16 | Jump to max 64K bytes Address | 3 | 2 |
| SJMP | rel | Jump on at 256 bytes | 2 | 2 |
| JMP | @A+DPTR | Jump to A+ DPTR | 1 | 2 |
| JZ | rel | Jump if A = 0 | 2 | 2 |
| JNZ | rel | Jump if A ≠ 0 | 2 | 2 |
| CJNE | A, direct,rel | Jump if A ≠ < direct > | 3 | 2 |

| | | | | |
|---|---|---|---|---|
| CJNZ | A, #data,rel | Jump if A ≠ < #data > | 3 | 2 |
| CJNZ | Rn, #data,rel | Jump if Rn ≠ < #data > | 3 | 2 |
| CJNZ | @Ri, #data,rel | Jump if @Ri ≠ < #data > | 3 | 2 |
| DJNZ | Rn,rel | Decrement and jump if Rn not zero | 2 | 2 |
| DJNZ | direct,rel | Decrement and jump if direct not zero | 3 | 2 |
| NOP | | No Operation | 1 | 1 |

## Memory organization

The central processing unit (CPU) manipulates operands in three memory spaces; there are 1024 bytes internal data memory (consisting of 256 bytes standard RAM and 768 bytes AUX-RAM) and 64K bytes internal/external program memory (see FIGURE 15)

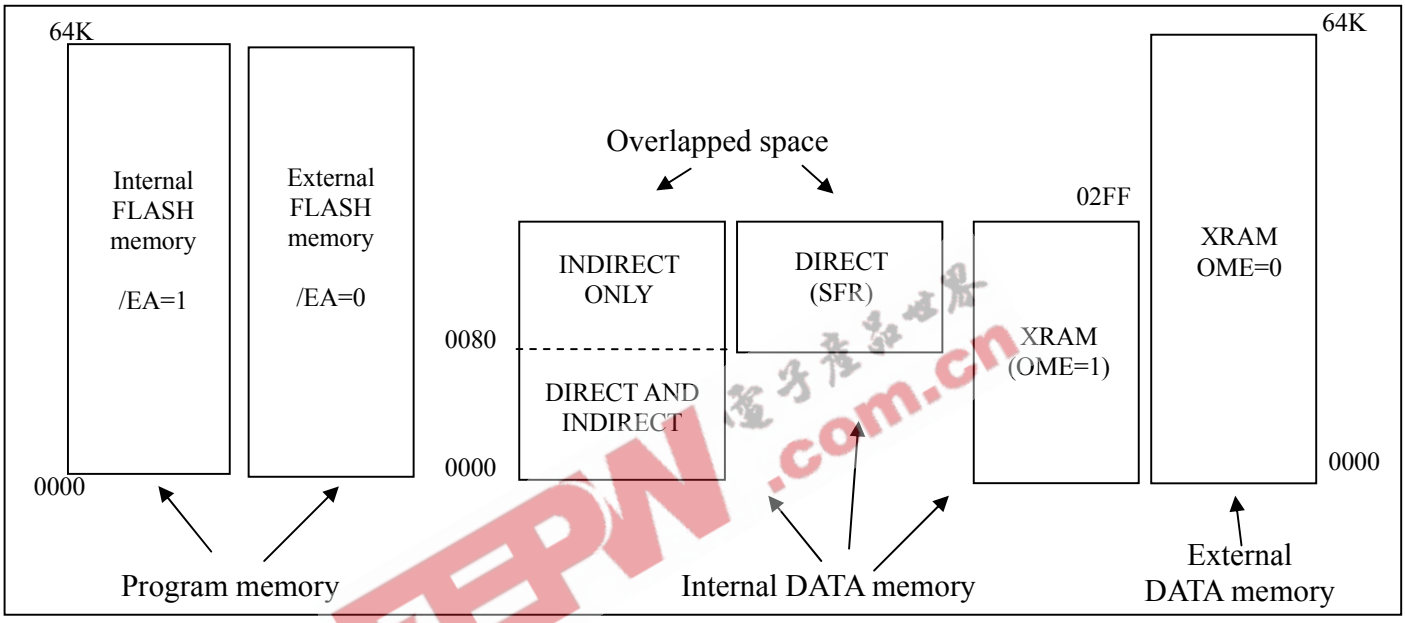



Figure 15 Memory organization of SM89S16R1

## Program memory

The program memory of SM89S16R1 consists of 64K bytes FLASH memory on chip. If during RESET, the /EA pin was held high, the SM89S16R1 does not execute out of the internal program memory. If the /EA pin was held low during RESET the SM89S16R1 fetch all instructions from the external program memory.
External writer can program it. The feature of FLASH memory is shown as following：

- **READ:** byte-wise
- **WRITE:** byte-wise within 30us (previously erased by a chip erase).
- **ERASE:**

  Page Erase (512 bytes) within 10 ms

  Full Erase (64K bytes) within 2 sec.

  Erased bytes contain FFH
- **Endurance :** 10K erase and write cycles each byte at TA=25℃
- **Retention :** 10 years

## Internal Data memory

The data memory of SM89S16R1 consists of 1024 bytes internal data memory (256 bytes standard RAM and 768 bytes AUX-RAM). The AUX-RAM is enable by SCONF.1 ($BF.1), and read/write by MOVX

## Analog to Digital Converter (ADC)

The ADC block diagram was shown as below:
Those are only 4 pins mirror to Port 2[7:4] at Vin<3:0>. The digital output DATA [11:4] were put into ADCD ($8FH).
And the ADC interrupt vector is 4BH.
The ADC SFR shown as below:

**ADSCR ($8EH)**

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|
| Com | Con | ADCSS1 | ADCSS0 | CH1 | CH0 | | |

COM: Read only. When conversion complete, it will be set.
CON: when set, the ADC will conversion continuous, else it will conversion only once.
ADCSS [1:0]: ADC clock select. (ADC_CLK range 500 KHz~2.5 MHz).If over frequency of ADC_CLK, the conversion data may be unstable.

| ADCSS1 | ADCSS0 | ADC_CLK |
|---|---|---|
| 0 | 0 | FOSC/8 |
| 0 | 1 | FOSC/16 |
| 1 | 0 | FOSC/32 |
| 1 | 1 | FOSC/64 |

CH [1:0]: ADC channel select.

| CH1 | CH0 | Input select |
|---|---|---|
| 0 | 0 | CH0 |
| 0 | 1 | CH1 |
| 1 | 0 | CH2 |
| 1 | 1 | CH3 |

**ADCD ($8FH)**

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|
| AD.5 | AD.4 | AD.3 | AD.2 | AD.1 | AD.0 | | |

*Read Only.

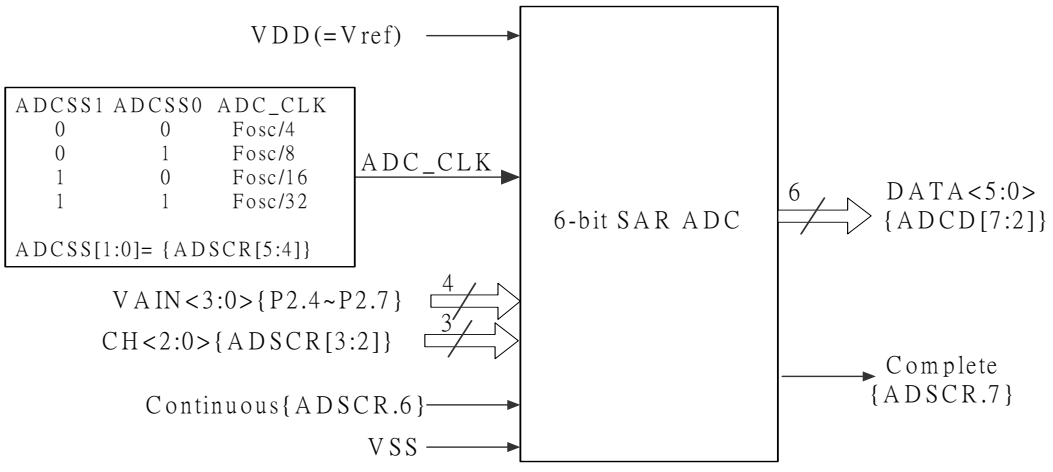



Figure 16 ADC Block Diagram

## Pulse Width Modulation (PWM)

The PWM output pins are P1.4 and P1.5.
The PWM clock is {Fosc/ (2xDivider)}, the PWM output frequency is {(PWM clock)/32} at 5 bits resolution and {(PWM clock)/256} at 8 bits resolution.
The PWM SFR show as below:

### PWMC ($D3H and $D4H)

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|
| | | | | | PBS | PFS1 | PFS0 |

PBS: when set, the PWM is 5 bits resolution.
PFS [1:0]: The PWM clock divider select.

| PFS1 | PFS0 | PWM clock divider select |
|---|---|---|
| 0 | 0 | 2 |
| 0 | 1 | 4 |
| 1 | 0 | 8 |
| 1 | 1 | 16 |

### PWMD ($B3H and $B4H)

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|
| PWMD.7 | PWMD.6 | PWMD.5 | PWMD.4 | PWMD.3 | PWMD.2 | PWMD.1 | PWMD.0 |

## Real Time Clock (RTC)

The on-chip RTC keeps time of second and minute functions. Its time base is a 32.768 KHz crystal between pins X32OUT (alternate function of ALE) and X32IN (alternate function of PSEN). The RTC maintains time to a second. It also allows a user to read (and write) seconds and minute.
The RTC function used SFR descriptor as below:

### RTCS ($A1H)

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|
| RTCen | Stable | SEC.5 | SEC.4 | SEC.3 | SEC.2 | SEC.1 | SEC.0 |

RTCen: When set to '1', enable the enable RTC function. When this bit set, the ALE and PSEN pins output will disable, and the ALE and PSEN pins will use for RTC function as X32OUT and X32IN.
Stable: Read only. The Stable bit will set to 1 when the RTC module stable. Please wait 2 seconds before used the RTC function.
SEC [5:0]: show the current second counter at RTC function. The range is from 00H to 3BH.

### RTCC ($A2H)

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|
| INT_SEL1 | INT_SEL0 | MIN.5 | MIN.4 | MIN.3 | MIN.2 | MIN.1 | MIN.0 |

INT_SEL [1:0]: the interrupt distribution selection bit, the interrupt vector is 43H.
00: the interrupt is set as 0.5 second
01: the interrupt is set as 1 second
10: the interrupt is set as 30 second
11: the interrupt is set as 60 second
MIN [5:0]: show the current minute counter at RTC function. The range is from 00H to 3BH.

## Starting and stopping the RTC:

### RTCS ($A1H)

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|
| RTCen | Stable | SEC.5 | SEC.4 | SEC.3 | SEC.2 | SEC.1 | SEC.0 |

The RTC Function is enable by set the RTCS.7 (RTCen=1), then the ALE and /PSEN pins will switch to X32OUT and X32IN that for RTC function used, the ALE and PSEN signal output will disable; the crystal frequency is 32.768 KHz. See figure 17.

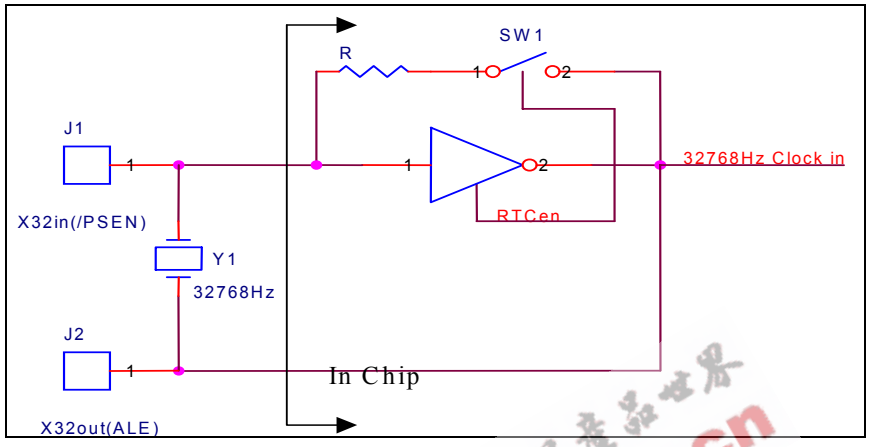



Figure 17 The RTC Crystal connect diagram

The stable bit (RTCS.6) will set to 1 when the RTC module stable. The design is about 31.25 ms; suggest waiting 2 second to use the RTC function. This bit will clear when RTCen bit set again.
The SEC [5:0] will show the second counter (range from 00H to 3BH), and the MIN [5:0] will show the minute counter (range from 00H to 3BH) of RTC function. This two register will clear when RTCen bit set.

## Interrupt:

### IE1 ($A9H)

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|
| | | | | EADC | ERTC | | |

ERTC: When set to '1', enable the RTC interrupt. If you want to use the RTC interrupt function, must enable the EA bit in IE.7 and enable the ERTC bit in IE1.2.
EADC: When set to '1', enable the ADC interrupt. If you want to use the ADC interrupt function, must enable the EA bit in IE.7 and enable the EADC bit in IE1.3

### RTCC ($A2H)

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|
| INT_SEL1 | INT_SEL0 | MIN.5 | MIN.4 | MIN.3 | MIN.2 | MIN.1 | MIN.0 |

Then select the interrupt distribution in INT_SEL [1:0] in RTCC [7:6].
The RTC can select each of 4 interrupt sources: 0.5 second, 1 second, 0.5 minute, and 1 minute. The interrupt vector is 43H, it can wake-up CPU from POWER-DOWN mode.

### IFR ($AAH)

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|
| | | | | ADCIF | RTCIF | | |

ADCIF: When interrupt occupy the ADC interrupt flag (IFR.3) will set, and the CPU will execute the interrupt subroutine at the interrupt vector 4BH. The ADC Interrupt Flag must clear by software.

RTCIF: When interrupt occupy the RTC interrupt flag (IFR.2) will set, and the CPU will execute the interrupt subroutine at the interrupt vector 43H. The RTC Interrupt Flag must clear by software.

**IP1 ($B9H)**

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|
| | | | | PADC | PRTC | | |

The interrupt priority can be set at IP1.2 or IP1.3.
PADC: When set to '1', enable the ADC interrupt priority.
PRTC: When set to '1', enable the RTC interrupt priority.

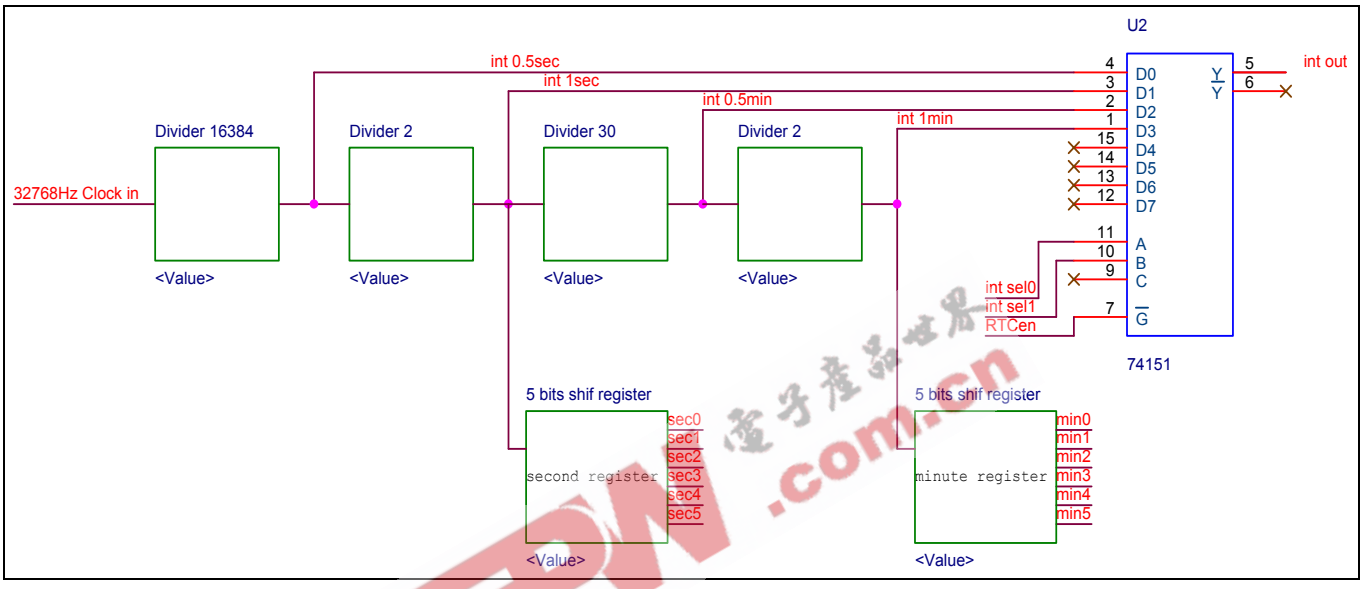



Figure 18 The RTC Block Diagram

## LED Driving Capability Control

This function is set the sink current more then 10 mA for each pin, 26 mA for whole Port 0, 15 mA for whole Port 1 or whole Port2 or whole Port3 or whole Port4, and total 71 mA for whole chip.
The SFR show as below:

| Port Name | SFR Address | Iol(max) for total port |
|---|---|---|
| Port0 | $92H | 26 mA |
| Port1 | $93H | 15 mA |
| Port2 | $94H | 15 mA |
| Port3 | $95H | 15 mA |
| Port4 | $96H | 15 mA |

## The Power Down Wake Up (PDWU) function

The device can be put into Power Down mode by writing 1 to bit PCON.1. The instruction that does this will be the last instruction to be executed before the device goes into Power Down mode. In the Power Down mode, all the clocks are stopped and the device comes to a halt. All activity is completely stopped and the power consumption is reduced to the lowest possible value. In this state the ALE and PSEN pins are pulled low. The port pins output the values held by their respective SFRs.

The SM89S16R1 will exit the Power Down mode with a reset or by a RTC (Real Time Clock) interrupt or by an external interrupts pin enabled as level detects.

1. An external reset can be used to exit the Power Down state. The high on RST pin terminates the Power Down mode, and restarts the clock. The program execution will restart from 0000H.
2. An external interrupt pin and RTC interrupt can be used to exit the Power Down state when the external interrupt or RTC interrupt actives and provided the corresponding interrupt is enabled, while the global enable (EA) bit is set and the external input has been set to a level detect mode or RTC interrupt set. If these conditions are met, then the low level on the external pin or RTC interrupt re-starts the oscillator. Then device executes the interrupt service routine for the corresponding external interrupt or RTC interrupt. After the interrupt service routine is completed, the program execution returns to the instruction after the one that put the device into Power Down mode and continues from there.

**PCON ($87H)**

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|
| SMOD | | | | | | PD | IDLE |

SMOD: This bit set to '1' to make the UART baud-rate double.
PD: When set to '1' , the MCU will into Power Down mode
IDLE: When set to '1' , the MCU will into IDLE mode

**SCONF ($BFH)**

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|
| | | | PDWUE | | | OME | ALEI |

PDWUE: When set to '1', enable the PDWU function.
OME: When set to '1', enable the 768 bytes expanded RAM.
ALEI: When set to '1', it will stop ALE clock output for EMI reduce.

**IE ($A8H)**

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|
| EA | | ET2 | ES0 | ET1 | EX1 | ET0 | EX0 |

EA: When set to '1', enable interrupt global.
ET2: When set to '1', enable Timer2 interrupt.
ES0: When set to '1', enable UART interrupt.
ET1: When set to '1', enable Timer1 interrupt.
EX1: When set to '1', enable external interrupt 1.
ET0: When set to '1', enable Timer0 interrupt.
EX0: When set to '1', enable external interrupt 0.

**TCON ($88H)**

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|
| TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 |

TF1: Timer 1 overflow flag.
TR1: Timer 1 run control bit.
TF0: Timer 0 overflow flag.
TR0: Timer 0 run control bit.
IE1: External Interrupt 1 edge flag.
IT1: Interrupt 1 type control bit.
IE0: External Interrupt 0 edge flag.
IT0: Interrupt 0 type control bit.

**IP ($B8H)**

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|
| | | PT2 | PS0 | PT1 | PX1 | PT0 | PX0 |

PT2: Timer2 interrupt priority.
PS0: UART interrupts priority.
PT1: Timer1 interrupt priority.
PX1: external interrupt 1 priority.
PT0: Timer0 interrupt priority.
PX0: external interrupt 0 priority.

## The Priority structure and vector locations of interrupts:

| Source | Flag | Priority level | Vector Address |
|---|---|---|---|
| External interrupt 0 | IE0 | 1(highest) | 03H |
| Timer 0 overflow | TF0 | 2 | 0BH |
| External interrupt 1 | IE1 | 3 | 13H |
| Timer 1 overflow | TF1 | 4 | 1BH |
| UART 0 interrupt | RI+TI | 5 | 23H |
| Timer 2 overflow | TF2+EXF2 | 6 | 2BH |
| RTC interrupt | RTCIF | 7 | 43H |
| ADC interrupt | ADCIF | 8 | 4BH |

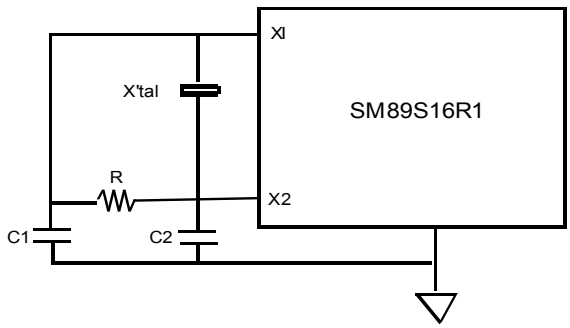
**T2MOD ($C9H)**

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|
| | | | | | | T2OE | DCEN |

T2CR: Timer 2 Capture Reset. In the Timer2 Capture Mode this bit enables/disables hardware automatically reset Timer2 while the value in TL2 and TH2 have been transferred into the capture register.
T2OE: Timer2 clock Output Enable bit. If set to 1, the Timer2 clock will output to P1.0.
DCEN: Down Count Enable. When set this bit then allows Timer2 to be configured as an up/down counter.

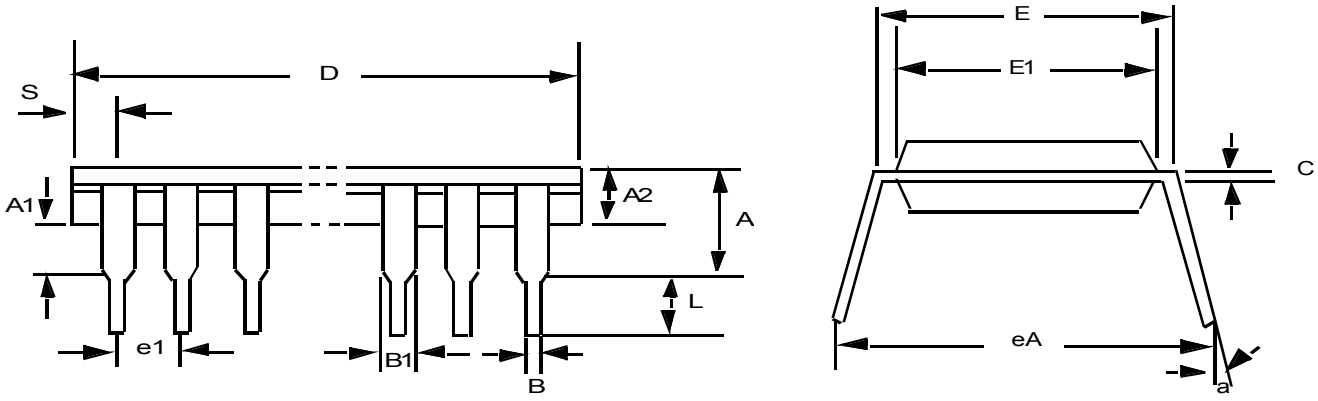
**Application Reference**

| Valid for SM89S16R1 | | | | |
|---|---|---|---|---|
| X'tal | 3MHz | 6MHz | 9MHz | 12MHz |
| C1 | 30 pF | 30 pF | 30 pF | 22 pF |
| C2 | 30 pF | 30 pF | 30 pF | 22 pF |
| R | open | open | open | open |
| | | | | |
| X'tal | 16MHz | 25MHz | 33MHz | 40MHz |
| C1 | 30 pF | 15 pF | 5 pF | 2 pF |
| C2 | 30 pF | 15 pF | 5 pF | 2 pF |
| R | open | open | 6.8K | 4.7K |




**Note:**
Oscillation circuit may differs with different crystal or ceramic resonator in higher oscillation frequency which was due to each crystal or ceramic resonator has its own characteristics.
User should check with the crystal or ceramic resonator manufacturer for appropriate value of external components.

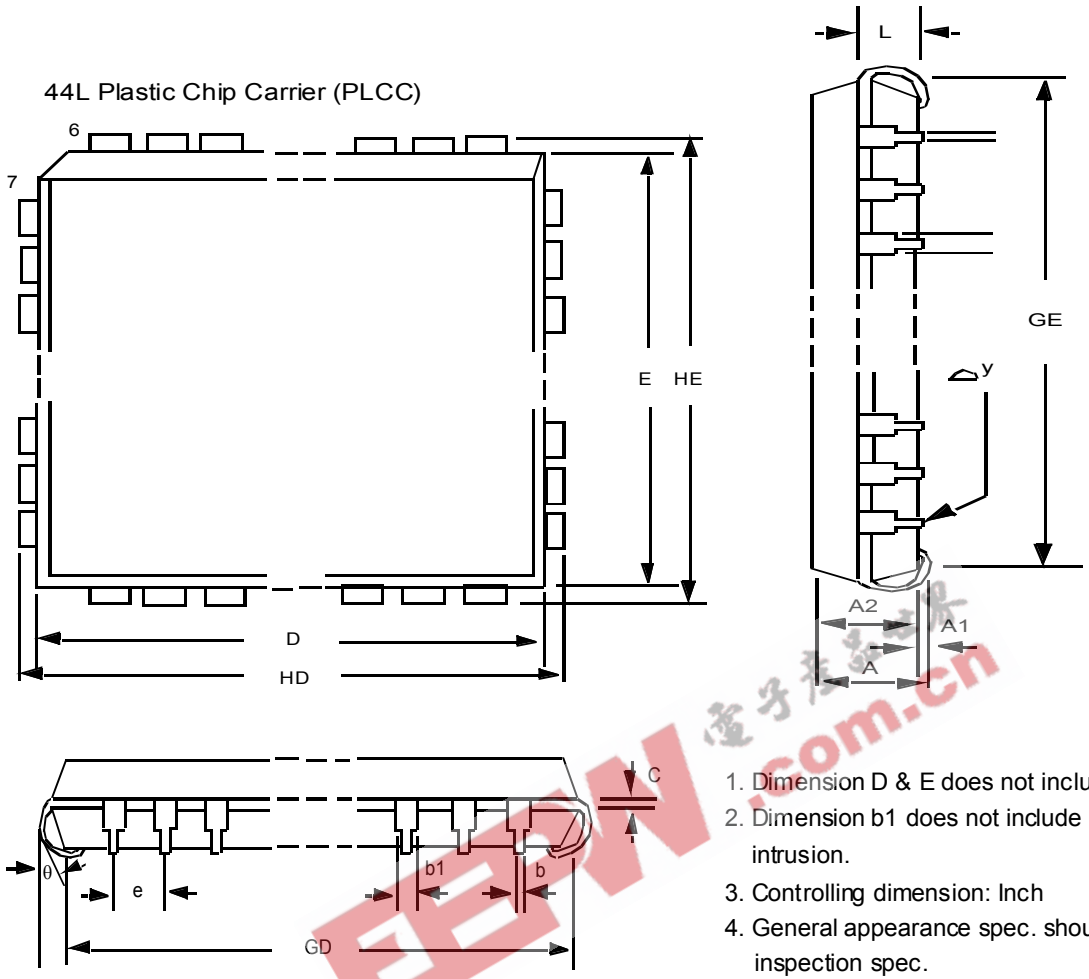
40L 600mil PDIP Information




Note:
1. Dimension D Max & include mold flash or tie bar burrs.
2. Dimension E1 does not include inter lead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dam bar protrusion/ infusion.
5. Controlling dimension is inch.
6. General appearance spec. should base on final visual inspection spec.

| Symbol | Dimension in inch Minimal / maximal | Dimension in inch Minimal / maximal |
|---|---|---|
| A | - / 0.210 | - / 5.33 |
| A1 | 0.010 / - | 0.25 / - |
| A2 | 0.150 / 0.160 | 3.81 / 4.06 |
| B | 0.016 / 0.022 | 0.41 / 0.56 |
| B1 | 0.048 / 0.054 | 1.22 / 1.37 |
| C | 0.008 / 0.014 | 0.20 / 0.36 |
| D | - / 2.070 | - / 52.58 |
| E | 0.590 / 0.610 | 14.99 / 15.49 |
| E1 | 0.540 / 0.552 | 13.72 / 14.02 |
| e1 | 0.090 / 0.110 | 2.29 / 2.79 |
| L | 0.120 / 0.140 | 3.05 / 3.56 |
| a | 0 / 15 | 0 / 15 |
| eA | 0.630 / 0.670 | 16.00 / 17.02 |
| S | - / 0.090 | - / 2.29 |

44L Plastic Chip Carrier (PLCC)

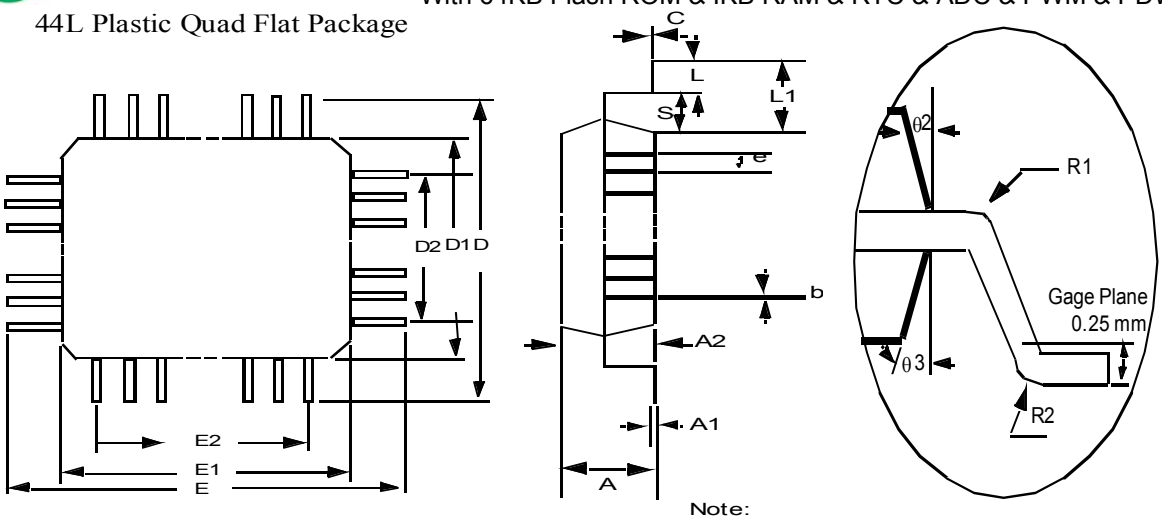


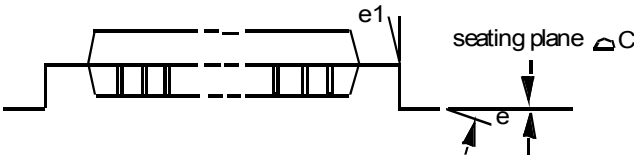

1. Dimension D & E does not include inter lead flash.
2. Dimension b1 does not include dam bar protrusion/ intrusion.
3. Controlling dimension: Inch
4. General appearance spec. should base on final visual inspection spec.

| Symbol | Dimension in inch<br>Minimal / maximal | Dimension in inch<br>Minimal / maximal |
|---|---|---|
| A | - / 0.185 | - / 4.70 |
| A1 | 0.020 / - | 0.51 / - |
| A2 | 0.145 / 0.155 | 3.68 / 3.94 |
| b | 0.026 / 0.032 | 0.66 / 0.81 |
| b1 | 0.016 / 0.022 | 0.41 / 0.56 |
| C | 0.008 / 0.014 | 0.20 / 0.36 |
| D | 0.648 / 0.658 | 16.46 / 16.71 |
| E | 0.648 / 0.658 | 16.46 / 16.71 |
| e | 0.050 BSC | 1.27 BSC |
| GD | 0.590 / 0.630 | 14.99 / 16.00 |
| GE | 0.590 / 0.630 | 14.99 / 16.00 |
| HD | 0.680 / 0.700 | 17.27 / 17.78 |
| HE | 0.680 / 0.700 | 17.27 / 17.78 |
| L | 0.090 / 0.110 | 2.29 / 2.79 |
| θ | - / 0.004 | - / 0.10 |
| y | / | / |

Specifications subject to change without notice contact your sales representatives for the most recent information.

44L Plastic Quad Flat Package




Note:
Dimension D1 and E1 do not include mold protrusion. Allowance protrusion is 0.25mm per side.
Dimension D1 and E1 do include mold mismatch and are determined datum plane.
Dimension b does not include dam bar protrusion. Allowance dam bar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dam bar cannot be located on the lower radius or the lead foot.

| Symbol | Dimension in inch<br>Minimal / maximal | Dimension in inch<br>Minimal / maximal |
|---|---|---|
| A | - / 0.100 | - / 2.55 |
| A1 | 0.006 / 0.014 | 0.15 / 0.35 |
| A2 | 0.071 / 0.087 | 1.80 / 2.20 |
| b | 0.012 / 0.018 | 0.30 / 0.45 |
| c | 0.004 / 0.009 | 0.09 / 0.20 |
| D | 0.520 BSC | 13.20 BSC |
| D1 | 0.394 BSC | 10.00 BSC |
| D2 | 0.315 | 8.00 |
| E | 0.520 BSC | 13.20 BSC |
| E1 | 0.394 BSC | 10.00 BSC |
| E2 | 0.315 | 8.00 |
| e | 0.031 BSC | 0.80 BSC |
| L | 0.029 / 0.041 | 0.73 / 1.03 |
| L1 | 0.063 | 1.60 |
| R1 | 0.005 / - | 0.13 / - |
| R2 | 0.005 / 0.012℃ | 0.13 / 0.30 |
| S | 0.008 / - | 0.20 / - |
| θ | 0℃ / 7℃ | as left |
| θ1 | 0℃ / - | as left |
| θ2 | 10℃ REF | as left |
| θ3 | 7℃ REF | as left |
| ⌓C | 0.004 | 0.10 |