



**16-BIT CONSTANT CURRENT LED DRIVER**

**GENERAL DESCRIPTION**

The SM16706P/SP/F/FN are specifically designed for LED display constant current drivers.

This constant current output circuits is able to setup by external resistor ( $I_{OUT} = 5 \sim 90\text{mA}$ ).

This IC is monolithic integrated circuit designed to be used together with Bi-CMOS process.

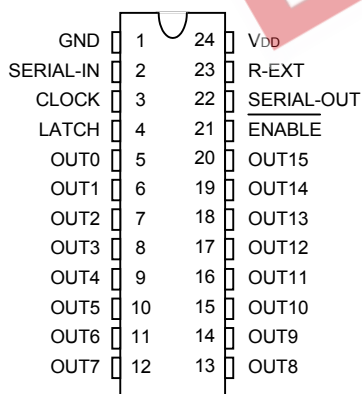
The devices consist of 16bit shift register, latch, AND-GATE and Constant Current Drivers.

**FEATURES**

- \* Constant Current Output :  
can setup all output current with one resistor for 5 to 90mA.
- \* Maximum Clock Frequency :  
 $f_{CLK} = 25$  (MHz)  
(Cascade Connect Operate,  
 $T_{opr} = 25^{\circ}\text{C}$ )
- \* 5V CMOS Compatible Input
- \* 24 pin SKINY DIP,SDIP, SOP or SSOP package
- \* Constant Output Current Matching :

Output-GND Voltage	Current Matching	Output Current
$\geq 0.4\text{V}$	$\pm 6.0\%$	5 ~ 40mA
$\geq 0.7\text{V}$	$\pm 6.0\%$	5 ~ 90mA

**PIN ASSIGNMENTS**



SM16706

Part Number	Package Type
SM16706P	24pin SKINY DIP
SM16706SP	24pin SDIP
SM16706F	24pin SOP
SM16706FN	24pin SSOP



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**PIN DESCRIPTION**

Pin NO.	I / O	Pin Name	Function Description
1		GND	GND terminal
2	I	SERIAL-IN	Terminal of serial-data input to the shift register.
3	I	CLOCK	Input terminal of a clock for shift register on rising edge.
4	I	LATCH	Input terminal of data strobe. Latches pass data with "H" level input of LATCH-terminal, and hold data with "L" level input.
5 ~ 20	O	OUT0 ~ 15	Constant Current-sinking output terminals.
21	I	ENABLE	Input terminal of output enable. All outputs (OUT0~15) do off with "H" level input of ENABLE-terminal and do on with "L" level input.
22	O	SERIAL-OUT	Output terminal of serial-data for next SERIAL-IN terminal.
23	I / O	R-EXT	An external resistor at this terminal establishes all of the output current.
24		VDD	5V supply voltage terminal.



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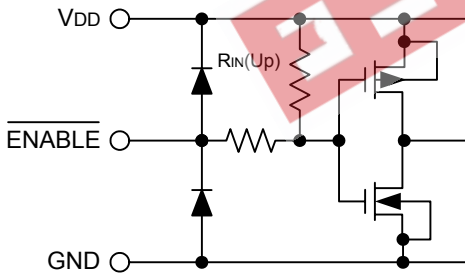
**TRUTH TABLE**

CLOCK	LATCH	ENABLE	SERIAL-IN	OUT0 ... OUT7 ... OUT15	SERIAL-OUT
UP	H	L	$D_n$	$D_n \dots D_{n-7} \dots D_{n-15}$	$D_{n-15}$
UP	L	L	$D_{n+1}$	No change	$D_{n-14}$
UP	H	L	$D_{n+2}$	$D_{n+2} \dots D_{n-5} \dots D_{n-13}$	$D_{n-13}$
DOWN	X	L	$D_{n+3}$	$D_{n+2} \dots D_{n-5} \dots D_{n-13}$	$D_{n-13}$
DOWN	X	H	$D_{n+3}$	Off	$D_{n-13}$

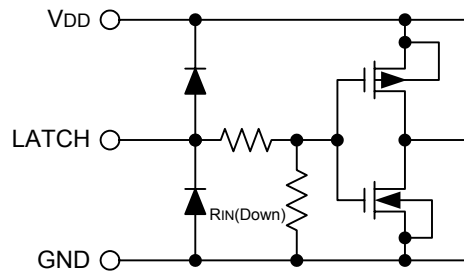
Note : 1. OUT0~15=on when  $D_n$ ="H" ; OUT0~15=off when  $D_n$ ="L".  
 2. In order to ensure that the level of the power supply voltage is correct, an external resistor must be connected between R-EXT and GND.

**EQUIVALENT CIRCUIT OF INPUTS AND OUTPUTS**

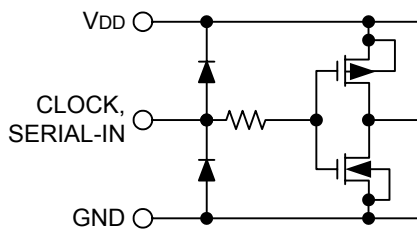
**1. ENABLE terminal**



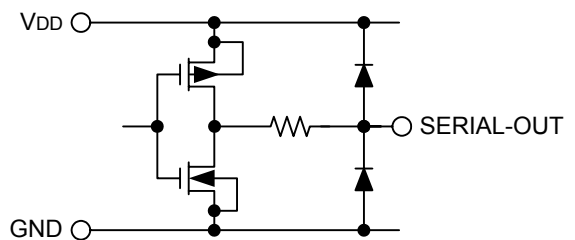
**2. LATCH terminal**



**3. CLOCK, SERIAL-IN terminal**



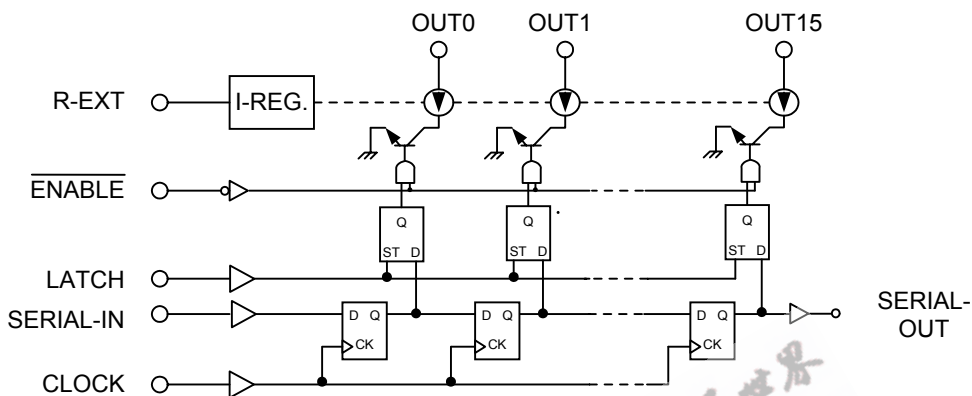
**4. SERIAL-OUT terminal**



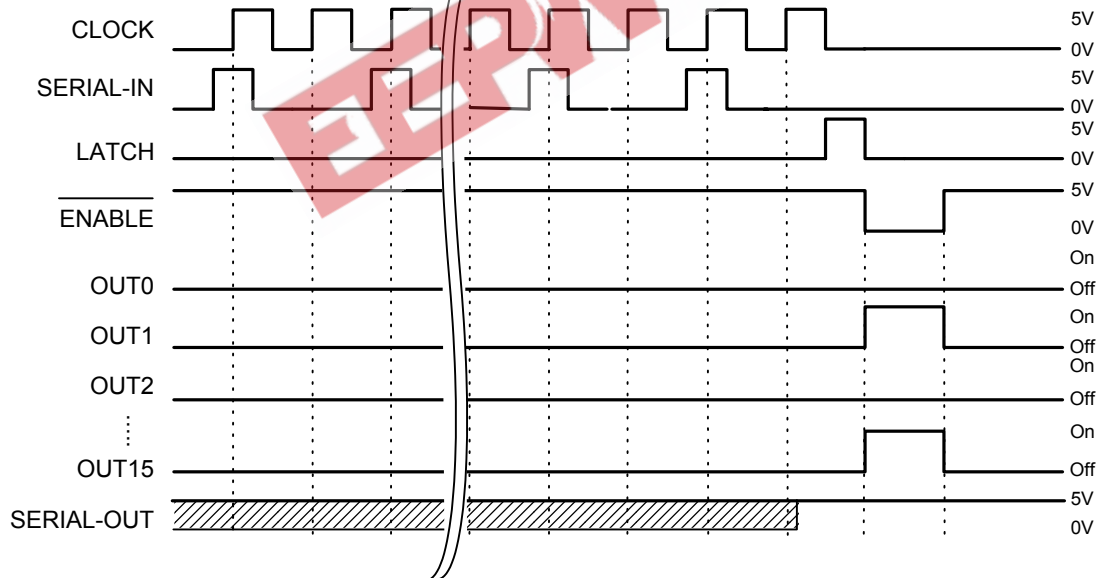


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**BLOCK DIAGRAM**



**TIMING DIAGRAM**



Note : Latches are level sensitive, not rising edges sensitive and not synchronous CLOCK.  
Input of LATCH-terminal to H Level, data passes latches, and input of LATCH -terminal to L level, data hold latches.



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**MAXIMUM RATINGS (Ta = 25°C)**

Characteristic	Symbol	Rating	Unit
Supply Voltage	VDD	0 ~ 7.0	V
Input Voltage	VIN	- 0.4 ~ VDD +0.4	V
Output Current	IOUT	90	mA
Output Voltage	VOUT	- 0.5 ~ 20.0	V
Clock Frequency	fCLK	25	MHz
GND Terminal Current	IGND	1440	mA
Power Dissipation	Pd	1.78 (DIP : FREE AIR, Ta = 25°C)	W
		1.00 (SOP/ SSOP : ON PCB, Ta = 25°C)	
Thermal Resistance	Rth (j-a)	70 (DIP : FREE AIR, Ta = 25°C)	°C / W
		120 (SOP/ SSOP : ON PCB, Ta = 25°C)	
Operating Temperature	Topr	-40 ~ 85	°C
Storage Temperature	Tstg	-55 ~ 150	°C

(Note) DIP : Ambient temperature derated above 25°C in the proportion of 14.2mW / °C  
 SOP/ SSOP: Ambient temperature derated above 25°C in the proportion of 8.3mW / °C

**RECOMMENDED OPERATING CONDITION (Ta = - 40 ~ 85°C unless otherwise noted)**

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	VDD	–	4.5	5.0	5.5	V
Output Voltage	VOUT	–	–	–	15.0	V
Output Current	Io	OUTn,DC test circuit	5	–	88	mA
	IOH	SERIAL-OUT	–	–	1.0	
	IOL	SERIAL-OUT	–	–	-1.0	
Input Voltage	VIH	–	0.7 VDD	–	VDD +0.3	V
	VIL	–	-0.3	–	0.3 VDD	
LATCH Pulse Width	tw LAT	VDD = 4.5 ~ 5.5V	20	–	–	ns
CLOCK Pulse Width	tw CLK		20	–	–	ns
ENABLE Pulse Width	tw EN		-500	–	–	ns
Set-up Time for DATA	tsetup(D)		20	–	–	ns
Hold Time for DATA	thold (D)		20	–	–	ns
Set-up Time for LATCH	tsetup(L)		20	–	–	ns
Clock Frequency	fCLK		Cascade operation	–	–	25
Power Dissipation	Pd	Ta = 85°C(DIP FREE AIR)	–	–	0.92	W
		Ta = 85°C (SOP/ SSOP ON PCB)	–	–	0.50	



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**ELECTRICAL CHARACTERISTICS (V<sub>DD</sub> = 5.0V, T<sub>a</sub> = 25°C unless otherwise noted)**

Characteristic		Symbol	Condition	Min.	Typ.	Max.	Unit
Input Voltage	"H" Level	V <sub>IH</sub>	—	0.7 V <sub>DD</sub>	—	V <sub>DD</sub>	V
	"L" Level	V <sub>IL</sub>	—	GND	—	0.3 V <sub>DD</sub>	
Output Leakage Current		I <sub>OH</sub>	V <sub>OH</sub> = 15.0V	—	—	10	μA
Output Voltage	SERIAL-OUT	V <sub>OL</sub>	I <sub>OL</sub> = 1.0mA	—	—	0.4	V
		V <sub>OH</sub>	I <sub>OH</sub> = -1.0mA	4.6	—	—	
Output Current 1		I <sub>OL1</sub>	V <sub>CE</sub> = 0.7V R <sub>EXT</sub> = 470Ω (Include skew)	34.1	40.0	45.9	mA
		I <sub>OL2</sub>	V <sub>CE</sub> = 0.4V	33.7	39.5	45.3	
Current Skew		Δ I <sub>OL1</sub>	I <sub>OUT</sub> = 40mA V <sub>CE</sub> = 0.4V R <sub>EXT</sub> = 470Ω	—	± 1.5	± 4.0	%
Output Current 2		I <sub>OL3</sub>	V <sub>CE</sub> = 0.7V R <sub>EXT</sub> = 240Ω (Include skew)	66.3	75.0	89.7	mA
		Current Skew	Δ I <sub>OL2</sub>	I <sub>OUT</sub> = 75mA V <sub>CE</sub> = 0.7V R <sub>EXT</sub> = 240Ω	—	± 1.5	
Supply Voltage Regulation		% / V <sub>DD</sub>	R <sub>EXT</sub> = 470Ω, T <sub>a</sub> = -40 ~ 85°C	—	2.5	5.0	% / V
Pull-Up Resistor		R <sub>IN (up)</sub>	—	150	300	600	KΩ
Pull-Down Resistor		R <sub>IN (down)</sub>	—	100	200	400	KΩ
Supply Current	"OFF"	I <sub>DD (off) 1</sub>	R <sub>EXT</sub> = OPEN, OUT0 ~ 15 = off	—	0.9	1.5	mA
		I <sub>DD (off) 2</sub>	R <sub>EXT</sub> = 470Ω, OUT0 ~ 15 = off	3.5	4.6	8.0	
		I <sub>DD (off) 3</sub>	R <sub>EXT</sub> = 240Ω, OUT0 ~ 15 = off	6.5	8.0	15.0	
	"ON"	I <sub>DD (on) 1</sub>	R <sub>EXT</sub> = 470Ω, OUT0 ~ 15 = on	7.0	9.3	18.0	
		V <sub>DD (on) 2</sub>	R <sub>EXT</sub> = 240Ω, OUT0 ~ 15 = on	10.0	18.0	32.0	



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**SWITCHING CHARACTERISTICS (Ta = 25 °C unless otherwise noted)**

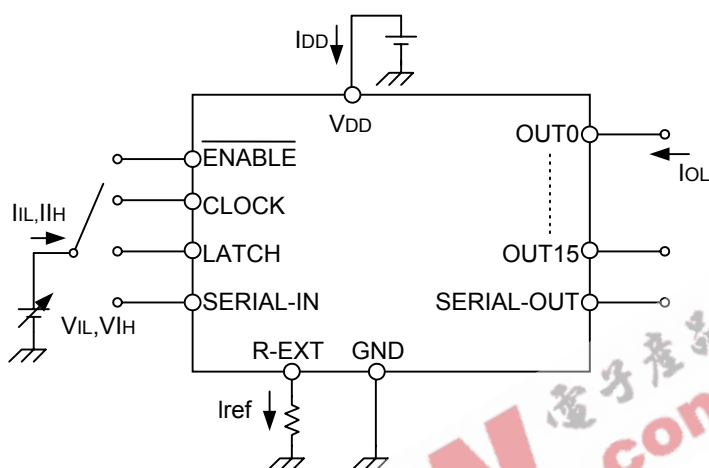
Characteristic		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time ("L" to "H")	SERIAL-IN-OUTn	tpLH	VDD = 5.0V REXT = 470Ω VL = 3.0V RL = 68Ω CL = 10 pF	–	160	320	ns
	LATCH-OUTn			–	160	320	
	ENABLE-OUTn			–	160	320	
	CLOCK-SERIAL-OUT			–	20	40	
Propagation Delay Time ("H" to "L")	SERIAL-IN-OUTn	tpHL	VDD = 5.0V REXT = 470Ω VL = 3.0V RL = 68Ω CL = 10 pF	–	160	320	ns
	LATCH-OUTn			–	160	320	
	ENABLE-OUTn			–	160	320	
	CLOCK-SERIAL-OUT			–	20	40	
Output Rise Time		tor		150	170	600	ns
Output Fall Time		tof		150	180	600	



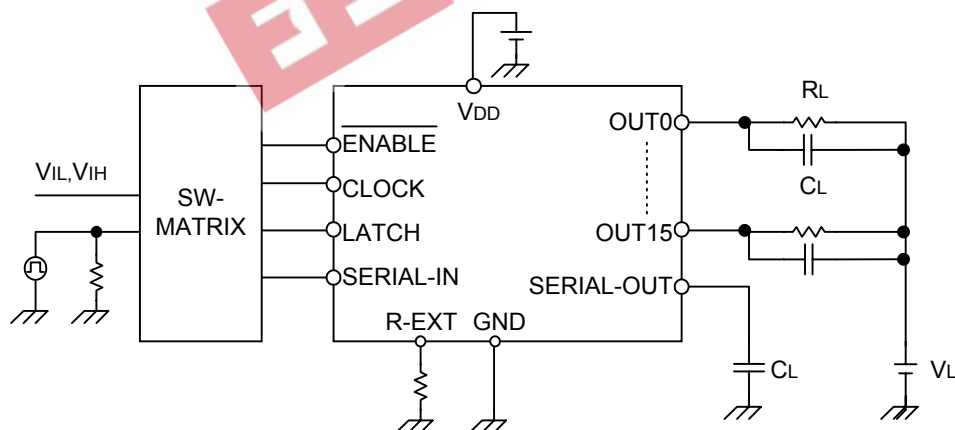
## 16-BIT CONSTANT CURRENT LED DRIVER

### TEST CIRCUIT

DC Characteristic



AC Characteristic



### PRECAUTIONS FOR USING

Utmost care is necessary in the design of the output line, VDD and GND line, since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

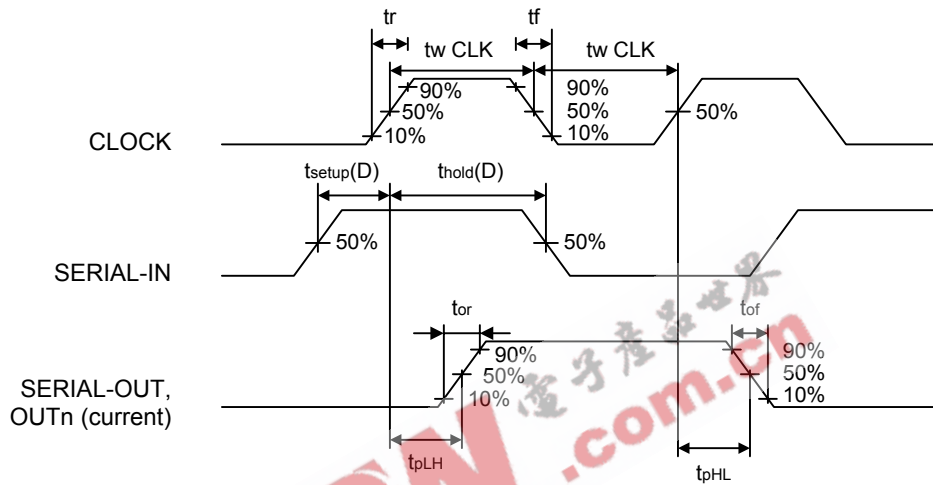




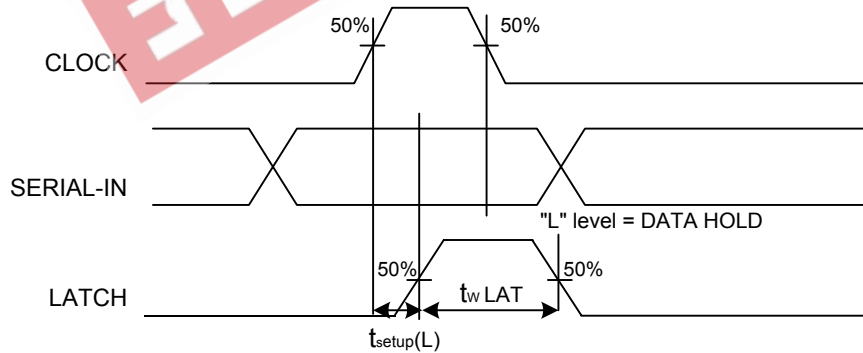
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**TIMING WAVEFORM**

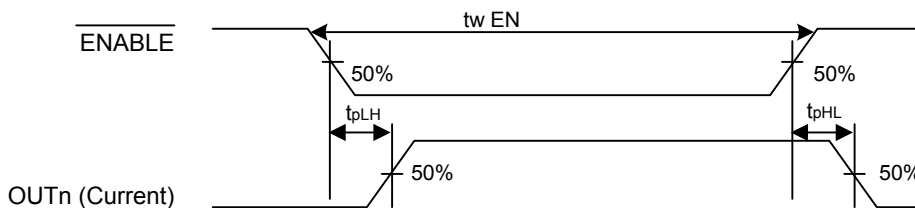
**1. CLOCK, SERIAL-IN, SERIAL-OUT, OUTn**



**2. CLOCK-LATCH**



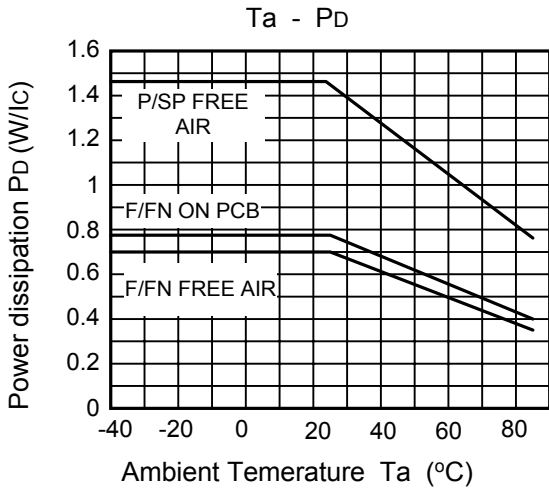
**3. ENABLE-OUTn**



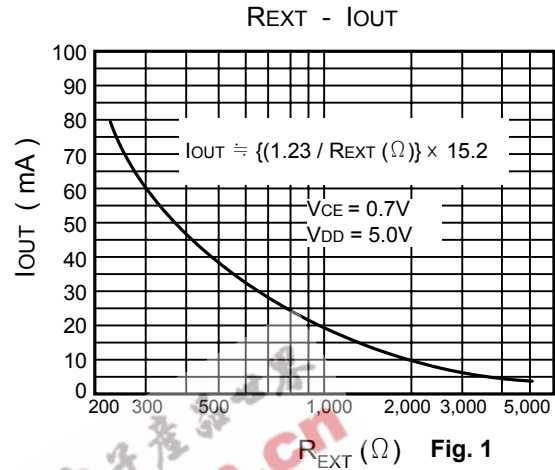


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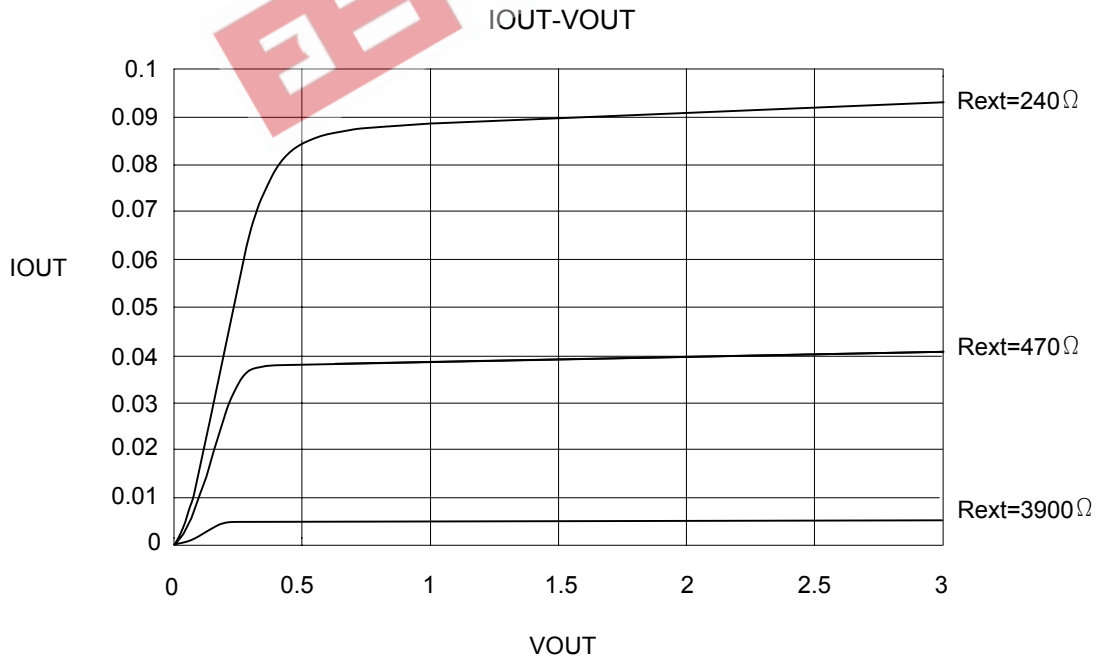
**Output Current - Duty (LED turn-on rate)**



**Output Current - REXT Resistor**



**Output Current - Output Voltage**





## 16-BIT CONSTANT CURRENT LED DRIVER

### [1] Output Current ( $I_{OUT}$ )

$I_{OUT}$  is set by the external resistor ( $R_{EXT}$ ) as shown in Figure1.

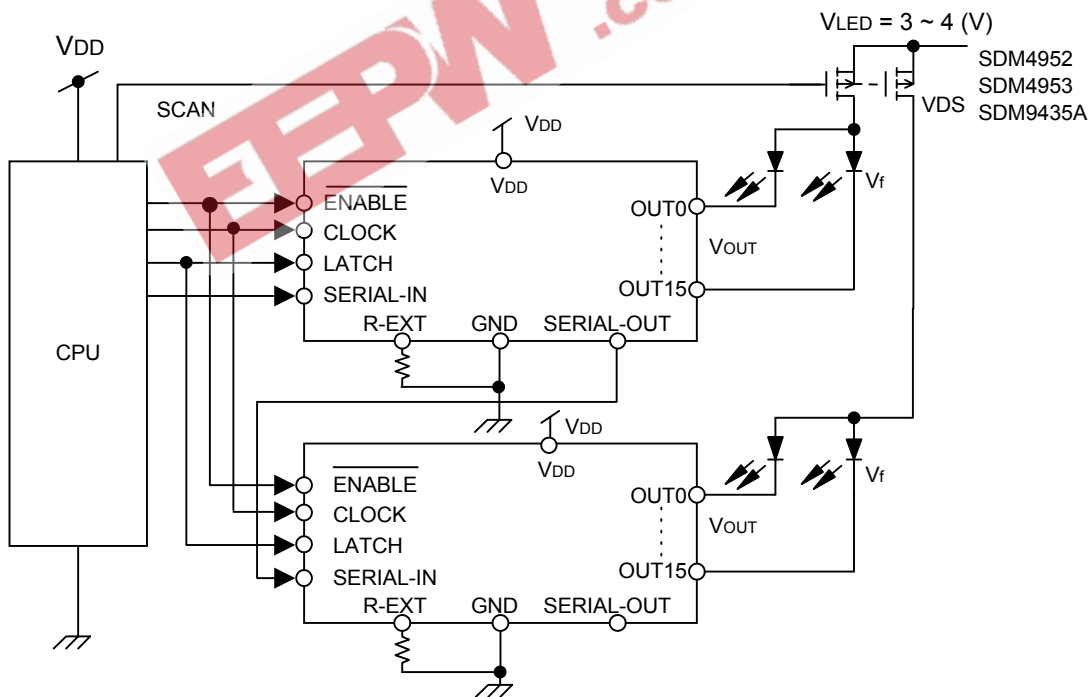
### [2] Total supply voltage ( $V_{LED}$ )

This device can operate at 0.4~0.7V ( $V_{OUT}$ ). When a higher voltage is input to the device, the excess voltage is consumed inside the device, that leads to more power dissipation. In order to minimize power dissipation and loss, we would like to recommend to set the total supply voltage as shown below,

$$V_{LED} \text{ (total supply voltage)} = V_{OUT} \text{ (IC Supply Voltage)} + V_f \text{ (LED Forward voltage)} + V_{DS} \text{ (MOSFET Voltage Drop)}$$

When the total supply is too high considering the power dissipation of this device, an additional R can decrease the OUT voltage ( $V_{OUT}$ ).

### PATTERN LAYOUT



### [3] Pattern Layout

This device has only one ground pin that means signal ground pin and power ground pin are common. If ground pattern layout contains large inductance and impedance, and the voltage between ground and LATCH, CLOCK terminals exceeds 2.5V by switching noise during operation, this device may misoperate. So we would advise you to pay attention to pattern layout to minimize ground inductance.

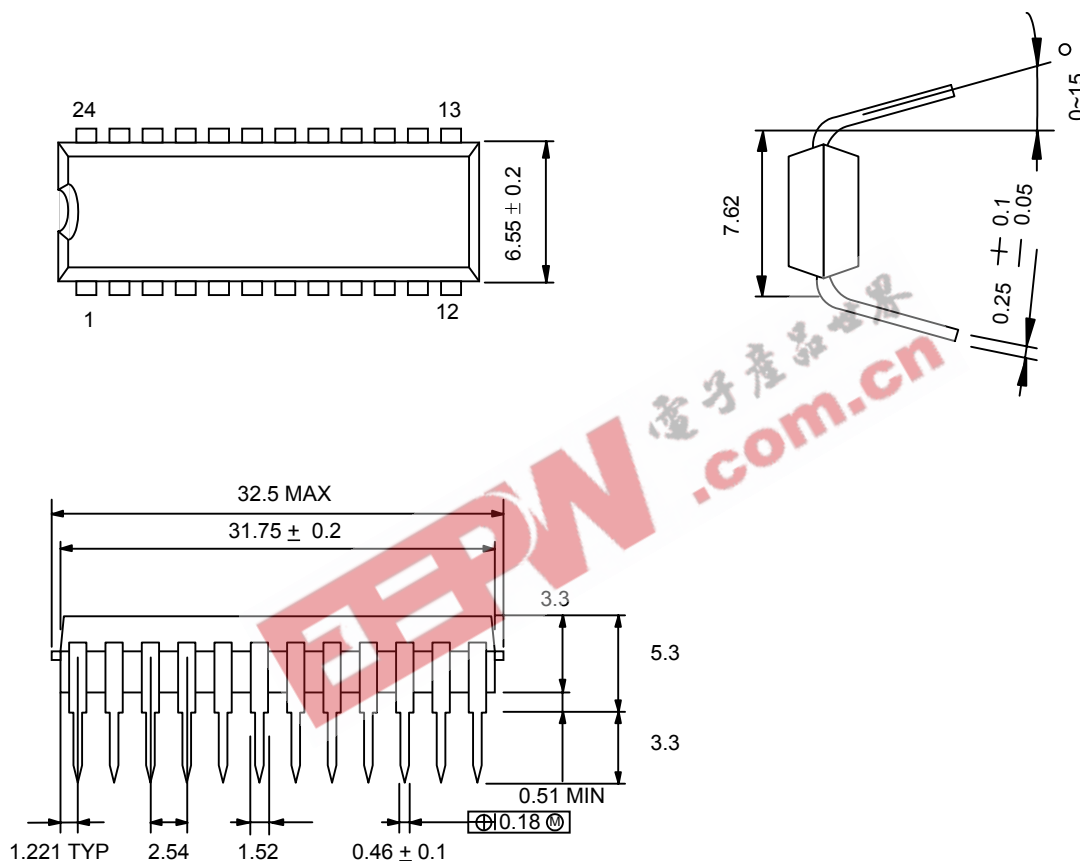


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**PACKAGE OUTLINE**

SM16706P 24 PIN SKINY DIP

Unit : mm



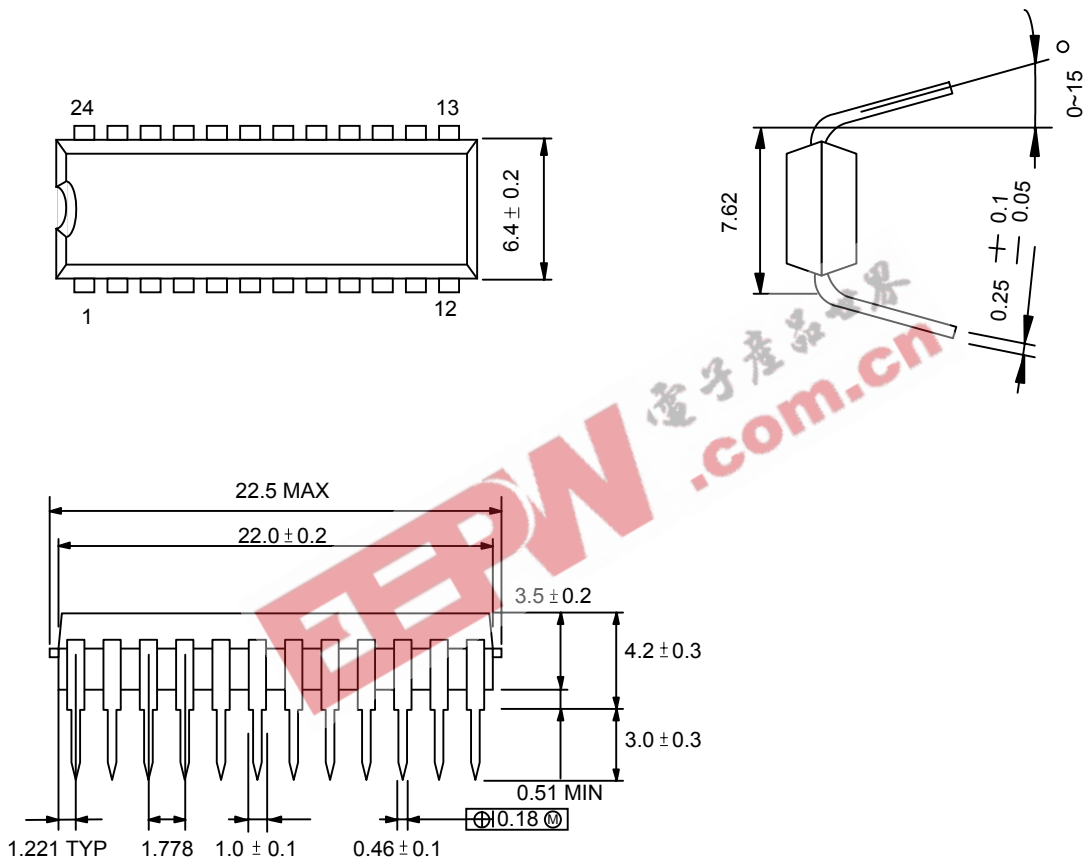


**16-BIT CONSTANT CURRENT LED DRIVER**

**PACKAGE OUTLINE**

SM16706SP 24 PIN SDIP

Unit : mm



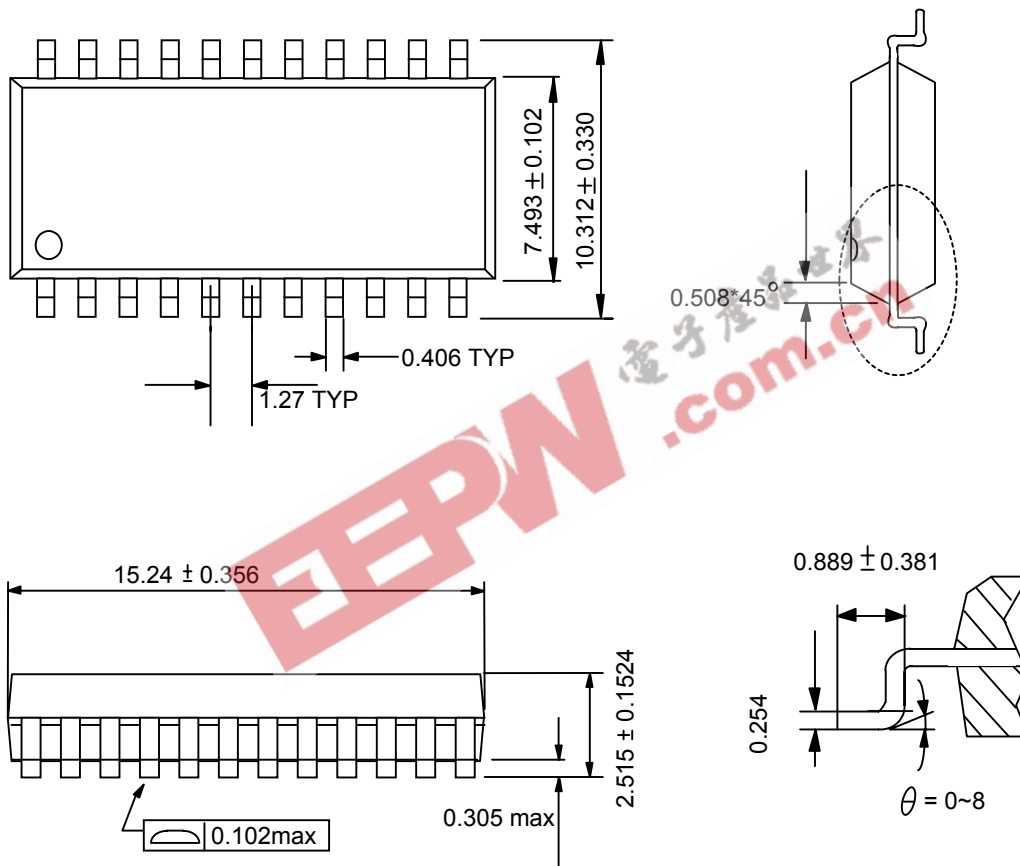


**16-BIT CONSTANT CURRENT LED DRIVER**

**PACKAGE OUTLINE**

SM16706F 24 PIN SOP

Unit : mm





**16-BIT CONSTANT CURRENT LED DRIVER**

**PACKAGE OUTLINE**

SM16706FN 24 PIN SSOP

Unit : mm

