SL05T1 Series

300 Watt, SOT-23 Low Capacitance TVS for High Speed Line Protections

This new family of TVS offers transient overvoltage protection with significantly reduced capacitance. The capacitance is lowered by integrating a compensating diode in series. This integrated solution offers ESD protection for high speed interfaces such as communication systems, computers, and computer peripherals.

Specification Features:

- TVS Diode in Series with a Compensating Diode Offers <5 pF Capacitance
- ESD Protection Meeting IEC 61000–4–2, 4–4, 4–5
- Peak Power Rating of 300 Watts, 8 × 20 μs
- Bi–Direction Protection Can Be Achieved By Using Two Devices
- Flammability Rating UL 94 V–0

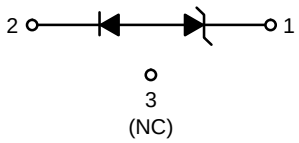
Mechanical Characteristics:

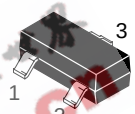
CASE: Void-free, transfer-molded, thermosetting plastic case
FINISH: Corrosion resistant finish, easily solderable
MAXIMUM CASE TEMPERATURE FOR SOLDERING PURPOSES:
260°C for 10 Seconds
Package designed for optimal automated board assembly
Small package size for high density applications
Available in 8 mm Tape and Reel

Use the Device Number to order the 7 inch/3,000 unit reel. Replace the “T1” with “T3” in the Device Number to order the 13 inch/10,000 unit reel.

ON Semiconductor®

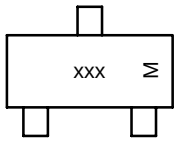
http://onsemi.com





SOT–23
CASE 318
STYLE 26

MARKING DIAGRAM



xxx = Device Code
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping
SL05T1	SOT–23	3000/Tape & Reel
SL15T1	SOT–23	3000/Tape & Reel
SL24T1	SOT–23	3000/Tape & Reel
SL05T3	SOT–23	10,000/Tape & Reel
SL15T3	SOT–23	10,000/Tape & Reel
SL24T3	SOT–23	10,000/Tape & Reel

DEVICE MARKING INFORMATION

See specific marking information in the device marking column of the table on page 3 of this data sheet.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Power Dissipation @ 8x20 usec (Note 1) @ $T_L \le 25°C$	P_{pk}	300	W
IEC 61000–4–2 Level 4	V_{pp}		
Contact Discharge		±8	kV
Air Discharge		±16	kV
IEC 61000–4–4 EFT		40	Amps
IEC 61000–4–5 Lightning		12	Amps
Total Power Dissipation on FR–5 Board (Note 2) @ $T_A = 25°C$	P_D	225	mW
Derate above 25°C		1.8	mW/°C
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	556	°C/W
Total Power Dissipation on Alumina Substrate (Note 3) @ $T_A = 25°C$	P_D	300	mW
Derate above 25°C		2.4	mW/°C
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	– 55 to +150	°C
Lead Solder Temperature – Maximum (10 Second Duration)	T_L	260	°C

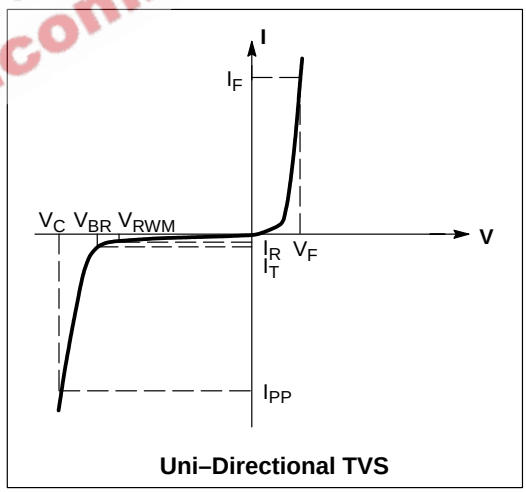
1. Non–repetitive current pulse per Figure 2
2. FR–5 = 1.0 x 0.75 x 0.62 in.
3. Alumina = 0.4 x 0.3 x 0.024 in., 99.5% alumina

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

UNIDIRECTIONAL (Circuit tied to Pins 1 and 3 or 2 and 3)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
ΘV_{BR}	Maximum Temperature Coefficient of V_{BR}
I_F	Forward Current
V_F	Forward Voltage @ I_F
Z_{ZT}	Maximum Zener Impedance @ I_{ZT}
I_{ZK}	Reverse Current
Z_{ZK}	Maximum Zener Impedance @ I_{ZK}



Uni–Directional TVS

ELECTRICAL CHARACTERISTICS

Device	Device Marking	V_{RWM} (Volts)	I_R @ V_{RWM} (μA)	Breakdown Voltage (Note 4) V_{BR} @ 1 mA (Volts) Min	Breakdown Voltage (Note 4) V_{BR} @ 1 mA (Volts) Max	V_C, Clamping Voltage (Note 5) @ 1 Amp (Volts)	V_C, Clamping Voltage (Note 5) @ 5 Amp (Volts)	Max I_{PP} (Amps)	Capacitance @ V_R = 0 V, 1 MHz (pF) Typ	Capacitance @ V_R = 0 V, 1 MHz (pF) Max
SL05	L05	5.0	20	6.0	8.0	9.8	11	17	3.5	5.0
SL15	L15	15	1.0	16.7	18.5	24	30	10	3.5	5.0
SL24	L24	24	1.0	26.7	29	43	55	5.0	3.5	5.0

4. V_{BR} measured at pulse test current of 1 mA at an ambient temperature of 25°C
5. Surge current waveform per Figure 2

TYPICAL CHARACTERISTICS

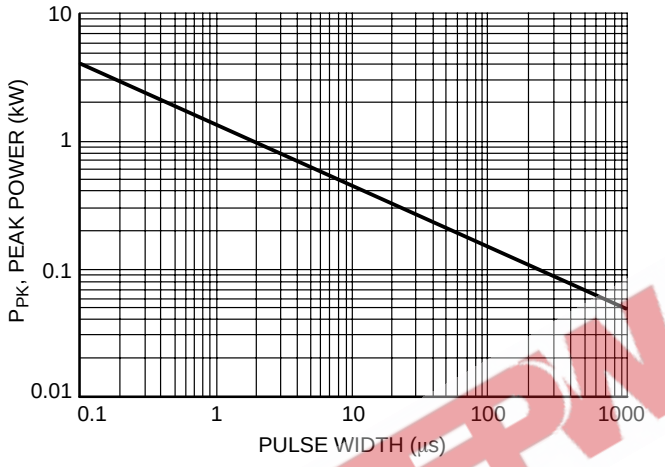


Figure 1. Maximum Peak Power Rating

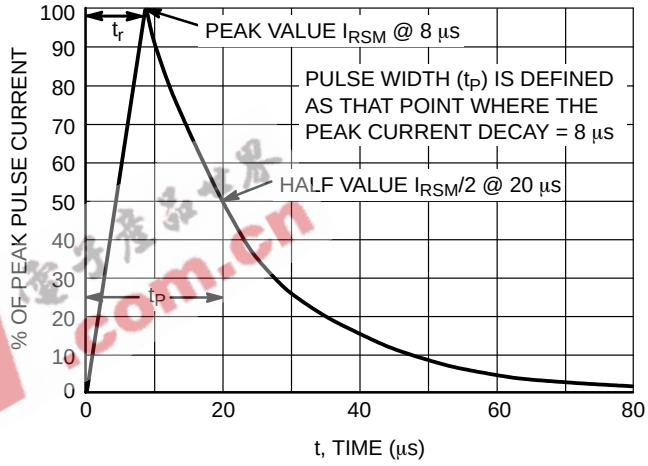


Figure 2. 8 × 20 μs Pulse Waveform

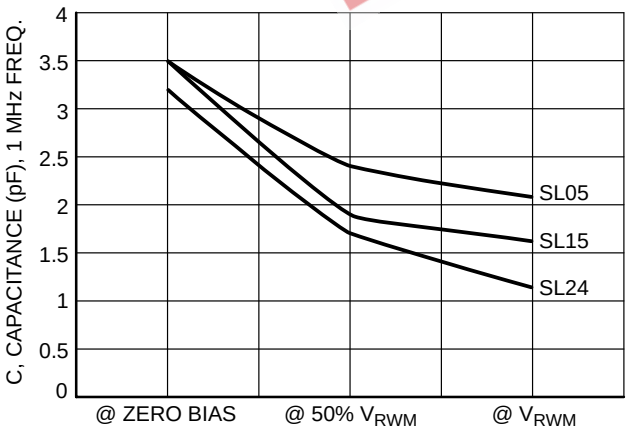


Figure 3. Typical Junction Capacitance

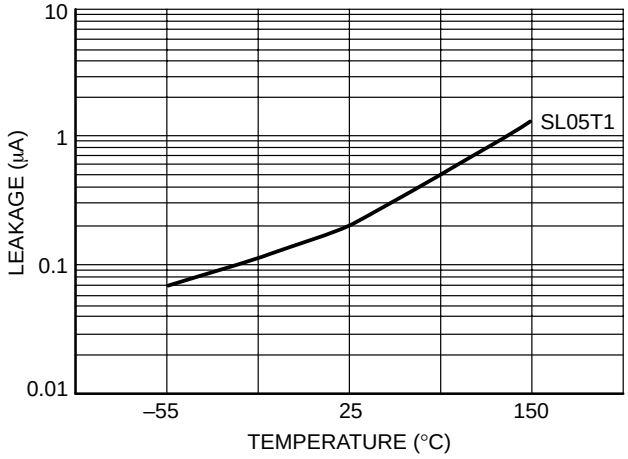
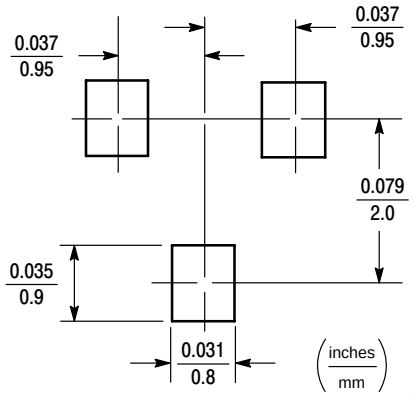


Figure 4. Typical Leakage Over Temperature

INFORMATION FOR USING THE SOT–23 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT–23

SOT–23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the SOT–23 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150°C - 25°C}{556°C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad®. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* * Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

Applications Background

This new family of TVS devices (SL05T1 series) are designed to protect sensitive electronics such as communications systems, computers, and computer peripherals against damage due to ESD conditions or transient voltage conditions. Because of their low capacitance value (less than 5 pF), they can be used in high speed I/O data lines. Low capacitance is achieved by integrating a compensating diode in series with the TVS which is basically based in the below theoretical principle:

- Capacitance in parallel: CT = C1+C2+....+Cn
- Capacitance in series: 1/CT = (1/C1)+(1/C2)+....+(1/Cn)

The Figure 5 shows the integrated solution of the SL05T1 series device:

Figure 5.

In the case that an over–voltage condition occurs in the I/O line protected by the SL05T1 series device, the TVS is reversed–biased while the compensation diode is forward–biased so the resulting current due to the transient voltage is drained to ground.

If protection in both polarities is required, an additional device is connected in inverse–parallel with reference to the first one, the Figure 6 illustrates the inverse–parallel connection for bi–directional or unidirectional lines:

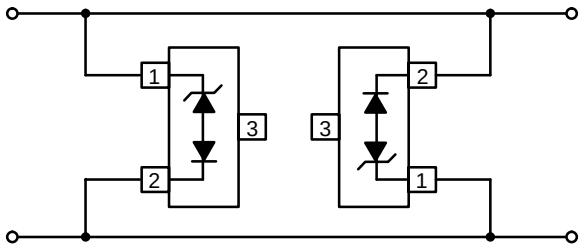


Figure 6.

An alternative solution to protect unidirectional lines, is to connect a fast switching steering diode in parallel with the SL05T1 series device. When the steering diode is forward–biased, the TVS will avalanche and conduct in reverse direction. It is important to note that by adding a steering diode, the effective capacitance in the circuit will be increased, therefore the impact of adding a steering diode must be taken in consideration to establish whether the incremental capacitance will affect the circuit functionality or not. The Figure 7 shows the connection between the steering diode and the SL05T1 series device:

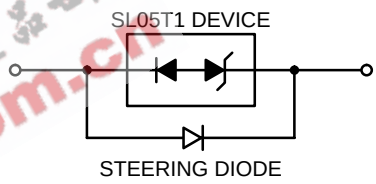


Figure 7.

Another typical application in which the SL05T1 series device can be utilized, is to protect multiple I/O lines. The protection in each of the I/O lines is achieved by connecting two devices in inverse–parallel. The Figure 8 illustrates how multiple I/O line protection is achieved:

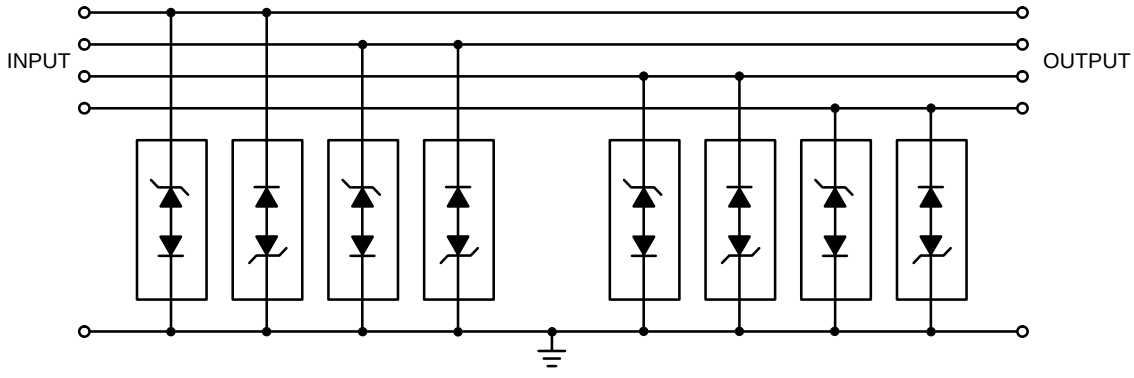


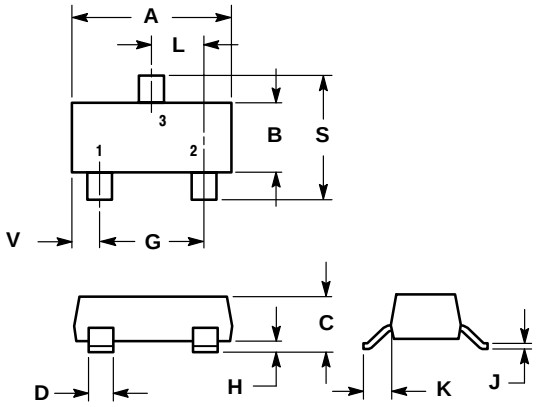
Figure 8.

For optimizing the protection, it is recommended to use ground planes and short path lengths to minimize the PCB's ground inductance.

Transient Voltage Suppressors – Surface Mount

300 Watts Peak Power

SOT–23
TO–236AB
CASE 318–09
ISSUE AH



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIUMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318–01, –02, AND –06 OBSOLETE, NEW STANDARD 318–09.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0385	0.0498	0.99	1.26
D	0.0140	0.0200	0.36	0.50
G	0.0670	0.0826	1.70	2.10
H	0.0040	0.0098	0.10	0.25
J	0.0034	0.0070	0.085	0.177
K	0.0180	0.0236	0.45	0.60
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.0984	2.10	2.50
V	0.0177	0.0236	0.45	0.60

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

Notes

SL05T1 Series

Thermal Clad is a registered trademark of the Bergquist Company.

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–0031
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Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local
Sales Representative.