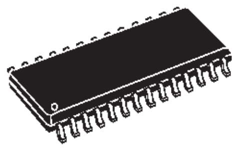
ST5451

ISDN HDLC AND GCI CONTROLLER

- MONOLITHIC ISDN ORIENTED HDLC AND GCI CONTROLLER.
- GCI AND µW/DSI COMPATIBLE.
- FULLY CONTROLLING GCI AND GCI-SCIT M & C/I CHANNELS MANAGEMENT.
- FULLY SUPPORTING LAPB AND LAPD PROTOCOL ON B OR D CHANNEL.
- EASILY INTERFACEABLE WITH ANY KIND OF STANDARD NON MULTIPLEXED OR MULTIPLEXED BUS MICROPROCESSOR.
- DMA ACCESS WITH MULTIPLEXED BUS µP
- CAN HANDLE AND STORE AT THE SAME TIME TWO FRAMES IN TRANSMISSION (64bytes FIFO Tx) AND EIGHT FRAMES IN RECEPTION (64bytes FIFO Rx)
- COMPATIBLE WITH ALL THE STMicroelectronics ISDN PRODUCT FAMILY.



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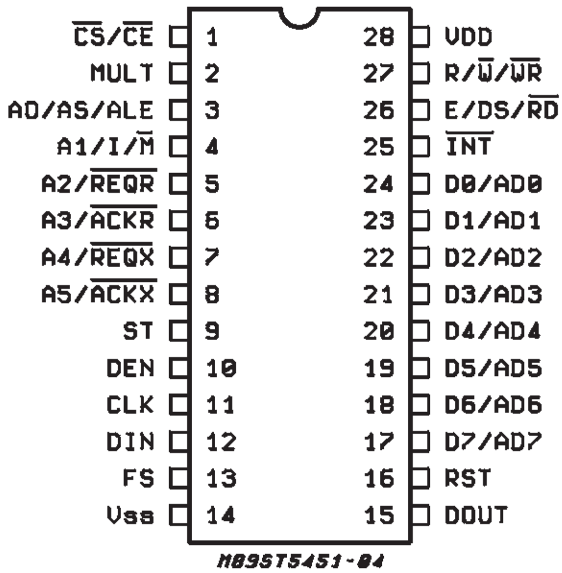
ORDERING NUMBER: ST5451D

PIN CONNECTION (Top view)



GENERAL DESCRIPTION

ST5451 HDLC and GCI controller is a CMOS circuit fully developed by STMicroelectronics and diffused in advanced 1.2 µm HCMOS3 technology.

The device is intended to be used mainly in ISDN applications, in Terminal (TE) and in Line Terminations (LT).

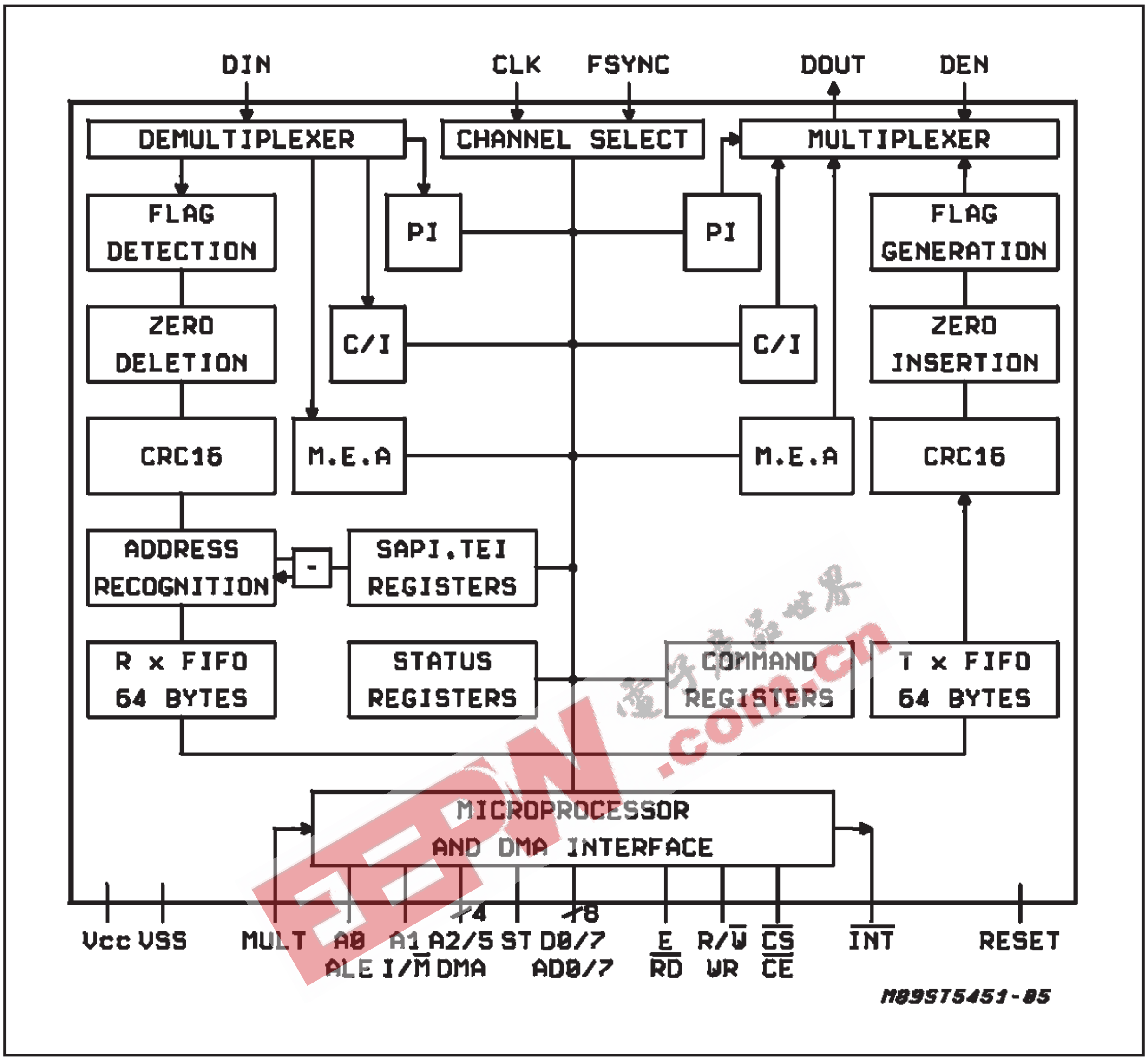
ST5451 can handle HDLC packets either on 16Kbit/s D channel or 64 Kbit/s B channel; it can work with a wide range of PCM signals going from GCI (General Circuit Interface) to DSI (Digital System Interface) to any PCM-like stream.

ST5451 is a complete GCI controller designed to comply with the GCI and GCI-SCIT (Special Circuit Interface for Terminal) completely handling Monitor (M) and Command/Indicate (C/I) channels.

ST5451 can be easily controlled by many different kind of microprocessors or microcontrollers having either non-multiplexed or multiplexed bus structure.

ST5451 can be used in connection with ST5420/1 S Interface Devices (SID-µW and SID-GCI) and ST5080 Programmable ISDN Combo (PIC) in Terminals and with ST5410 U Interface Device (UID) in Line Terminations.

BLOCK DIAGRAM



PIN DESCRIPTION

NAME	PIN	TYPE	FUNCTION
$\overline{\text{CS}}$	1	I	Chip Select. A low level enables ST5451 for read/write operations.
$\overline{\text{INT}}$	25	O	Interrupt request is asserted by ST5451 when it request a service. Open drain output.
MULT	2	I	Multiplexed Bus. Indicates the µP bus interface selected. MULT = 1: multiplexed bus and DMA available. MULT = 0: address and data bus separated.
I/$\overline{\text{M}}$	4	I	Intel/Motorola. When MULT = 1 this pin selects either Intel or Motorola 6805 bus.

DEMULTIPLEXED MICROPROCESSOR BUS INTERFACE (MULT = 0)

NAME	PIN	TYPE	FUNCTION
A0/A5	3-8	I	Address Bus. To transfer addresses from µP to ST5451.
D0/D7	17-24	I/O	Data Bus. To transfer data between µP and ST5451.
R/$\overline{W}$	27	I	Read/Write. "1" indicates a read operation; "0" a write operation.
E	26	I	Enable. Read/write operations are synchronized with this signal; its falling edge marks the end of an operation.

MULTIPLEXED MICROPROCESSOR BUS INTERFACE (MULT = 1 I/$\overline{M}$ = 1)

NAME	PIN	TYPE	FUNCTION
AD0/AD7	17-24	I/O	Address Data Bus. To transfer addresses and data between µP and ST5451.
$\overline{WR}$	27	I	Write. This signal indicates a write operation.
$\overline{RD}$	26	I	Read. This signal indicates a read operation.
ALE	3	I	Falling edge latches the address from the external A/D Bus.

MULTIPLEXED MICROPROCESSOR BUS INTERFACE (MULT = 1; I/$\overline{M}$ = 0)

NAME	PIN	TYPE	FUNCTION
AD0/AD7	17-24	I/O	Address Data Bus. To transfer addresses and data between µP and ST5451.
R/$\overline{W}$	27	I	Read/Write. "1" Indicates a write operation; "0" a write operation.
DS	26	I	Data Strobe. Read/Write operations are synchronized with this signal: its falling edge marks the end of an operation.
AS	3	I	Address Strobe. Falling edge latches the address from the external A/D Bus.

DMA (direct memory access): only when MULT = 1

NAME	PIN	TYPE	FUNCTION
$\overline{\text{DMA REQ X}}$ $\overline{\text{DMA REQ R}}$	7 5	O O	Direct Memory Access Requests: these outputs are asserted by the device to request an exchange of byte from the memory.
$\overline{\text{DMA ACK X}}$ $\overline{\text{DMA ACK R}}$	8 6	I I	Direct Memory Access Acknowledge: these inputs are asserted by the DMA controller to signal to the HDLC controller that a byte is being transferred in response to a previous transfer request.

GCI INTERFACE

NAME	PIN	TYPE	FUNCTION
D_{OUT}	15	I/O	Data output for B and D channels. In GCI mode it outputs B1, B2, M and C/I channels. In TE mode (GCI-SCIT) it can invert to input data for M' and C/I' channels (See Table 2).
D_{IN}	12	I/O	Data input for B and D channels. In GCI mode it inputs B1, B2, M and C/I channels. In TE mode (GCI-SCIT) it can invert to output data for M' and C/I' channels (See Table 2).
C_{LK}	11	I	Data Clock. It determines the data shift rate for GCI channels on the module interface.
FS	13	I	Frame synchronization. This signal is a 8 kHz signal for frame synchronization. The front edge gives the time reference of the first bit in the frame.
DEN	10	I	Data Enable. In TE mode, this pin is a normally low input pulsing high to indicate the active bit times for D channel transmit at DOUT pin. It is intended to be gated with CLK to control the shifting of data from HDLC controller to S interface device.

NON GCI INTERFACE

NAME	PIN	TYPE	FUNCTION
D_{OUT}	15	O	Data output. Digital output for serial data. Three modes: - HDLC Protocol multiplexed link - HDLC Protocol non multiplexed link - Non HDLC protocol (transparent Mode).
D_{IN}	12	I	Data input. Digital input for serial data. Three modes (See D_{OUT}).
C_{LK}	11	I	Data Clock. It determines the data shift rate. Two modes: Single or double bit rate.
FS	13	I	Frame synchronization. Used in mode HDCL protocol multiplexed link. Don't care in other modes. The rising edge gives the time reference of the first bit of the frame.
DEN	10	I	Data Enable. When high, enable the data transfer. on D_{OUT}

OTHERS

NAME	PIN	TYPE	FUNCTION
V_{DD}	28	I	Positive power supply = 5V $\pm$5%
V_{SS}	14	I	Signal ground
R_{ST}	16	I	Reset
ST	9	I	Special Test. (Reserved) must be tied to V_{SS}

2 - FUNCTIONS

2 - 1 - Basic HDLC Functions

2 - 1 - 1 - In Receive Direction:

- Channel selection
  In GCI channel B1 or B2 or D may be selected. B1 or B2 may be selected without M and C/I channels
- Flag detection
  A zero followed by six consecutive ones and another zero is recognized as a flag
- Zero delete
  A zero, after five consecutive ones within an HDLC frame, is deleted
- CRC checking
  The CRC field is checked according to the generator polynomial

$$X^{16} + X^{12} + X^5 + 1$$

- Check for abort
  Seven or more consecutive ones are interpreted as an abort flag
- Check for idle
  Fifteen or more consecutive ones are interpreted as "idle"
- Minimum lenght checking
  HDLC frames with less than n bytes between start and end flag are ignored: allowed values are $3 \leq n \leq 6$.

This value is set by a programmable register

- Address Field recognition
  4 SAPI and/or 3 TEI may be recognized. Several programmable registers indicate the recognized address types.

2 - 1 - 2 - In Transmit Direction:

- Shift control in TE mode
  D channel data are signalled by DEN pin.
- Flag generation
  A flag is generated at the beginning and at the end of every frame.
- Zero insert
  A zero is inserted after five consecutive ones within an HDLC frame
- CRC generation
  The CRC field of the transmitted frame is generated according to the generator polynomial

$$X^{16} + X^{12} + X^5 + 1$$

- Abort sequence generation
  An HDLC frame may be terminated with an abort sequence under microprocessor control
- Interframe time fill
  Flags or idle (consecutive ones) may be transmitted during the interframe time. A programmable bit selects the mode.

2 - 2 - FIFO Structure

2 - 2 - 1 - Receive FIFO Structure

In receive direction, a 64 byte FIFO memory is used. It is divided in 8 blocks of 8 bytes automatically chained.

In case of a frame length of 64 bytes or less, the whole frame can be stored in the FIFO. After the first 32 bytes have been received µP is interrupted and may read the available data.

In case of frames longer than 64 bytes, the µP is interrupted to read out the FIFO by 32 byte block.

In case of several short frames, up to eight may be stored inside the FIFO. After an interrupt, one frame is available for the µP. The eventual other seven frames are queued and transferred one by one.

2 - 2 - 2 - Transmit FIFO Structure

In transmit direction, a 64 byte FIFO memory is used, structured in 2 blocks of 32 bytes. ST5451 is requested to transmit after 32 bytes have been written into the FIFO.

If a transmission request does not include a message end, the HDLC controller will request the next data block by an interrupt.

2 - 3 - Microprocessor Interface

Three types of microprocessor interfaces are available (MULT and I/$\overline{M}$ control pins set the desired interface).

- Motorola non multiplexed families.
- Motorola multiplexed family (6805 type)
- Intel family.

You can connect ST5451 to a Direct Memory Access Controller as MC68440 or MC6450 (dual or quad channels).

A programmable register indicates DMA Interface enabling.

TABLE 1 - ST5451 Internal Registers

Address Hexa	Read	Write
00	Receive FIFO	Transmit FIFO
1F	-	-
20	ISTA0	ISTA0
21	ISTA1	ISTA1
22	ISTA2	ISTA2
23	STAR	CMDR
24	MODE	MODE
25	RFBC	TSR
26	CA	CA
27	CB	CB
28	CC	CC
29	CD	CD
2A	CE	CE
2B	CF	CF
2C	CIR1	CIX1
2D	CIR2	CIX2
2E	MONR1	MONX1/0
2F	-	MONX1/1
30	MONR2	MONX2/0
31	-	MONX2/1
32	-	MASK0
33	-	MASK1
34	-	MASK2
3E	CCR	CCR

TABLE 2 - CHANNEL ASSIGNMENT SELECT

CF REGISTER								C/I		M		8KB/s		16KB/s		56KB/s		64KB/s		C/I'		M'		CI"	
TE	MAS /SSC	CCS	CMS /SC	PI	VZ DOUT	MSD1	MSD0	RX	TX	RX	TX	RX	TX	DR	DX	RX	TX	RX	TX	RX	TX	RX	TX	TX	
X	X	X	X	X	X	X	0	RX ON DIN TX ON DOUT																	CONTINUOUS MODE
X	X	0	0	X	X	0	1							DIN	DOUT										MULTIPLEXED NON GCI MODE
X	0	0	1	X	X	0	1					DIN (1)	DOUT (1)												
X	1	0	1	X	X	0	1					DIN (2)	DOUT (2)												
X	X	1	0	X	X	0	1											DIN	DOUT						
X	0	1	1	X	X	0	1					DIN (3)	DOUT (3)												
X	1	1	1	X	X	0	1									DIN (4)	DOUT (4)								
1	1	0	0	0	0/1	1	1	DIN	DOUT	DIN	DOUT			DIN	DOUT										TERMINAL GCI MODE (D MASTER)
1	1	0	1	0	0/1	1	1	DIN	DOUT (6)	DIN	DOUT			DIN	DOUT (6)									DOUT (6)	
1	1	0	0	1	0/1	1	1	DIN	DOUT	DIN	DOUT			DIN	DOUT					DOUT (5)	DIN (5)	DOUT (5)	DIN (5)		
1	1	0	1	1	0/1	1	1	DIN	DOUT (6)	DIN	DOUT			DIN	DOUT (6)					DOUT (5)	DIN (5)	DOUT (5)	DIN (5)	DOUT (6)	
1	0	0	0	0	0/1	1	1	DIN	DOUT					DIN	DOUT										TERMINAL GCI MODE (D SLAVE)
1	0	0	1	0	0/1	1	1	DIN	DOUT (6)					DIN	DOUT (6)									DOUT (6)	
1	0	0	0	1	0/1	1	1	DIN	DOUT					DIN	DOUT					DIN	DOUT	DIN	DOUT		
1	0	0	1	1	0/1	1	1	DIN	DOUT (6)					DIN	DOUT (6)					DIN	DOUT	DIN	DOUT	DOUT (6)	
1	X	1	0	0	0/1	1	1	DIN	DOUT									DIN	DOUT						TERMINAL GCI MODE (B1 or B2)
1	0	1	1	0	0/1	1	1	DIN	DOUT			DIN (3)	DOUT (3)												
1	1	1	1	0	0/1	1	1	DIN	DOUT							DIN (4)	DOUT (4)								
1	X	1	0	1	0/1	1	1	DIN	DOUT									DIN	DOUT	DIN	DOUT	DIN	DOUT		
1	0	1	1	1	0/1	1	1	DIN	DOUT			DIN (3)	DOUT (3)							DIN	DOUT	DIN	DOUT		
1	1	1	1	1	0/1	1	1	DIN	DOUT							DIN (4)	DOUT (4)			DIN	DOUT	DIN	DOUT		
0	X	0	X	X	0/1	1	1	DIN	DOUT	DIN	DOUT			DIN	DOUT										REGULAR GCI MODE

(1) FIRST BIT OF 16KB/S CHANNEL SELECTED
(2) SECOND BIT OF THE 16KB/S CHANNEL SELECTED
(3) LAST BIT OF THE 64KB/S CHANNEL SELECTED
(4) SEVEN FIRST BITS OF THE 64KB/S CHANNEL SELECTED
(5) TO INSURE THE EXCHANGING OF MESSAGES WITH THE OTHERS ST5451 PERIPHERAL DEVICES THE MASTER DEVICE USES THE C/I' AND M' CHANNELS ON DIN PIN FOR THE OUTPUT SERIAL DATA DOUT PIN FOR THE INPUT SERIAL DATA
(6) ONLY THROUGH THE ACCESS PROCEDURE

THIS TABLE SHOWS THE USED CHANNELS ACCORDING TO THE CONFIGURATION OF THE CF REGISTER AND THE PINS USED (DIN, DOUT) WHERE THE RECEIVERS RX AND THE TRANSMITTERS TX GET OR PUT THE DATA

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3 - REGISTER DESCRIPTION

For all the register pictures MSB is on the left and LSB on the right
If not otherwise stated bit are considered active at 1.

FIFOS

RFIFO (read), XFIFO (write).

The address range of the two FIFOs are identical. All the 32 addresses give access to the "current" FIFO location.

When the closing Flag of a receive frame is detected, a status byte is available in the RFIFO. This byte has the following format:

RBC	RDO	CRC	RAB	0	0	0	0

RBC Receive Byte Count.
The length of the received frame is n time 8 bits (n=3,4,5,...)

RDO Receive Data Overflow
A part of the frame has not been lost because the receive FIFO was full

CRC CRC Check
The received CRC bytes were not correct

RAB Receive Abort
The received frame was not aborted

A status byte equal to D0H indicates a correctly received frame

ISTA0 Interrupt Status Register 0
After RESET 10H

RME	RPF	RFO	XPR	XDU	EXI2	EXI1	0

RME Receive Message End
One complete frame of length less than or equal to 32 bytes, or the last part of a frame of length greater than 32 bytes is stored in the RFIFO.

RPF Receive Pool Full
32 bytes of a frame are in RFIFO. The frame is not yet completely received.

RFO Receive Frame Overflow
A complete frame was lost because no storage space was available in the RFIFO.

XPR Transmit Pool Ready
One data block (32 bytes max) may be entered into the XFIFO.

XDU Transmit Data Underrun
A transmitted frame was terminated with an abort sequence because no data were available for transmission in XFIFO and no XME command was issued. It is not possible to transmit frame when that interrupt remains unacknowledged and XRES has not been set.

EXI2 Extended Interrupt 2
The interrupt reason is indicated in register ISTA2

EXI1 Extented Interrupt1
The interrupt reason is indicated in register ISTA1.

ISTA1 Interrupt Status Register 1
After RESET 01H
(GCI mode only)

0	0	CIC1	EOM1	XAB1	RMR1	RAB1	XMR1

CIC1 Comman/Indicate Change
A change in the value of CIR1 is detected

EOM1 End of Message 1 (monitor channel)
MON1 has received an end of message.

XAB1 Monitor Transmit ABORT
The received byte has not been detected in two successive frames.
MON1 has sent an ABORT (A bit) to the remote transmitter.

RMR1 Receive Monitor Register 1 ready
A byte has been received in register MONR1.

RAB1 Receive Abort
MON1 received an ABORT from the remote receiver.

XMR1 Transmit Monitor Register 1 ready
A byte can be stored in register MONX1

ISTA2 Interrupt Status Register 2
After RESET 01H
(GCI and TE mode only)

0	0	CIC2	EOM2	XAB2	RMR2	RAB2	XMR2

CIC2 Command/Indicate Change
A change in the value of CIR2 is detected.

EOM2 End of Message 2 (monitor channel)
MON2 has received an end of message.

XAB2 Monitor Transmit ABORT
The received byte has not been detected in two successive frames.
MON2 has sent an ABORT (A bit) to the remote transmitter.

RMR2 Receive Monitor Register 2 ready
A byte has been received in register MONR2.

RAB2 Receive ABORT
MON2 received an ABORT from the remote receiver.

XMR2 Transmit Monitor Register 2 ready
A byte can be stored in register MONX2.

MASK0, MASK1, MASK2
After Reset FF; the three mask registers MASK0, MASK1, MASK2 are associated respectively to the three interrupt registers ISTA0, ISTA1,and ISTA2.
Each interrupt source in ISTA registers can be selectively masked by setting to ”1” the corresponding bit in MASK1. Interrupt sources (masked or not) are indicated when ISTA is read by the microprocessor. When an interrupt source is not masked, $\overline{INT}$ goes low.

STAR Status Register
After Reset 48H

XDOV	XFW	IDLE	RLA	DCIO	0	0	0

XDOV Transmit Data Overflow
More than 32 bytes have been written into the XFIFO.

XFW XFIFO Write enable
Data can be entered into the XFIFO.

IDLE IDLE State
15 or more consecutive ones have been detected on the input data line.

RLA Receive Line Active
Frames or interframe flags are being received

DCIO D and C/I Channels are occupied

CMDR Command Register
After Reset 00

XHF	XME	RMC	RMD	RHR	XRES	M2RES	M1RES

XHF HDLC frame transmission can start.

XME Transmit Message End
The last part of the frame was entered in XFIFO and can be sent.

RMC Receive Message Complete
Reaction to RPF or RME interrupt. The received frame (or one pool of data) has been read and the corresponding RFIFO is free.

RMD Receive Message Delete
Reaction to RPF or RME interrupt. The entire frame will be ignored. The part of frame already stored is deleted.

RHR Reset HDLC receiver

XRES Reset HDLC transmitter
XFIFO is cleared and the transmitted frame (if any) is aborted.

M2RES Monitor 2 Reset
Reset MONITOR and C/I channels (TX and RX).

M1RES Monitor 1 Reset
Reset MONITOR and C/I channels (TX and RX).

* For the four first bits (XHF, XME, RMC, RMD), the reset is done by the device; the other bits level sensitive

MODE HDLC Mode Register
After Reset 00

DMA	FL1	FL0	ITF	RAC	CAC	NHF	FLA

DMA DMA Interface activation

FL1/0 Frame Length
Minimum frame length accepted

	FL1	FL0
3 bytes	0	0
4 bytes	0	1
5 bytes	1	0
6 bytes	1	1

ITF InterframeTime Fill
ITF= 1 : Flags are transmitted
ITF= 0 : IDLE is transmitted

RAC RAC= 1 : Activate RX
RAC= 0 : deactivate RX

CAC Channel Activation
CAC = 1 : Activate RX and TX
CAC = 0 : deactivate RX and TX

NHF HDLC Function Select
NHF = 1 : disable HDLC function

FLA Flag
FLA = 1 : transmit shared flags
FLA = 0 : transmit two flags between consecutive frames.

RFBC Receive Frame Byte Counter
After reset 00

RDC7	RDC6	RDC5	RDC4	RDC3	RDC2	RDC1	RDC0

RDC 0/7 Receive Data Count

Total number of bytes of received frame without CRC.

RDC 0/4 Indicate the number of bytes in the current block available in RFIFO.

RDC 5/7 Indicate the number of 32 bytes blocks received. If the frame exceeds 223 bytes, RDC 5/7 hold the value ”111”, only RDC 4/0 continue to count modulo 32.

See Table 3.
The contents of the register are valid after an RME interrupt. The µP must read N+1 bytes to transfer the number of bytes received and the status byte into the memory.

CIX1 Command/Indicate Transmit Register 1
After reset FFH
(GCI only)

1	1	1	1	C1	C2	C3	C4

C1, C2, C3, C4:

Code to be transmitted permanently in the outgoing GCI C/I channel.

CIR1 Command/Indicate Receive Register 1
After reset FFH
(GCI only)

1	1	1	1	C1	C2	C3	C4

C1, C2, C3, C4:

Incoming GCI C/I channel.

MONX1 Monitor Transmit Register 1
After reset FFH
(GCI only)

M1	M2	M3	M4	M5	M6	M7	M8

The value written in MONX1 is transmitted in the outgoing Monitor channel according to GCI transfer protocol. XMR1 interrupt indicates when MONX1 is again available.

MONR1 Monitor Receive Register 1
After reset FFH
(GCI only)

M1	M2	M3	M4	M5	M6	M7	M8

The value read from MONR1 gives the value of the byte received in the monitor channel according to GCI transfer protocol. RMR1 interrupt indicates when a new byte is available in MONR1 register.

CIX2 Command/Indicate Transmit Register 2
After Reset FFH
(GCI and TE mode only)

1	1	P1	P2	P3	P4	P5	P6

P1/P6 Code transmitted permanently in the 2nd GCI C/I channel.

CIR2 Command/Indicate Receive Register 2
After reset FFH
(GCI and TE mode selected only)

1	1	P1	P2	P3	P4	P5	P6

P1/P6 The contents of the 2nd C/I channel; they are the different requests received from TE peripheral devices to µP.
Six peripherals can make a simultaneous request.

MONX2 Monitor Transmit Register 2
After reset FFH
(GCI and TE mode only)
The value written in MONX2 is transmitted in the 2nd GCI M channel to a peripheral (if PI= 1; register CF).

TABLE 3

N (number of bytes in the frame received without CRC)	Counter 7 6 5	4 3 2 1 0	n (number of 32 bytes blocks received)
N	**n**	**m**	**n**
1 Min	000	00001	0
2	000	00010	0
3	000	00011	0
30	000	11110	0
31	000	11111	0
32	001	00000	1
33	001	00001	1
62	001	11110	1
63	001	11111	1
64	010	00000	2
222	110	11110	6
223	110	11111	6
224	111	11111	7
256	111	00000	7
257	111	00001	7
-	111	-	7

MONR2 Monitor Receive Register 2
After reset FFH
(GCI and TE mode only)
The value read from MONR2 gives the value of the byte received from M channel in 2nd GCI channel.

TSR Time Slot Register
After reset 00

TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0

In GCI mode (MDS1= 1 in CF Register)
a) CCS=1 in CF Reg. (64 Kbit/s)
Then: TSR2 indicates B1 or B2
TSR4/7 indicate position of GCI channel
b) CCS=0 in CF Reg. (16 Kbit/s)
Then: TSR4/7 indicate position of GCI and its D channel

In Multiplexed Mode (MDS1=0 in CF Register)
a) CCS=1 in CF Reg. (64 Kbit/s)
Then: TSR2/7 indicate channel position in the 64 time slots multiplex
b) CCS=0 in CF Reg. (16 Kbit/s)
Then: TSR0/7 indicate channel position in the 256 time slots multiplex.

CA Configurationn Register A
After reset 00

CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0

CA0	SAPI 0 is recognized	CA0 = 1
CA1	SAPI 63	CA1 = 1
CA2	SAPI x	CA2 = 1
CA3	SAPI y	CA3 = 1
CA4	TEI 127	CA4 = 1
CA5	TEI z	CA5 = 1
CA6	TEI t	CA6 = 1
CA7	Address filter active	CA7 = 1

CB Configuration register B
After reset 00
Content of CB indicate SAPI x value
High Order 6 Bits

SAPI	0	0

CC Configuration Register C
After reset 00
Content of CC indicate SAPI y value
High Order 6 Bits

SAPI	0	0

CD Configuration Register D
After reset 00
Content of CD indicate TEI z value.

7 High Order Bits

TEI	0

CE Configuration Register E
After reset 00
Content of CE indicate TEI t value.

7 High Order Bits

TEI	0

CF Configuration Register F
After 00

TE	MAS/SSC	CCS	CMS/SC	PI	VZDOUT	MDS1	MDS0

TE TE mode
TE = 1 : the frame is constitued by three GCI channels (GCI-SCIT)

MAS/SSC If CCS = 0, TE = 1, MDS0 and MDS1 = 1 (i.e. GCI mode, TE mode, 16 Kbit/s)
MAS/SSc is MAS and:
MAS = 0 means "Slave device"
MAS = 1 means "Master device"

If SC = 1 (i.e. a sub-channel is selected) MAS/SSC is SSC; if 16Kb is selected SSC chooses between first on second bit of the stream while, if 64Kb is selected SSC chooses between first or last seven bits of the stream (see TABLE 2 and CMS/SC)

CCS Channel Capacity Selection
CCS = 1: 64 Kb/s
CCS = 0: 16 Kb/s.

CMS/SC If CCS = 0, TE = 1, MDS0 and MDS1 = 1 (i.e. GCI mode, TE mode, 16Kbit/s)
CMS/SC is CMS (Contention mode selection) and:
CMS = 1 means "D and C/I channel access procedure active"
CMS = 0 means "D and C/Z channel access procedure active"

If CCS = 1 and TE = 1 CMS/SC is SC (Subchannel) and:
SC = 0 means "16Kbit/s or 64Kbit/s is used"
SC = 1 means "an 8Kbit/s or 56Kbit/s subchannel inside a 16Kbit/s or 64kbit/s is used" (see MAS/SSC)

PI Peripheral Interface (only if TE=1)
PI = 1: CIX2, CIR2, MONX2, MONR2, active

VZDOUT When level 1 device is inactive (i.e. CIR1 = DI = 1111) and GCI has to be waken up (i.e. TIM = 0000 in CIX1), DOUT is set to zero requiring FS and CLK if VZ DOUT=1.

MDS1 Mode Bit 1
MDS1 = 1:GCI mode
MDS1 = 0: Multiplexed mode

MDS0 Mode Bit 0
MDS0 = 1: Multiplexer and Demultiplexer are active.
MDS=0 No multiplexer.

CCR Configuration Register 00
After reset 00

TLP	ADDR	AD3	AD2	AD1	AD0	CRS	TRI

TLP Test Loop
TLP = 1: The transmitter is internally connected to the receiver; the transmit output is not activated. The digital interface must be activated to provide the bit clock and frame Synchro.

ADDR Address Recognized
If TE = 1 and PI = 1
ADDR = 1: The first byte received in MONR2 is compared with AD0/3. If equal the message is accepted, otherwise is ignored.
ADDR = 0: The message is always accepted.

AD0/3 When PI = 1, is the component address.

AD0/2 Address bit used to access D and C/I channels (TE = CMS =1, CCS = 0).

CRS Clock Rate Selection
CRS = 1: Clock frequency is twice the data rate (GCI).
CRS = 0: Clock frequency and data rate are identical.

TRI Tristate
TRI = 1: DOUT in tristate
TRI = 0: DOUT in open drain.

4 - WORKING PROCEDURES

4 - 1 - RECEIVE FRAME

Recognized frame (by means of SAPI and/or TEI identification), having a minimum length is stored in the RFIFO with all bytes between the opening flag and CRC field.

When the frame is less than or equal to 32 bytes, is transferred in one block, and just after the receiving completion interrupt (RME), a status byte is appended at the end. The frame and its status byte remain stored until µP acknowledgement (RMC).

When the frame is longer than 32 bytes, blocks of 32 bytes plus one remainder block of lenght 1 to 32 are transferred to the microprocessor. The receiving 32 byte block generates a RPF interrupt and the data in RFIFO remains valid until µP acknowledgement (RMC).

The µP can ignore a received frame by meaning RMD (Receive Memory Delete), reaction to RPF or RME. The part of frame already stored is deleted and the remainder frame is ignored by the HDLC Controller.

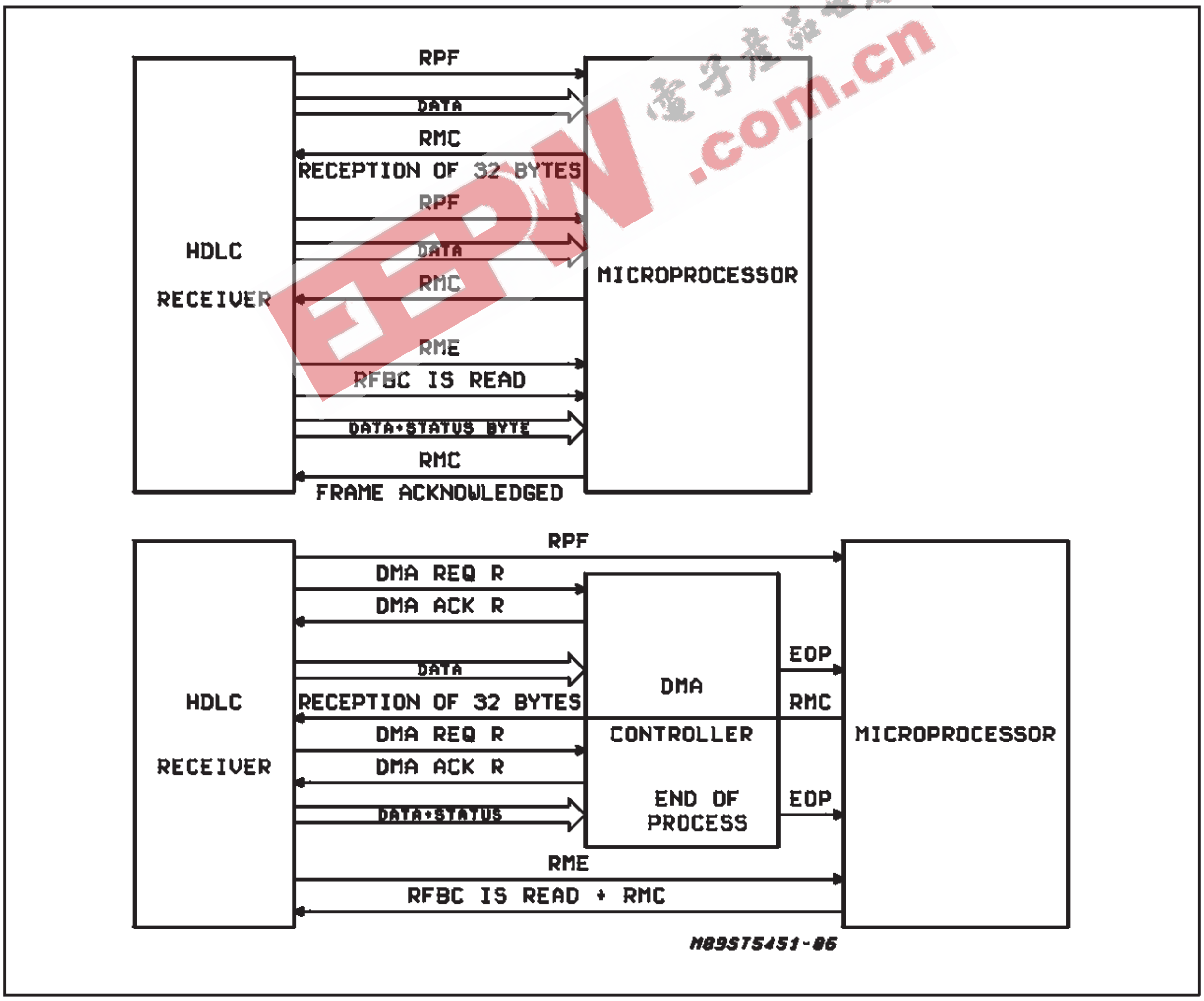
The last block of the frame generates the RME interrupt.

RFBC register bits 0 to 4 indicate the number of bytes currently stored in the RFIFO. Bits 5 to 7 indicate the total number of 32 byte blocks already received. Bits 5 to 7 do not overflow. When the counter status 7 has been reached, it indicates a frame length greater than 223 bytes (see Table 3).

RFBC register is valid only after the RME interrupt and remains valid until RMC acknowledgement by µP.
At each read access by the µP, RFBC 5/7 bits remain unchanged, RFBC 0/4 bits are decreased to reach value 0 when the whole block is read.

Interrupts are queued inside the device. They are sent one by one to the microprocessor after each acknowledgement RMC. If a frame is lost because the RFIFO was full, a RFO interrupt is generated.

Figure 1: Receiving of an HDCL frame



4- 2 - TRANSMIT FRAME

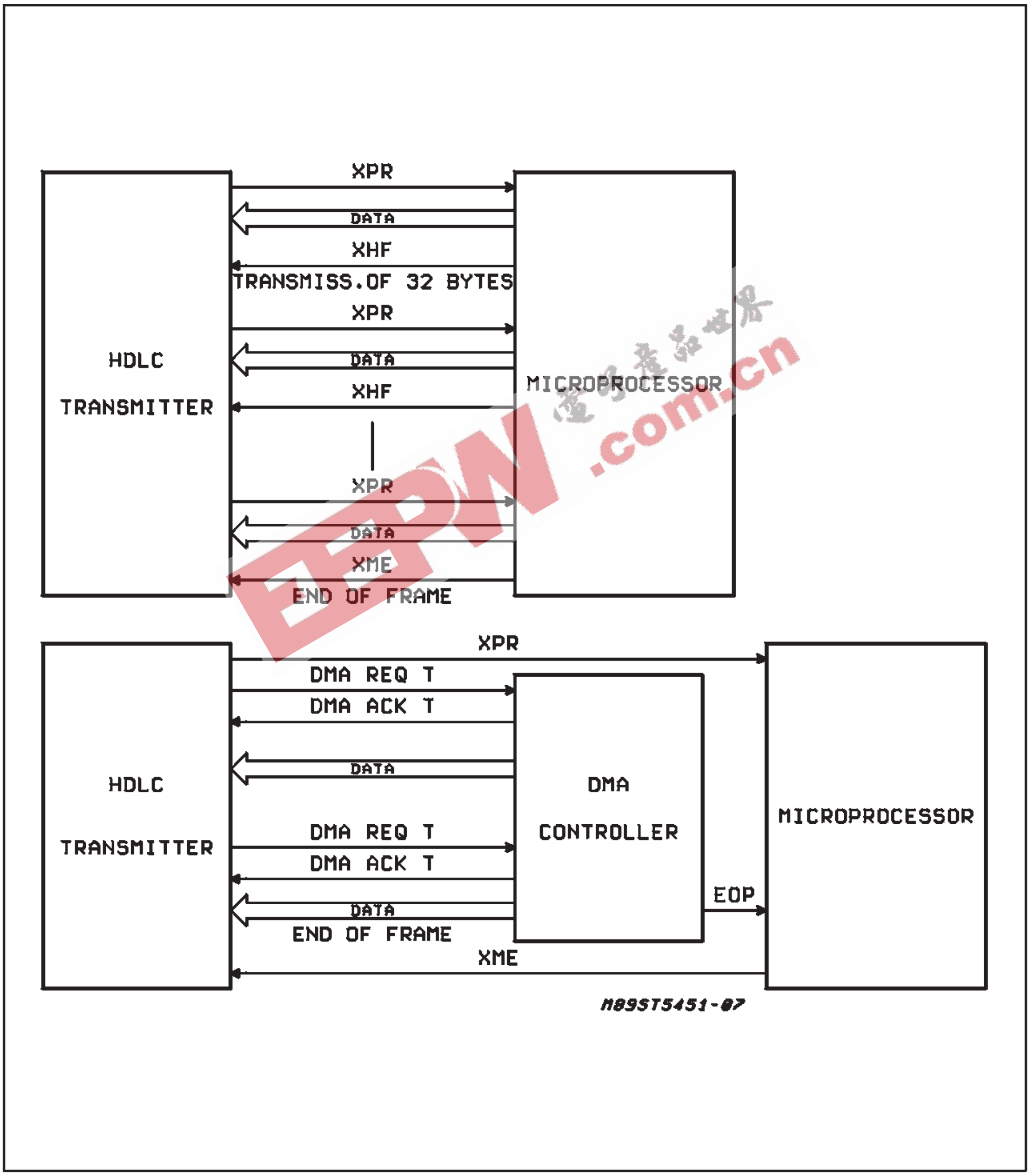
After polling bit XFW or after a XPR interrupt, up to 32 bytes may be stored in XFIFO. Transmission begins after that XHF command is issued by µP. ST5451 will request another data block by an XPR interrupt if the XFIFO contains less than 32 bytes.

When XME is set, all remaining XFIFO bytes are transmitted, the CRC field and the closing flag are added. The HDLC controller then generates a new XPR interrupt.

If the XFIFO becomes empty while XME command has not been set, an abort sequence is generated, followed by interframe time fill and XDU interrupt is generated.

A frame may be aborted by XRES command as well.

Figure 2: Transmission of an HDCL frame



4 - 3 - COMMAND/INDICATE PROCEDURE

The exchange of information in the C/I channel runs as follows:
The two circuits (i.e. ST5421 and ST5451) connected on the GCI interface send one each other a permanent four bit command code in C/I field.

RECEIVE C/I

The ST5451 stores on every frame the four bits of C/I channel coming from level 1 circuit in a first register CIR. This value is compared with the previous one. If a one new appears during two consecutive frames, this new value is loaded in register CIR1 and a CIC1 interrupt is generated.

TRANSMIT C/I

The transmit register CIX1 can be written at any time by the µP. Its content is continuously sent in the C/I channel.

Note: The TIM command (0000) forces a low level on DOUT, if CIR1 = DI (1111) when VZ DOUT = 1 to require FS and CLK.

4 - 4 - MONITOR CHANNEL

The GCI Monitor channel procedure allows full duplex data transmission with acknowledgement using A bit.

MESSAGE RECEIVING

An interrupt (bit RMR1 in ISTA1 register) is generated when a new byte is available in register MONR1.
ST5451 generates an interrupt bit (XAB1 in ISTA1) if it does not read twice the same bytes meanwhile sending an ABORT to the remote transmitter.
It performs an interrupt (EOM in ISTA1) also when it has received an End Of Message. Acknowledgement to remote transmitter is sent if:
- the byte was received twice with the same value
- the microprocessor reads the previous byte stored in register MONR1.
This procedure performs flow control between S interface device and µP.

MESSAGE TRANSMISSION

ST5451generates an interrupt (XMR1 in ISTA1) when register MONX1 is available.
Writing register MONX1/0 generates a message transmission. When the last byte is stored in the register MONX1/1, ST5451 sends the End of Message to remote receiver. If an Abort is received, one interrupt (RAB1) is generated.

4 - 5 - M' and C/I' CHANNELS

The procedure allows a full duplex data transmission between microprocessor and the peripheral devices connected on C/I' local and M' channel through GCI-SCIT channel 1.
Receive Interrupt on C/I' (DOUT is an input).
A new value on C/I' indicates to ST5451 master that one device in the terminal wants to send a message. Up to six peripherals may generate such an interrupt to the microprocessor.
ST5451 writes at every frame the six bits of C/I' channel coming from peripherals in register CIR'.
This value is compared with the previous one and if a new one appears during two consecutive frames, is loaded in register CIR2 and CIC2 interrupt (ISTA2 register) is generated.
µP may send a message on M' channel (DIN becomes an output) to allow the peripheral device to transmit.

MESSAGE TRANSMISSION ON M' CHANNEL

ST5451 sets interrupt XMR2 (ISTA2 register) if register MONX2/0 is available. Writing MONX2/0 generates a message transmission. When the last byte is stored in register MONX2/1, ST5451sends End of Message to remote peripheral.
If an ABORT is received, interrupt RAB2 (ISTA2 register) is issued. Then microprocessor may send its message again.

MESSAGE RECEPTION ON M' CHANNEL

Interrupt bit RMR2 (ISTA2 register) is generated when a new byte is available in MONR2 register.
ST5451 sets interrupt bit XAB2 (ISTA2 register) if it does not read twice the same byte; in this case, it sends an ABORT to remote peripheral.
The controller generates interrupt bit EOM2 (ISTA2 register) when End Of Message is received.

4 - 6 - ACCESS PROCEDURE TO D AND C/I CHANNELS (GCI and TE mode selected only)

Up to eight HDLC controllers may be connected to D channel and C/I channel. A contention resolution mechanism is used if bit CMS (Contention Mode Selection) is set.
The mechanism allows to give an access without losing data.
An access request may be generated, if CIX1 (Command/Indicate Register 1) contains a different code from DI (1111). During the procedure, M channel (with A and E bits) may be used. On input DIN, the GCI controller checks the CMS4 bit (CMS channel - Third GCI channel) (see Fig. 4).
CMS4 indicates the status of C/I and D channels CMS4= 1 "channels free"; CMS4= 0 channels occupied.
If the channels are free, the HDLC controller starts transmitting its individual address AD2 on CMS1, AD1 on CMS2, AD0 on CMS3. If an erroneous address is detected, the procedure is terminated immediately. If the complete address can be read without error, the D and C/I channels are occupied: the ST5451 transmits CMS4 = 0: The HDLC controller which has the lowest address has priority over the others.
The access request is withdrawn if the HDLC controller transmits code DI = 1111. the CMS4 bit (CMS field) is set.

Figure 3: GCI-SCIT Frame Timing

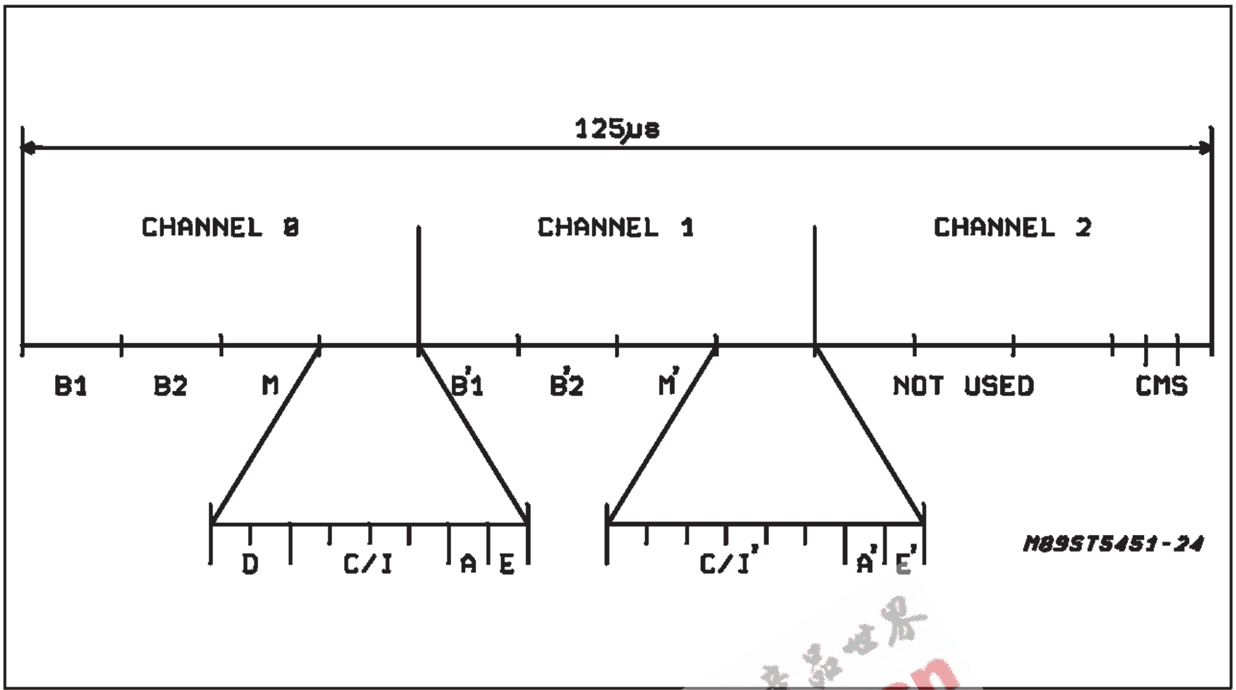
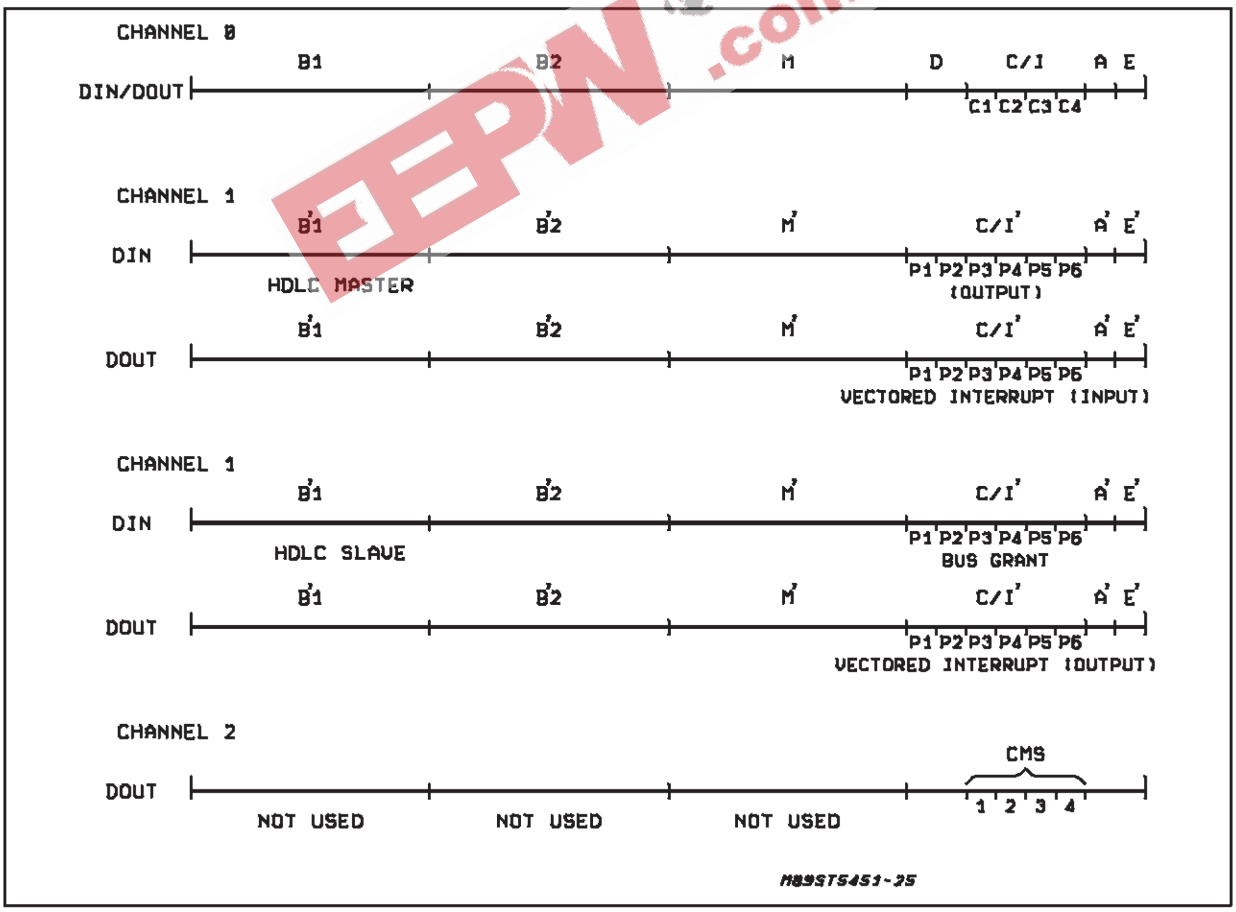


Figure 4: GCI-SCIT Channels Timing



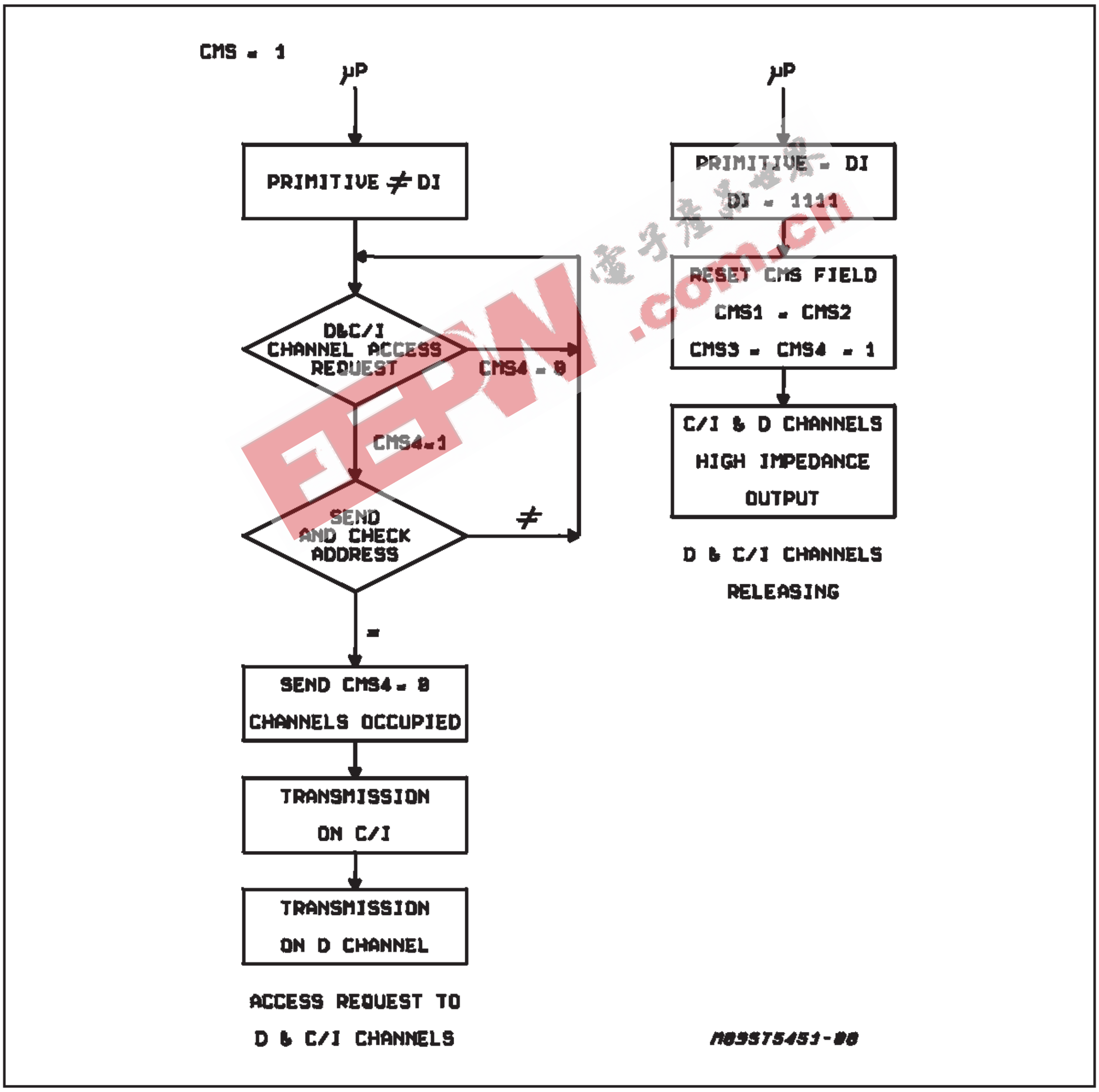
4 - 7 - DMA ACCESS

The HDLC controller has a DMA interface which is activated by DMA bit in MODE register.The DMA interface is available only when multiplexed bus is selected.
ST 5451 asserts DMA REQR or DMA REQX to request an exchange of bytes between the FIFOS and the external memory.
The external DMA controller asserts DMA ACKR or DMA ACKX to access the FIFOS.
These signals are equivalent to E/DS/RD functions.
During DMA access, CS/CE pin must be inactive; AS and E/DS/RD signals can be present.
Outside DMA Access, all registers are accessible by the µP except the FIFOS.

FRAME RECEPTION:
When one block has been stored in RFIFO, DMA REQ R pin goes low and RPF (or RME) interrupts the µP. The DMA controller reads the RFIFO. After the RME interrupt, the frame length will be available in RFBC register. The block is acknowledged by RMC command.

FRAME TRANSMISSION:
When a 32 byte block is free in XFIFO, DMA request goes low and XPR interrupts the µP. The DMA controller can write data in the XFIFO. At the end of the frame, the µP send XME to HDLC controller; CRC and closing flag will be sent by the HDLC controller.

Figure 5: D and C/I channels Access Procedure



4 - 8 - INTERRUPT PROCEDURE

4 - 8 - 1 - HDLC CHANNELS

4 - 8 - 1 - 1 - RECEIVE DIRECTION

RRE and RPF interrupts

RPF bit (register ISTA0) set high to indicate the HDLC controller has received a block of 32 bytes which is not a complete message.

This bit remains high until it is erased by the microprocessor.

As for each bit of ISTA0 register, except the extension bits of ISTA1 and ISTA2 (EXI1, EXI2), the way to erase RPF is to write a ”0” at its location and to write a ”1” at the location of the others (for example 7FH into ISTA0 to erase RME). The processing order is:
- put Mask0 on ISTA0 (if Mask Off)
- (Read FIFOR) X 32
- Write ISTA0 to erase RPF (BFH)
- Write RMC to ”1” for asking for another block of the frame
  (NB: RMC, RMD are automatically erased by the controller)
- Remove Mask0

RME bit (register ISTA0) set high to indicate the HDLC controller has received a short frame or the last block of a large frame. The message is now complete, the bit remains high until it is erased by the microprocessor. The processing order is:
- put Mask0 on ISTA0 (if upper level Mask Off)
- Read RFBC with a mask on the 3 most significant bits, to know the number ”N” of transfers to do
- (Read FIFOR) x N for data
- Read FIFOR for status on the frame
- Write ISTA0 to erase RME (7FH)
- Write RMC or RMD to ”1” for asking for another frame.

RF0 interrupts

RF0 is a bit of the interrupt register ISTA0 set high to indicate an overflow of the receive FIFO has been detected, either because more than 8 frames cannot be stored or because more than 64 bytes can’t be stored. This information is also stored into the status of the concerned frame (RDO).

The processing order of the microprocessor is:
- Looking for RPF and RME bits and pop - up the frames. Then look for the status and throw down the frame concerned. In general case, only one frame is lost.

4 - 8 - 1 - 2 - TRANSMIT DIRECTION

XPR Interrupt

XPR is a bit of the interrupt register ISTA0 coming high to indicate HDLC controller has a free block of 32 bytes. This bit remains high until the microprocessor write a byte into the block and erase this bit into ISTA0; if another block is free, XPR get high again immediately.

The processing order of the microprocessor is in non DMA Mode:
- Put Mask0 on ISTA0 (if upper level Mask Off)
- Write at least one byte into FIFOX
- Write ISTA0 to erase XPR
- Write XHF to ”1” for launching the transmit operation of block (a block is not necessarily 32 bytes)
  or write XME to ”1” for launching the transmit of a short frame or of the last part of a frame
- Remove masks

In DMA Mode two general cases are possible:

1) The external DMA controller works by ”pages” less or equal to 32 bytes. The ”process” of the DMAC is a short frame transmission and the processor must give an XME at the end of the DMAC process (refer to figure 2).

2) The DMA controller works by ”pages” of more than 32 bytes. It’s process is the transfer of the whole frame.
The circuit doesn’t need an XHF at the end of an intermediate 32 byte block; since it has reached 32 bytes written into the current fifo, it begins the transfer and toggles on the second fifo as soon as the first is full. (At this moment an XME is possible if the 32nd byte was the end of the frame - case 1) and then, a 33rd write operation into the fifo generates an internal XHF and the frame following blocks are expected.
- In the two cases the flow control is done between DMAC and ST5451 by the way of REQX and ACKX signals

The processing order is:
- Put Mask0
- Give order to DMAC to begin transfer
- Wait for DMAC end of process
- Write ISTA to erase on XPR
- Write XME to signal the end of the frame to the ST5451 (otherwise the ST5451 will put ”underrun” interrupt, as soon as its two blocks are free).

XDU Interrupt

XDU is a bit of the interrupt register ISTA0 coming high to indicate HDLC controller has detected an underrun (a frame is being transmitted and no more bytes are available into the FIFO).

The HDLC controller finish the frame by transmitting an ”Abort” and no more data can be transmitted even in NHF mode. To be sure XDU is seen by the MIcroprocessor, XDU interrupt bit must be erased in ISTA0 in addition of XRES security procedure

The transmit control is frozen and the only way to reinitialize a transmit session is to write an XRES, after erasing XDU.

4 - 8 - 2 - M CHANNELS INTERRUPTS EOM, RMR, XMR, RAB

Receive Direction

RMR 1/2 is a bit of interrupt register ISTA 1/2 coming high to indicate the M (or M') channel controller has received a valid byte on receiving channel (two identical consecutive bytes).

The microprocessor processing order is;

1. Erasing RMR 1/2 interrupt into ISTA 1/2
2. Read MONR 1/2 register.

This order can't be inverted because, as long as MONR isn't read, the receive state machine is locked in wait state, a new byte can't be acknowledged and so, a new interrupt can't be done.

More, if MONR is read first, the receive state machine is ready for receiving a new byte and create another interrupt. So, if the interrupt bit corresponding to the previous frame isn't erased before a new byte arrives, this byte won't be seen (the microprocessor won't be informed) and the controller will be locked waiting for MONR read.

XAB 1/2 is a bit of the interrupt register coming high to indicate the receive controller has detected an abort (two conscutive bytes not identical) as long as this interrupt isn't erased, the receiver is locked in wait state.

EOM 1/2 is a bit of the interrupt register coming high to indicate the receive controller has detected an end of message. As long as the interrupt isn't erased, the receiver is locked in wait state.

Transmit Direction

XMR 1/2 is a bit of the interrupt register coming high to indicate a byte can be written into MONX. The processing order is:

1. Erasing XMR bit
2. Writing a new byte into MONX.

If this order is inverted, the new byte will be transmitted and a new XMR may be erased before being seen by the microprocessor.

RAB 1/2 is a bit of the interrupt register coming high to indicate the remote receiver has reported an abort detection. The processing order is:

1. Erasing RAB bit
2. Erasing XMR bit
3. Writing a new byte into MONX.

If a write operation of the new byte is done before the RAB erasing, the byte will be lost and the transmitter will stay waiting for it.

4 - 8 - 3 - CI CHANNEL INTERRUPTS

CIC 1/2 is a bit of ISTA 1/2 interrupt register coming high to indicate a valid byte has been detected by the command indicate receive controller, and readable into CIR 1/2 register. The processing order is:

1. Erasing CIC bit
2. Reading CIR register.

If this order is inverted, a next byte may be unseen by the microprocessor. It is recommended to work with "Ping Pong" protocol on CI channels, as non flow control is done.

4 - 9 - SOFTWARE RESET PROCEDURES

4 - 9 - 1 - XRES (Transmit Direction)

XRES is a level sensitive command of CMDR which initialize the transmit process.

- XPR interrupt bit is erased
- XDU interrupt bit is not erased (security procedure)
- All data in FIFOs are lost
- After an XRES, the microprocessor must wait for an XPR before writing new data.

The processing order is:

- Writing a "1" into XRES (CMDR)
- Writing a "0" into XRES (CMDR)
- Read ISTA0 waiting XPR or enable XPR interrupt

4 - 9 - 2 - RHR (Receive Direction)

RHR is a level sensitive command of CMDR, which reinitialize the receive process.

- RME, RPF bits are erased
- RFO bit is erased
- All frames in FIFO R are lost
- If RHR is released (got down) at the time a frame is on line, the HDLC controller waits for a flag.

4 - 9 - 3 - M1RES, M2RES M/CI channels

MRES is a level sensitive command of CMDR which initialize the M/CI channel protocole in both directions.

XMR, RAB, RMR, CIC, XAB, EOM bits are erased by MRES.

After a clock programming (bit CRS), it's necessary to put MRES bit to initialize properly the M protocol.

TYPICAL APPLICATIONS

ST5451 HDLC controller may be used in TE, NT2, NT12 or LT.

Figures 6 to 8 illustrate three typical applications in multifunctional TE.

The D channel containing only signalling is processed by the LAPD controller and routed via a parallel µP interface to the terminal processor. The support of the LAPD protocol which is implemented by the HDLC controller device allows in cost senstive applications the use of a low cost microprocessor. See fig. 6.

Fig. 7 illustrates a configuration in which the D channel containing signalling data (SAPI s) as well as packet switched data (SAPI p) is processed by two controllers and two independent microprocessors.

Fig. 8 illustrates a configuration in which one microprocessor is connected to two controllers via a DMA controller.
D channel with LAPD signalling data and B channel LAPB packet data are processed by the same µP. A DMA controller performs device to memory transfers. It is a typical work station application.

Fig. 9 and 10 illustrate 2 typical applications in NT2 or exchange.

An NT2 or LT in fig.9 with eight D channel controllers connected to the GCI interface handle subscriber 0 to 7. Any GCI compatible transceiver (S or U) may be used to do the subscriber line interface; a GCI compatible exchange circuit may implement the system interface. This is one decentralized application.

Fig. 10 illustrates a centralized application. Using a switching net work, it is possible to connect:

up to thirty two 64 Kbit/s channels on a 2 Mb/s PCM highway to 32 B channel controllers

up to sixty four 64 Kbit/s channels on a 4 Mb/s PCM highway to 64 B channel controllers

up to two hundred fifty six D channels on a 4 Mb/s highway to 256 D channel controllers.

Figure 6: Low cost GCI terminal application

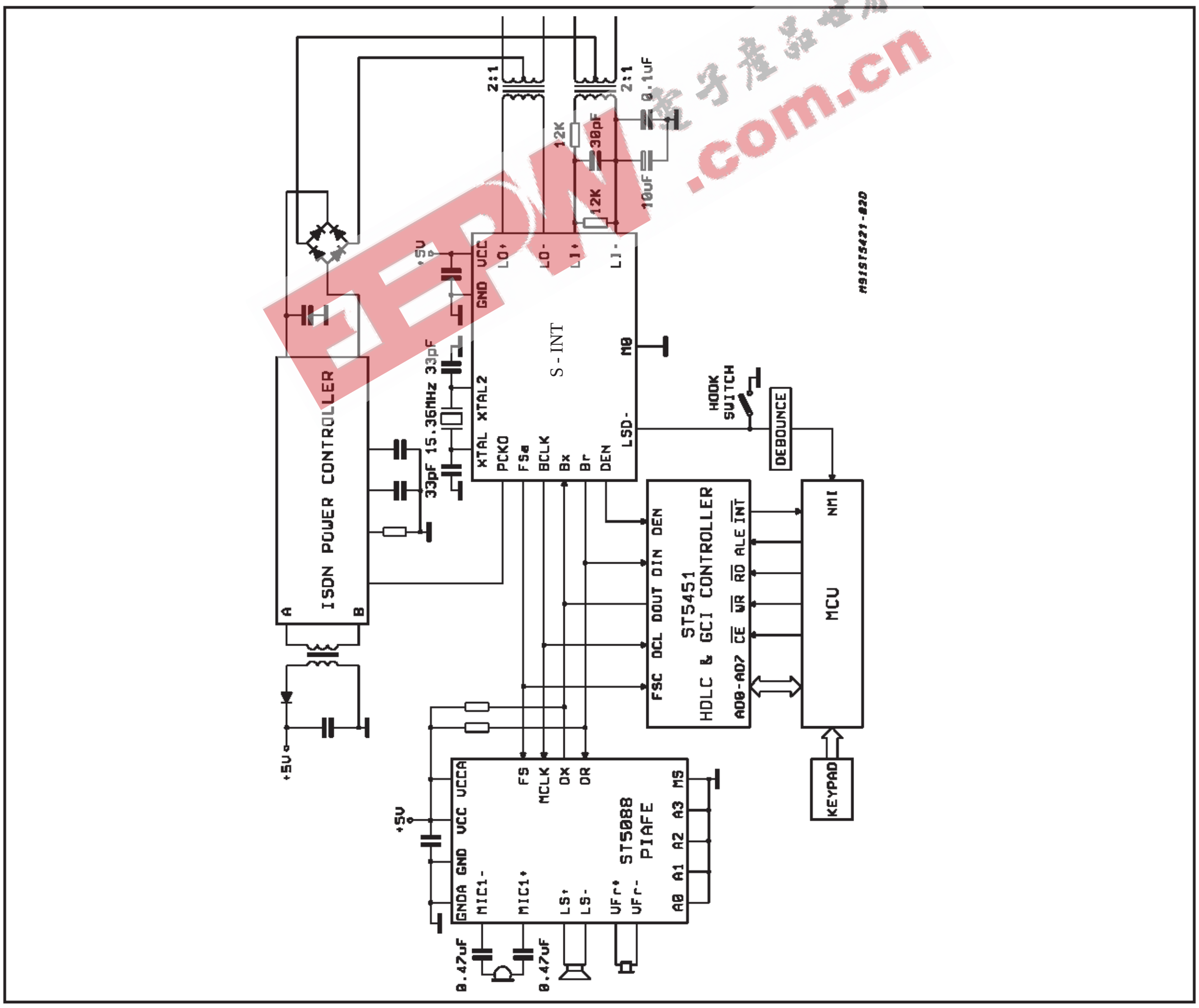


Figure 7: LAPB and LAPD protocol on the same D channel handlended with 2 different µPs

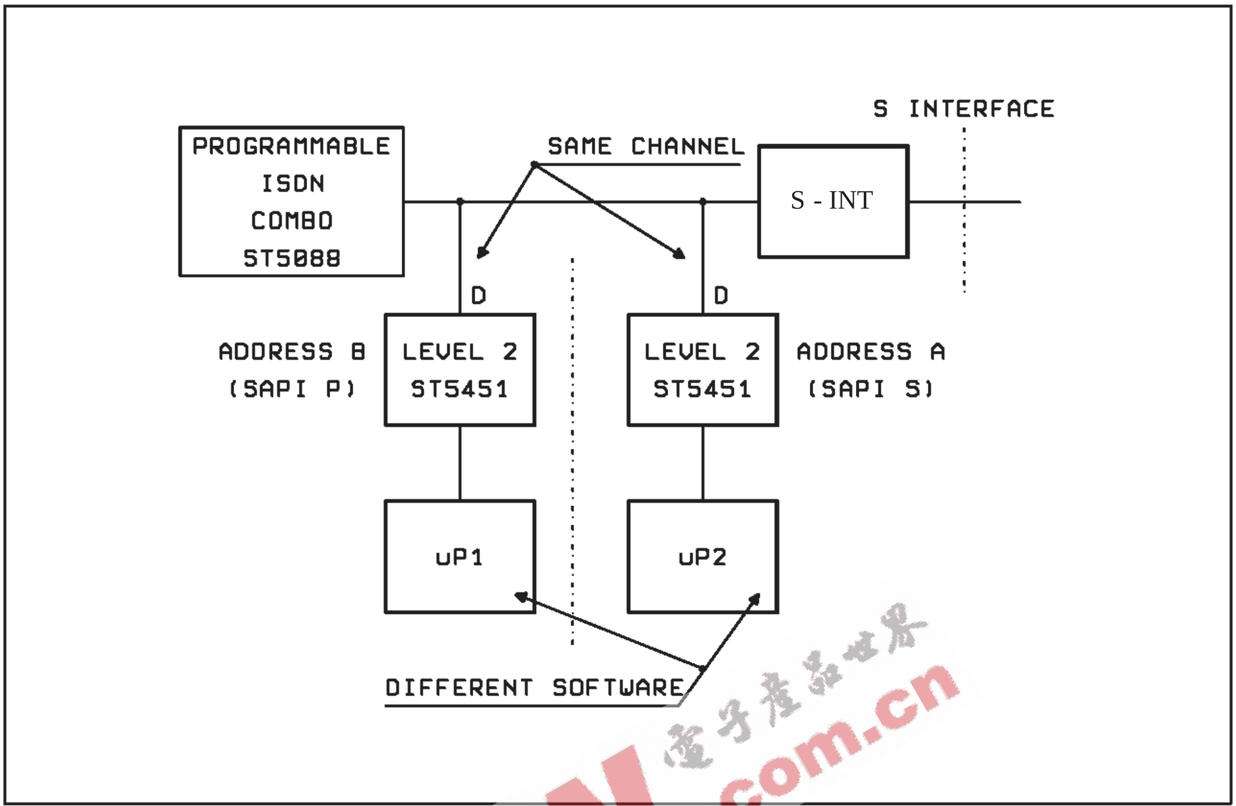


Figure 8: LAPB and LAPD protocol handling an B and D channel

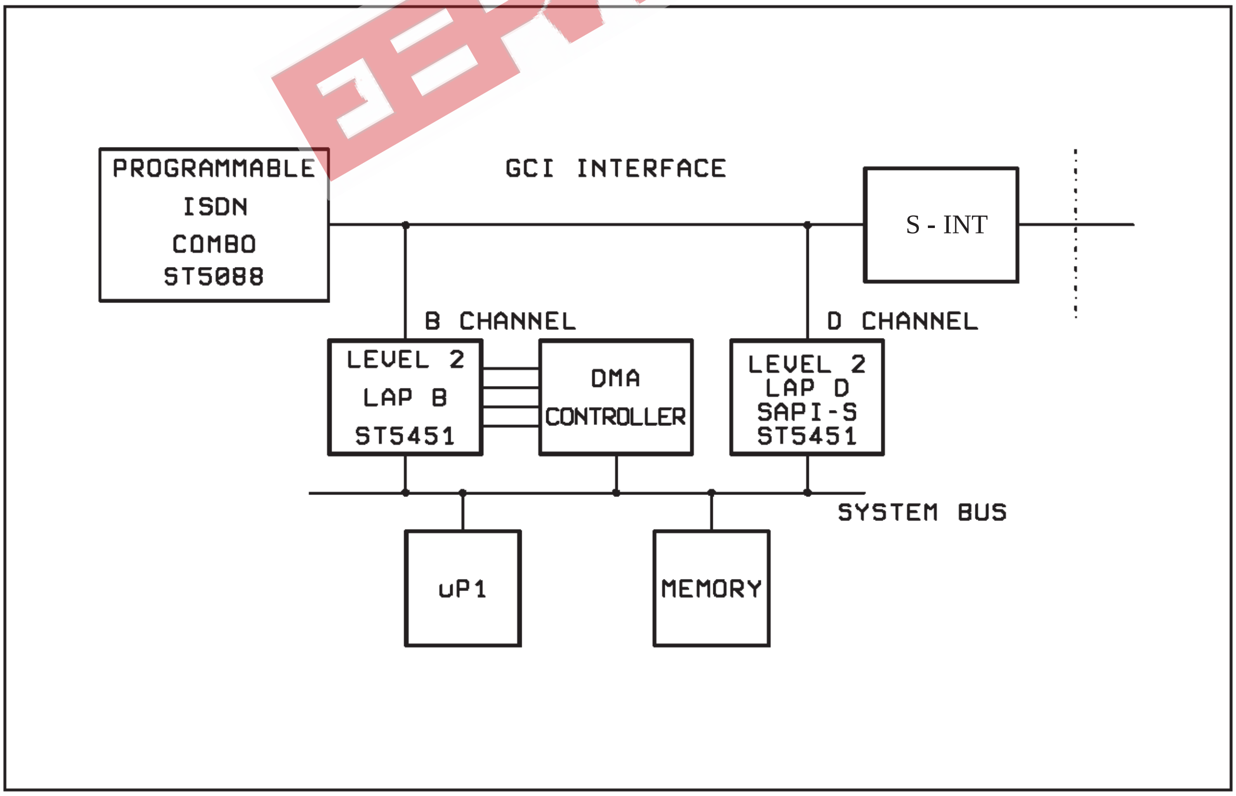


Figure 9: Decentralized D channel handling in NT2 or LT

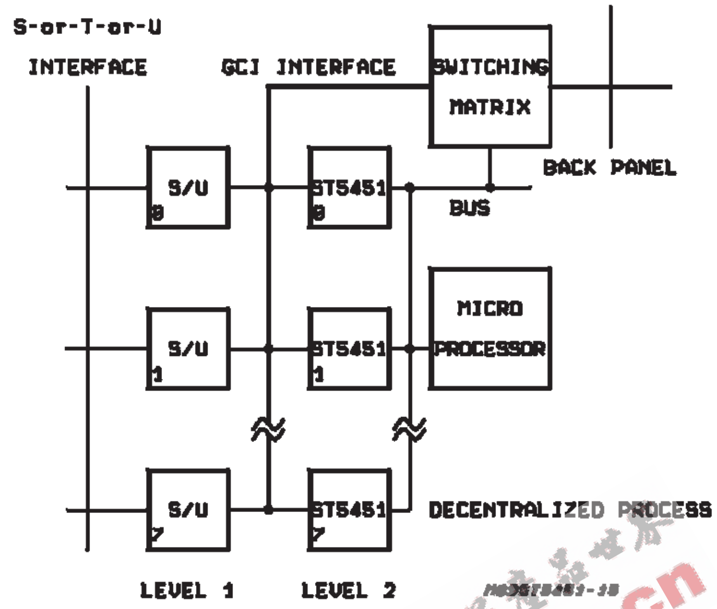


Figure 10: Centralized D channel handling in NT2 or LT

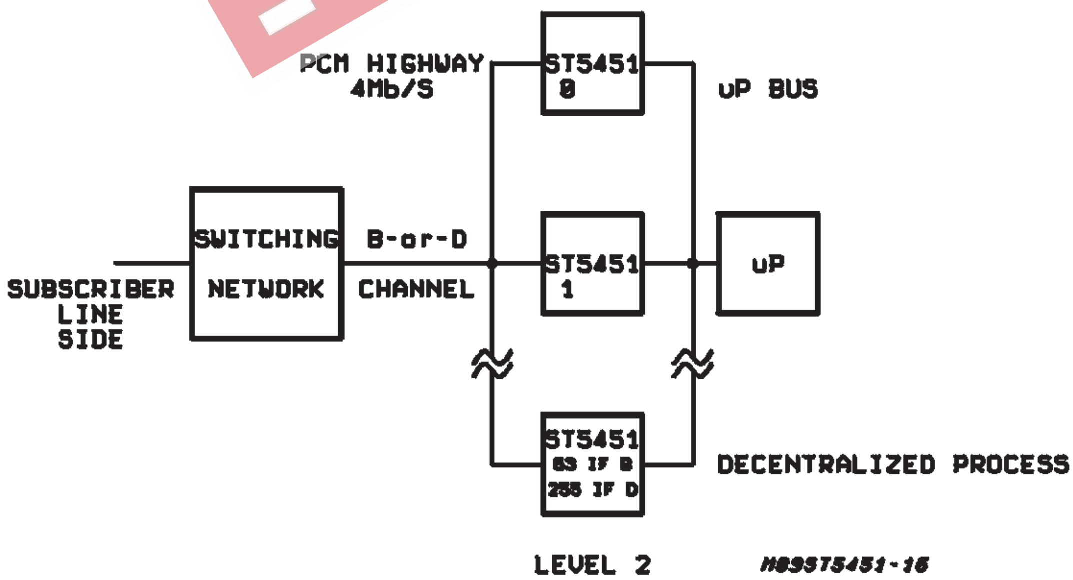


Figure 11: HDCL Frame Transmission Procedure

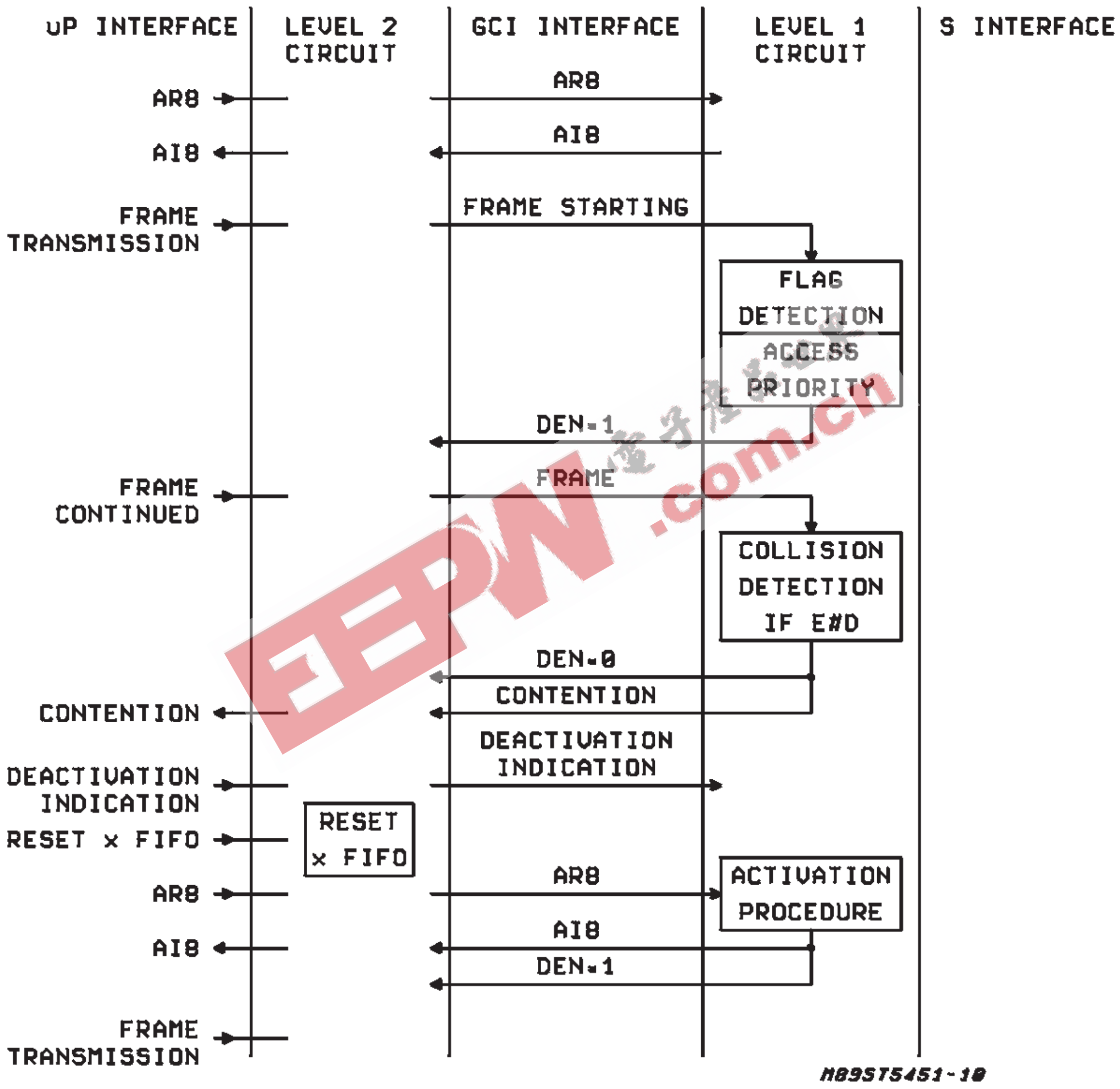


Figure 12: HDCL Frame Transmission Procedure in D Channel

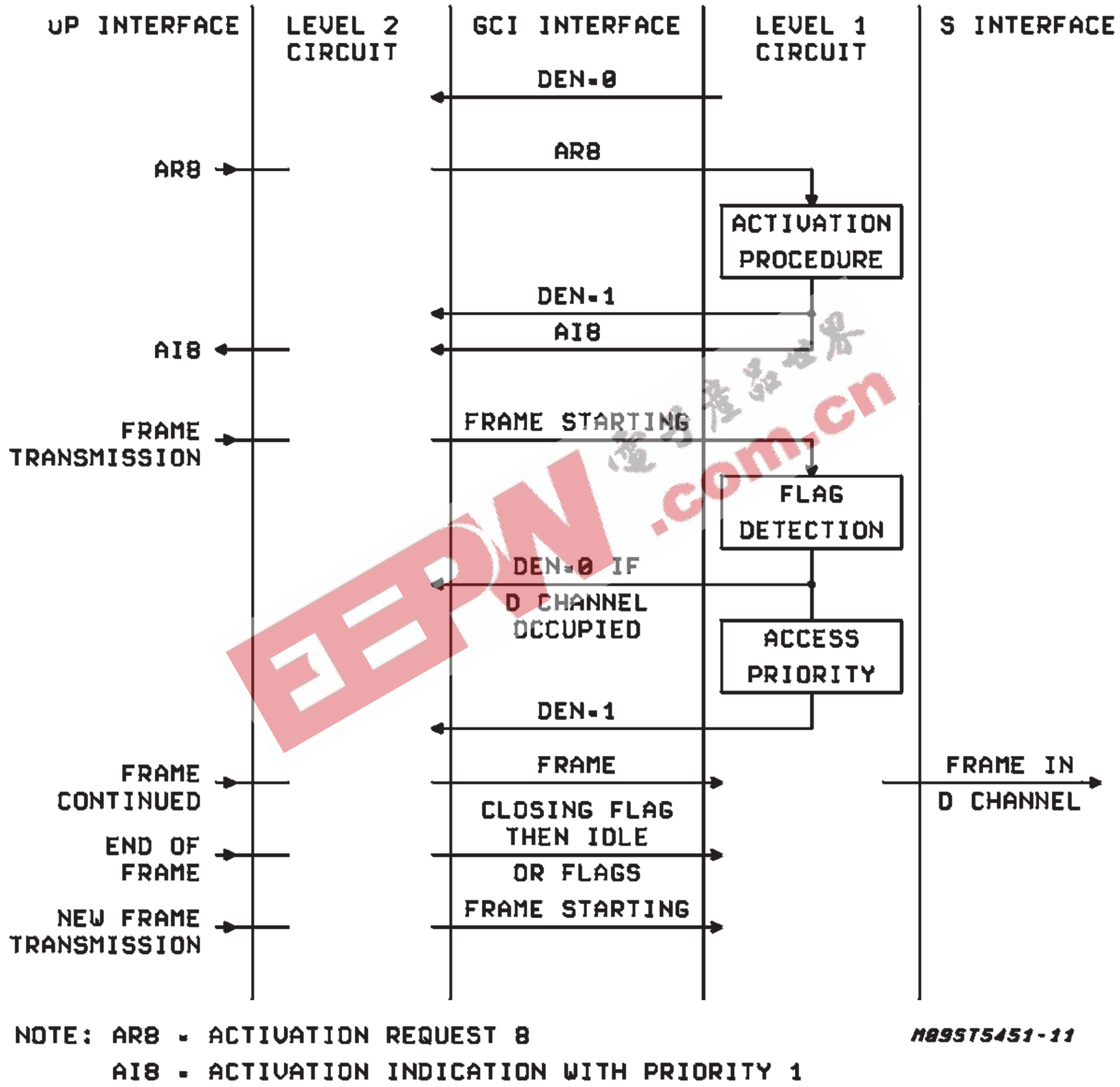
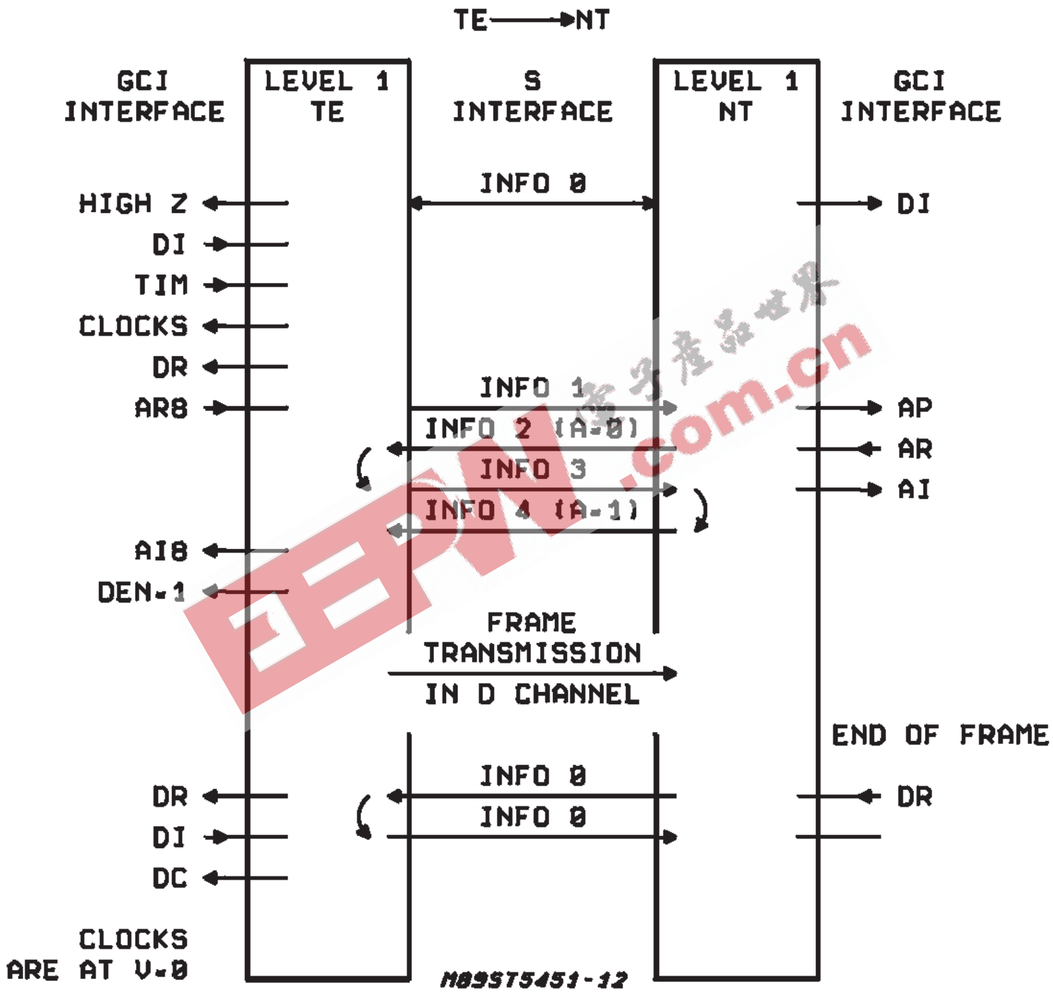


Figure 13: S Activation and Deactivation procedure



ELECTRICAL CHARACTERISTICS (T from 0 to 70°C, V_{DD} = 5 ± 0.25V).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_S	Supply Current	CLK Freq. = 4MHz CLK Freq. = 2MHz NO CLK Freq.	– – –	4 2 20	– 4 300	mA mA µA

STATIC CHARACTERISTICS - GCI INTERFACE (T from 0 to 70°C, V_{DD} = 5 ± 0.25V).

Symbol	Parameter	Condition	Min.	Max.	Unit
VIH	High Level Input Voltage	Maximum leakage current : ± 10 µA	2.4	VDD+0,4	V
VIL	Low Level Input Voltage	Maximum leakage current : ± 10 µA	VSS-0,4	0,8	V
VOH	High Level Output Voltage	IOH = -0,4 µA	2,4		V
VOL	Low Level Output Voltage	IOL = 2mA		0,45	V
VOL	Low Level Output Voltage D_{OUT} . D_{in} . INT	IOL = 7mA		0,45	V
C	Input/Output Capacity			10	pF
C_{OUT}	Load Capacity DIN/DOUT			150	pF
	Load Capacity $\overline{INT}$			150	pF
	Load Capacity AD0/7			100	pF

DYNAMIC ELECTRICAL CHARACTERISTICS - GCI Interface

Symbol	Parameter	Min.	Typ.	Max.	Unit
FSync	8 KHz		8		KHz
F_{CLK}	64 x n x FSync 1 ≤ n ≤ 8	512		4096	KHz
t_{WCH}	Period of CLK High	80			ns
t_{WCL}	Period of CLK Low	80			ns
t_{RC}	Rise Time of CLK			10	ns
t_{FC}	Full Time of CLK			10	ns
t_{HCF}	Hold Time: CLK - FS	0			ns
t_{SFC}	Set-up Time: FS - CLK	30			ns
t_{DCD}	Delay Time: CLK High to data valid. out: 150 pF			80	ns
t_{DCZ}	Delay Time: to Data Disabled	0		80	ns
t_{DFD}	Delay Time: FSync. High to data valid. count: 150 pF. Applies only if Sync rises later than CLK raising edge.			80	ns
t_{SDC}	Set-up Time: Data valid to CLK receive edge.	30			ns
t_{HDC}	Hold Time: CLK low to data invalid.	30			ns

DYNAMIC ELECTRICAL CHARACTERISTICS - Double Clock Interface

Symbol	Parameter	Min.	Typ.	Max.	Unit
FSync	8 KHz		8		KHz
F_{CLK}	16 x n x FSync $1 \leq n \leq 64$	128		8192	KHz
t_{WCH}	Period of CLK High	50			ns
t_{WCL}	Period of CLK Low	50			ns
t_{RC}	Rise Time of CLK			10	ns
t_{FC}	Full Time of CLK			10	ns
t_{HCF}	Hold Time: CLK - FS	0			ns
t_{SFC}	Set-up Time: FS - CLK	30			ns
t_{DCD}	Delay Time: CLK High to data valid. out: 150 pF			80	ns
t_{DCZ}	Delay Time: to Data Disabled	0		80	ns
t_{DFD}	Delay Time: FSync. High to data valid. count: 150 pF. Applies only if Sync rises later than CLK raising edge.			80	ns
t_{SDC}	Set-up Time: Data valid to CLK receive edge.	30			ns
t_{HDC}	Hold Time: CLK low to data invalid.	30			ns

ELECTRICAL CHARACTERISTICS - Single Clock Interface

Symbol	Parameter	Min.	Typ.	Max.	Unit
FSync	8 KHz		8		KHz
F_{CLK}	8 x n x FSync $1 \leq n \leq 64$	64		4096	KHz
t_{WCH}	Period of CLK High	80			ns
t_{WCL}	Period of CLK Low	80			ns
t_{RC}	Rise Time of CLK			10	ns
t_{FC}	Full Time of CLK			10	ns
t_{HCF}	Hold Time: CLK - FS	0			ns
t_{SFC}	Set-up Time: FS - CLK	100			ns
t_{DCD}	Delay Time: CLK High to data valid. out: 150 pF			80	ns
t_{DCZ}	Delay Time: to Data Disabled	0		80	ns
t_{DFD}	Delay Time: FSync. High to data valid. count: 150 pF. Applies only if Sync rises later than CLK raising edge.			80	ns
t_{SDC}	Set-up Time: Data valid to CLK receive edge.	30			ns
t_{HDC}	Hold Time: CLK low to data invalid.	30			ns

Figure 14: GCI Timing

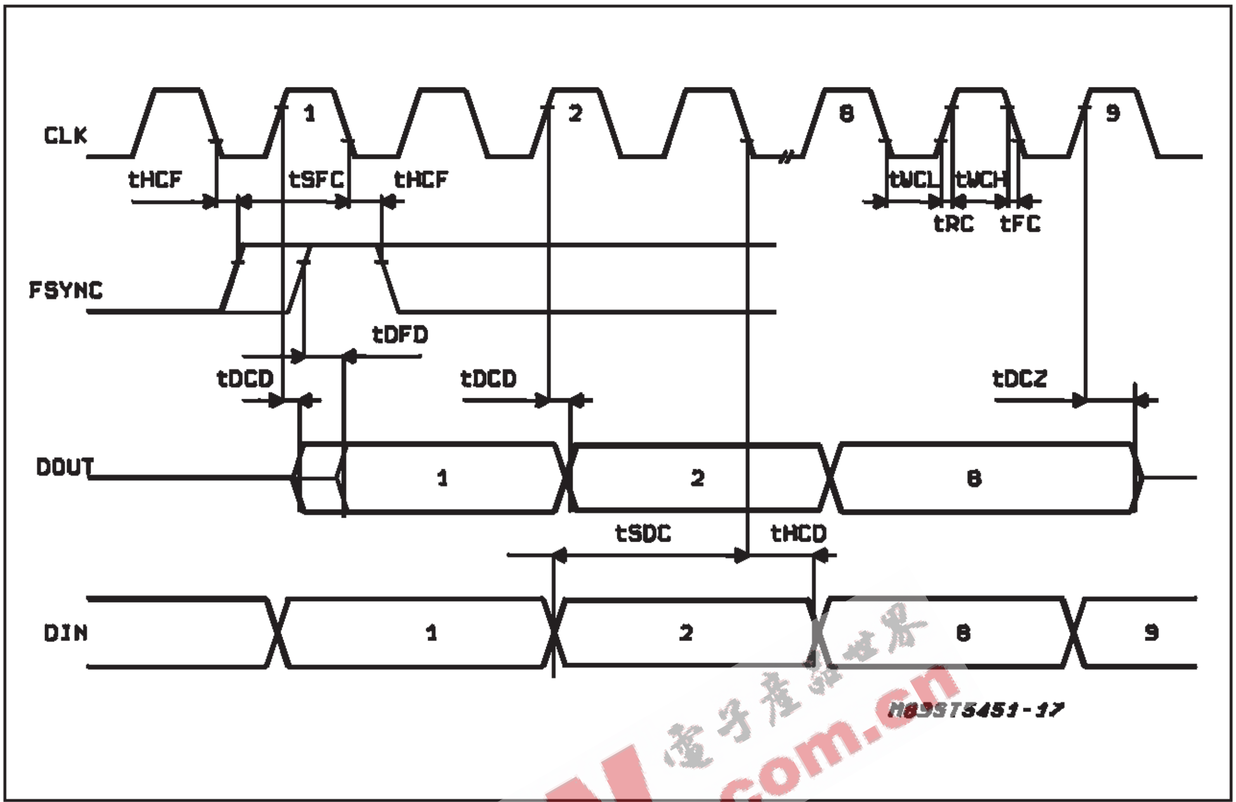


Figure 15: Single Clock Diagram

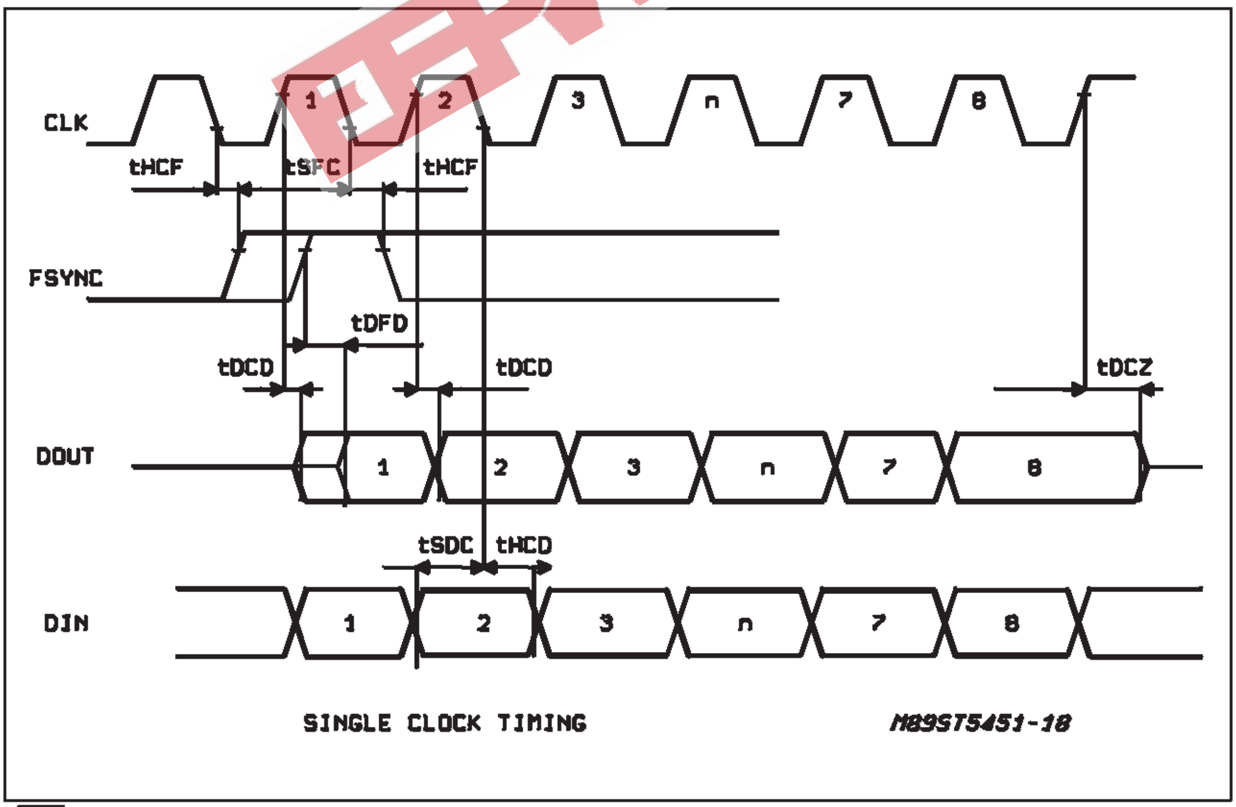
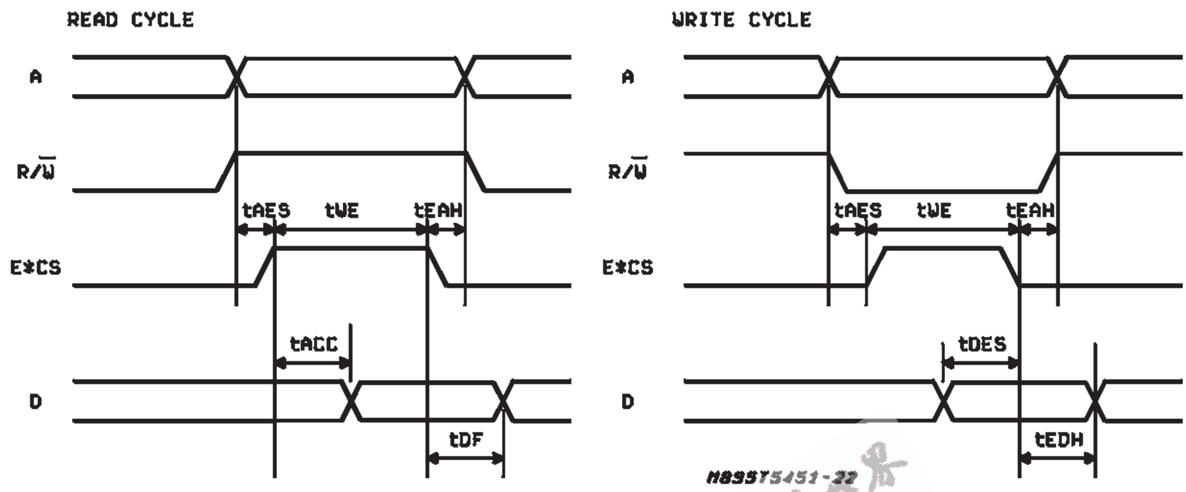


Figure 16: Non-multiplexed µP bus timing



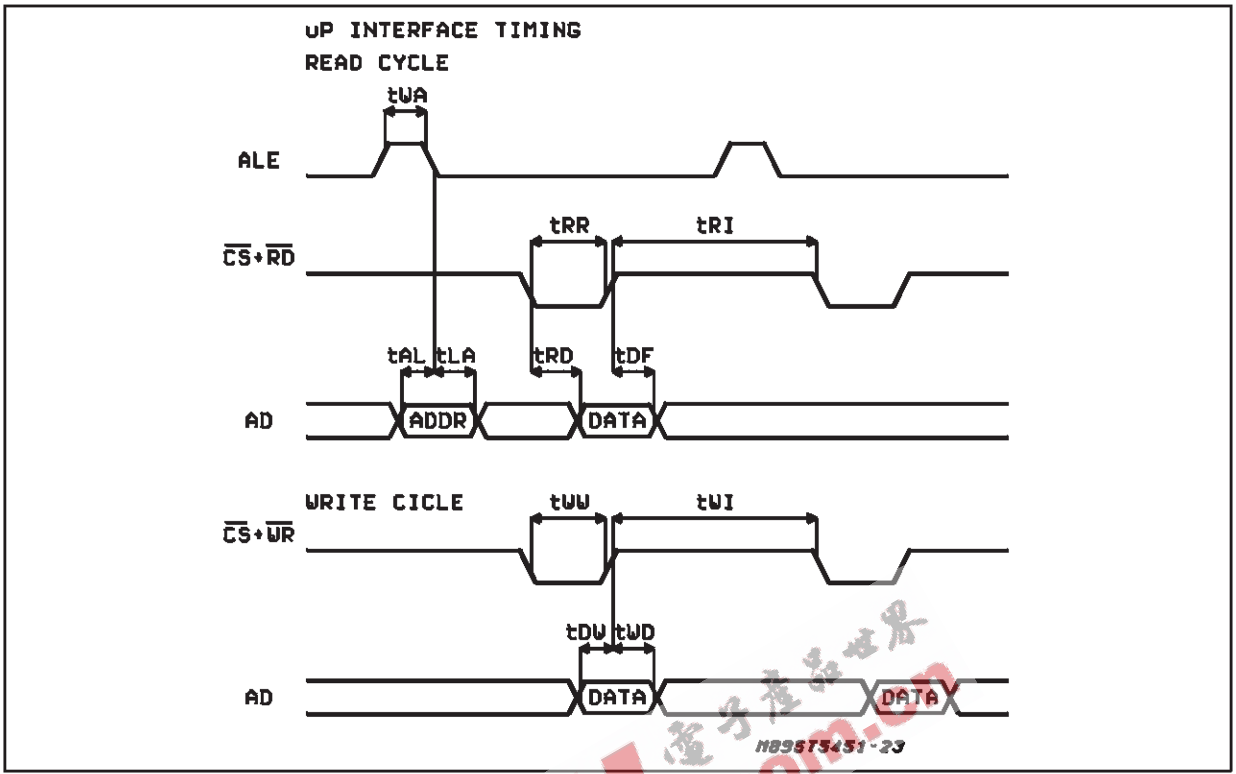
READ CYCLE (Non-multiplexed mode)

Symbol	Parameter	Min.	Max.	Unit
t_{EAH}	Address Hold After E	10		ns
t_{EAH}	R/$\overline{W}$ Hold After E	10		ns
t_{AES}	Address to E Setup	20		ns
t_{AES}	R/$\overline{W}$ to E. Setup	20		ns
t_{ACC}	Data Delay from E		110	ns
t_{DF}	Output Float Delay		25	ns
t_{WE}	Minimum Width of E	110		ns

WRITE CYCLE (Non-multiplexed mode)

Symbol	Parameter	Min.	Max.	Unit
t_{EAH}	Address Hold After	10		ns
t_{EAH}	R/$\overline{W}$ Hold After E	10		ns
t_{AES}	Address to E Setup	20		ns
t_{AES}	R/$\overline{W}$ to E.CS Setup	20		ns
t_{DES}	Data to End of E Setup	35		ns
t_{EDH}	End of E.CS to Data hold	10		ns
t_{WE}	Minimum Width of E	60		ns
t_{RW}	Minimum Width of RESET	100		ns

Figure 17: Multiplexed Intel-like µP bus timing



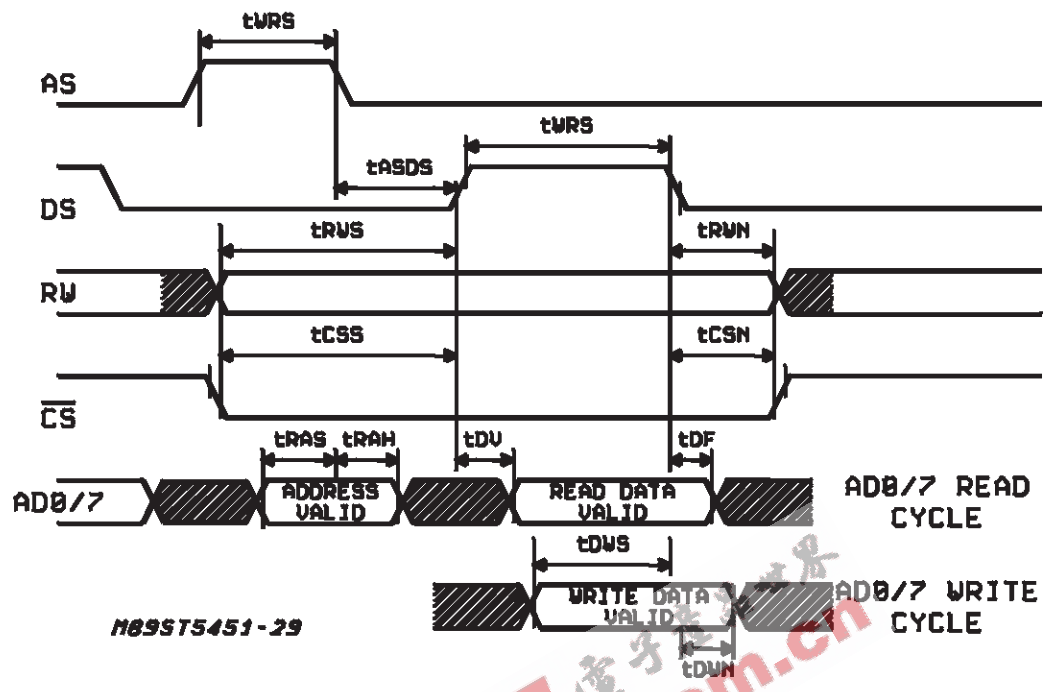
READ CYCLE (Multiplexed Intel Mode)

Symbol	Parameter	Min.	Max.	Unit
t_{LA}	Address Hold After ALE	10		ns
t_{AL}	Address to ALE Setup	20		ns
t_{RD}	Data Delay from $\overline{RD}$		110	ns
t_{RR}	$\overline{RD}$ Pulse Width	110		ns
t_{DF}	Output Float Delay		25	ns
t_{RI}	$\overline{RD}$ Control Interval	70		ns
t_{WA}	ALE Pulse Width	30		ns
t_{CSS}	$\overline{CE}$ to $\overline{RD}$ or $\overline{WR}$ set-up t_{CSS}	20		ns
t_{CSH}	$\overline{CE}$ hold after $\overline{RD}$ to $\overline{WR}$ t_{CSH}	10		ns

WRITE CYCLE (Multiplexed Intel Mode)

Symbol	Parameter	Min.	Max.	Unit
t_{WW}	$\overline{WR}$ Pulse Width	60		ns
t_{DW}	Data Setup to $\overline{WR}$	35		ns
t_{WD}	Data Hold after $\overline{WR}$	10		ns
t_{WI}	$\overline{WR}$ Control Interval	70		ns

Figure 18: Multiplexed Motorola-like µP bus timing



Symbol	Parameter	Min.	Max.	Unit
t_{WAS}	AS Pulse Width	30		ns
t_{WDS}	DS Pulse Width	110		ns
t_{ASDS}	AS low to DS high	10		ns
t_{RWS}	RW to DS setup	20		ns
t_{RWH}	RW hold after DS	10		ns
t_{CSS}	CS to DS setup	20		ns
t_{CSH}	CS hold after DS	10		ns
t_{AAS}	Address to AS setup	20		ns
t_{AAH}	Address hold after AS	10		ns

READ CYCLE

Symbol	Parameter	Min.	Max.	Unit
t_{DV}	Data Valid after DS		110	ns
t_{DF}	Output Flat Delay		25	ns

WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit
t_{DWS}	Data to DS setup	35		ns
t_{DWH}	Data Hold after DS	10		ns

DMA BUS TIMING (Reception Mode)

Symbol	Parameter	Min.	Max.	Unit
t_{ACC}	Data Delay from ACKR		110	ns
t_{DF}	Output Float Delay		25	ns
$t_W\overline{AR}$	Minimum width $\overline{ACKR}$	110		ns
t_{WAR}	Minimum width ACKR	70		ns
t_{DRAR}	REQR Delay from ACKR		80	ns

Figure 19: DMA frame reception timing

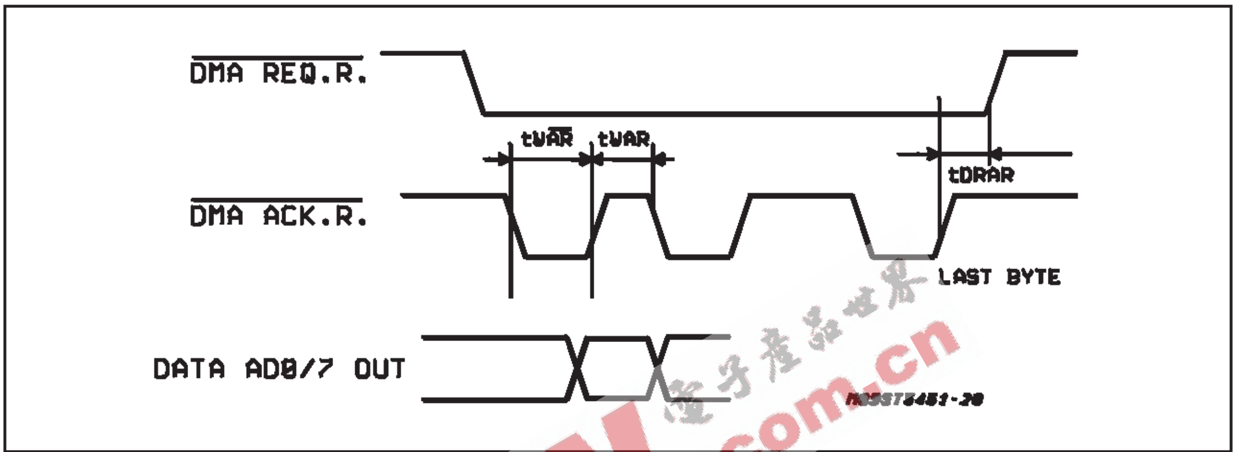
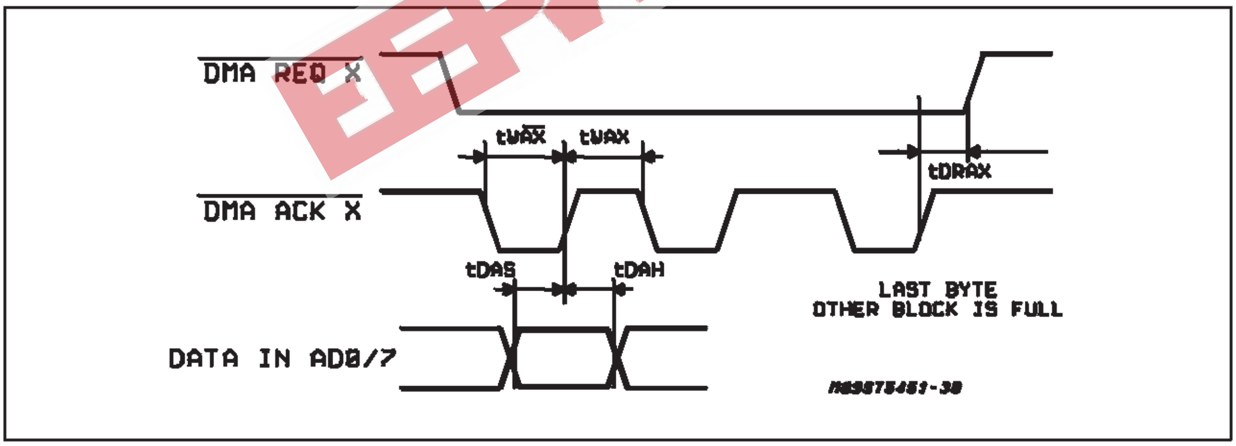


Figure 20: DMA frame transmission timing



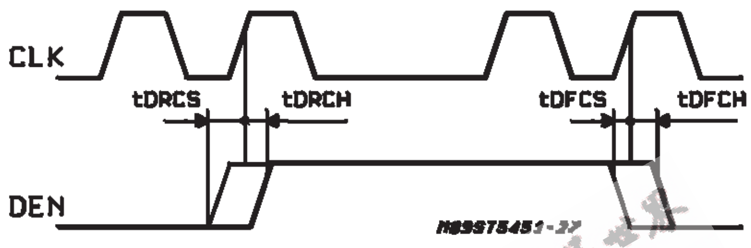
DMA BUS TIMING (Transmission Mode)

Symbol	Parameter	Min.	Max.	Unit
t_{DAS}	Data Setup to ACKX	35		ns
t_{DAH}	Data Hold from ACKX	10		ns
$t_W\overline{AX}$	Minimum width $\overline{ACKX}$	60		ns
t_{WAX}	Minimum width ACKX	70		ns
t_{DRAX}	REQX Delay from ACKX	80		ns

DEN TIMING

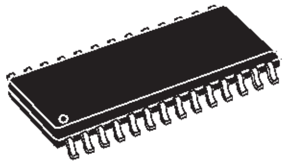
Symbol	Parameter	Min.	Max.	Unit
t_{DRCS}	DEN setup to CLK		30	ns
t_{DRCH}	DEN Hold from CLK		30	ns
t_{DFCS}	DEN Setup to CLK		30	ns
t_{DRCH}	DEN Hold from CLK		30	ns

Figure 21: DEN Timing

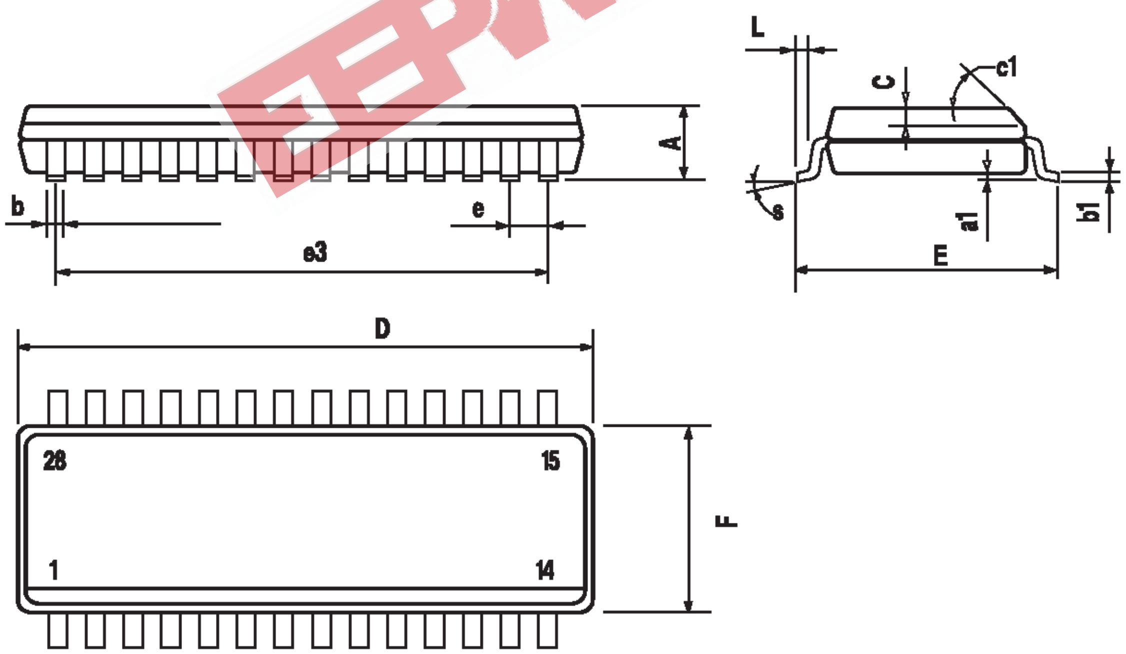


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8 ° (max.)					

OUTLINE AND MECHANICAL DATA



SO28



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