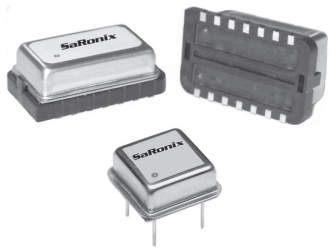
SaRonix

Crystal Clock Oscillator

3.3 & 5V, ACMOS, LVCMOS

Technical Data

ST41xx Series



ACTUAL SIZE

Description

A crystal controlled, low-current oscillator providing precise rise and fall times to drive ACMOS/LVCMOS loads. The tri-state function enables the output to go high impedance. Available in either a 14 or an 8 pin DIP compatible, resistance welded, all metal case. Pin 7 (or Pin 4) is grounded to case to reduce EMI. True SMD DIL 14 version also available, utilizing new adaptor technology (see separate data sheet for package dimensions).

Applications & Features

- Fiber Channel
- Gigabit Ethernet
- HCMOS/ACMOS/LVCMOS MPU's
- 3.3 or 5V operation
- High Drive capability
- Tri-State output standard
- Short circuit protected output
- Plastic SMD available, see ST41xH Series data sheet.
- Ceramic SMD available, see S19xx Series data sheet.
- True SMD version available, select option S in part number builder (see separate data sheet for package dimensions).

Frequency Range: 32 MHz to 125 MHz

Frequency Stability: ±20, ±25, ±50 or ±100 ppm over all conditions: calibration tolerance, operating temperature, input voltage change, load change, aging*, shock and vibration.
*1 year @ +40°C average ambient operating temperature

Temperature Range:

Operating:	0 to +70°C or -40 to +85°C
Storage:	-55 to +125°C

Supply Voltage:

Recommended Operating:	+5V ±5% or 3.3V ±10%

Supply Current: 50mA typ, 65mA, 35mA max @ 3.3V

Output Drive:

Symmetry:	ACMOS 32 to 60 MHz	ACMOS 60+ to 125 MHz	TTL 32 to 60 MHz	TTL 60+ to 125 MHz
0 to +70°C:	45/55%	45/55%	45/55%	45/55%
-40 to +85°C:	45/55%	40/60% (45/55% @ 3.3V)	45/55%	40/60%

Rise & Fall Times:	2ns max 20% to 80% V_{DD}
	1.5ns max 0.5 to 2.5V
Logic 0:	10% V_{DD} max or 20% V_{DD} max @ 3.3V
Logic 1:	80% V_{DD} min or 80% V_{DD} min @ 3.3V
Load:	50Ω ACMOS or 95Ω ACMOS @ 3.3V
Period Jitter RMS:	13ps max 32 to 72 MHz
	20ps max 72+ to 125 MHz, 0 to +70°C
	25ps max 72+ to 125 MHz, -40 to +85°C

Mechanical:

Shock:	MIL-STD-883, Method 2002, Condition B
Solderability:	MIL-STD-883, Method 2003
Terminal Strength:	MIL-STD-883, Method 2004, Condition B2
Vibration:	MIL-STD-883, Method 2007, Condition A
Solvent Resistance:	MIL-STD-202, Method 215
Resistance to Soldering Heat:	MIL-STD-202, Method 210, Condition A, B or C (I or J for Gull Wing or SMD)

Environmental:

Gross Leak Test:	MIL-STD-883, Method 1014, Condition C
Fine Leak Test:	MIL-STD-883, Method 1014, Condition A2
Thermal Shock:	MIL-STD-883, Method 1011, Condition A
Moisture Resistance:	MIL-STD-883, Method 1004

Part Numbering Guide

ST41 3 0 A – 106.2500 (T)

Series

Type
3 = 3.3V LVCMOS
5 = 5V TTL
6 = 5V ACMOS

Package Style
0 = Full Size, Metal
9 = Half Size, Metal
J = Half Size, Metal, Gull Wing
K = Full Size, Metal, Gull Wing
S = True SMD Adaptor (see product photo)

Stability Tolerance
AA = ±20 ppm, 0 to +70°C
A = ±25 ppm, 0 to +70°C
B = ±50 ppm, 0 to +70°C
C = ±100 ppm, 0 to +70°C
E = ±50 ppm, -40 to +85°C
F = ±100 ppm, -40 to +85°C

Frequency

Packing Method
(T) = Tape & Reel for SMD versions full reel increments only (200pcs)
Blank = Bulk

DS-183 REV C

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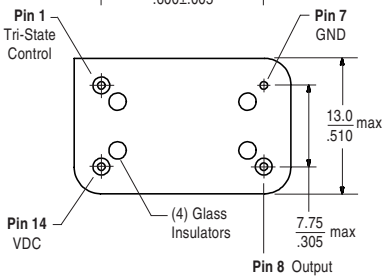
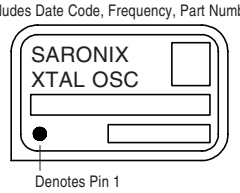
Package Details

FULL SIZE PACKAGE

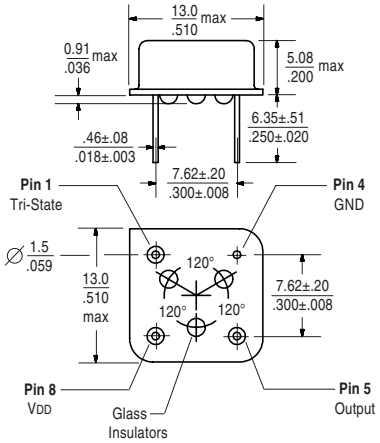


Standard Marking Format **

Includes Date Code, Frequency, Part Number

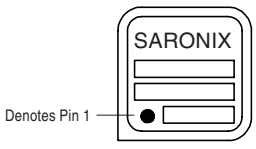


HALF SIZE PACKAGE



Standard Marking Format **

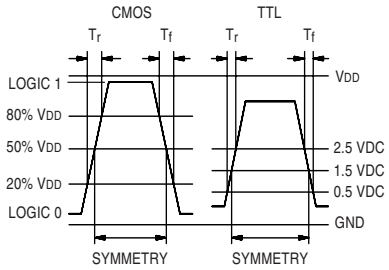
Includes Date Code, Frequency, Part Number



** Exact location of items may vary

Scale: None (Dimensions in $\frac{mm}{inches}$)

Output Waveform

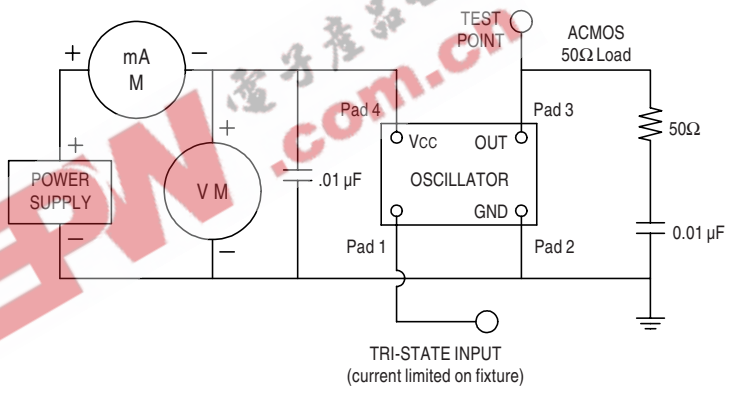


Tri-State Logic Table

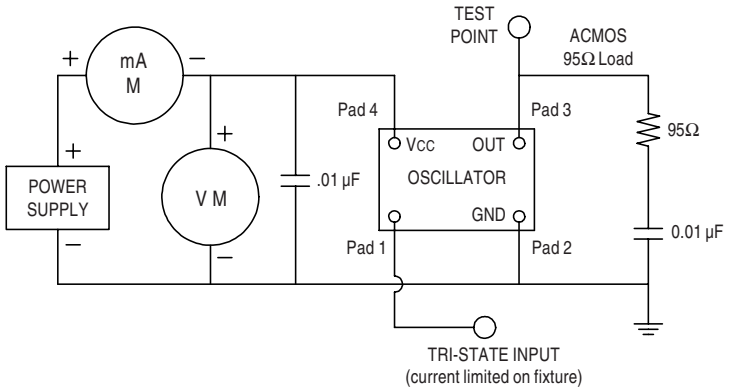
Pin 1 Input	Pin 8 (5) Output
Logic 1 or NC	Oscillation
Logic 0 or GND	High Impedance

Required Input Levels on Pin 1:
Logic 1 = 2.2V min
Logic 0 = 0.8V max

Test Circuits



50Ω ACMOS TEST CIRCUIT



95Ω ACMOS TEST CIRCUIT

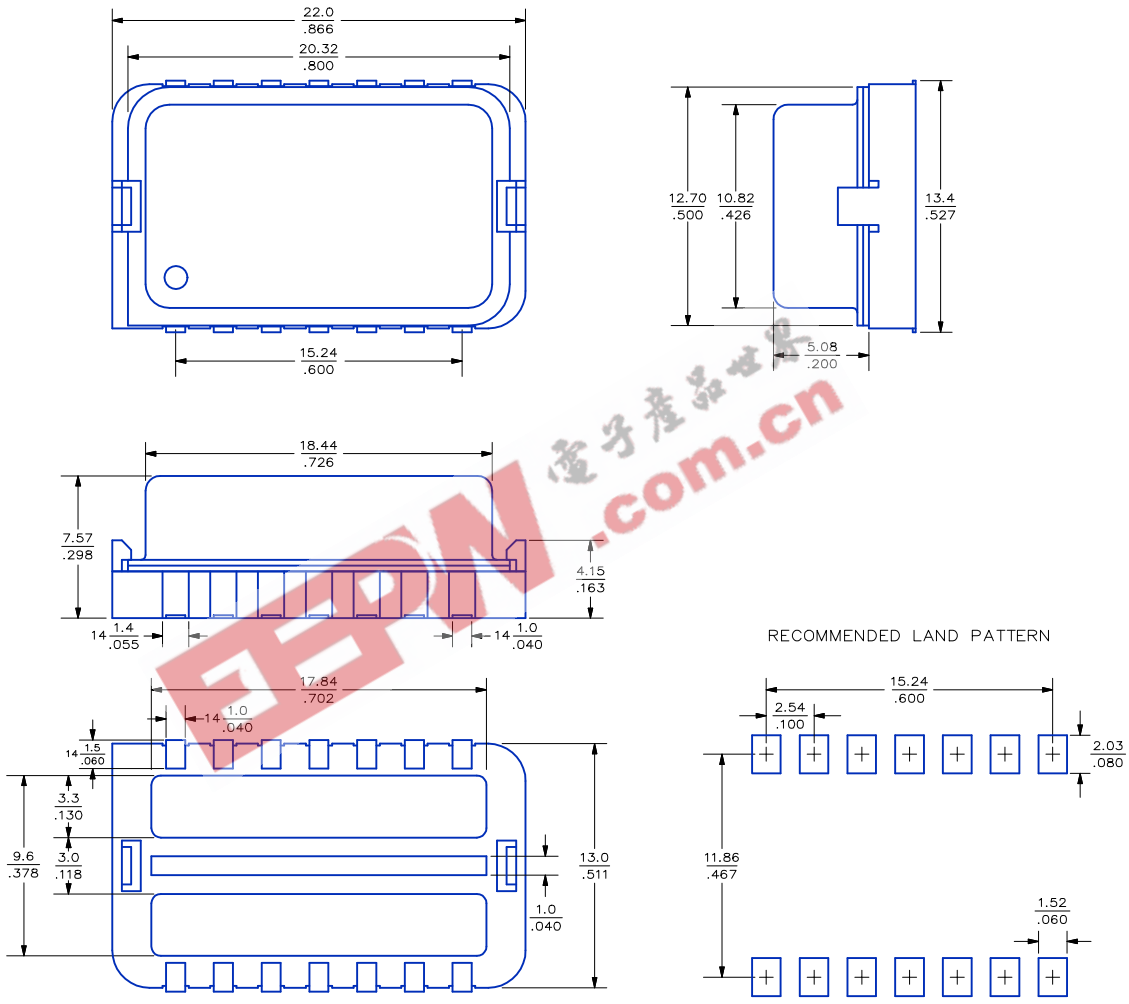
All specifications are subject to change without notice.

DS-183 REV C

SaRonix

True SMD Adaptor - 7.57mm High

Technical Data



REV A