STK22C48

2Kx8 AutoStore nvSRAM

FEATURES

- **25, 45 ns Read Access & R/W Cycle Times**
- **Unlimited Read/Write Endurance**
- **Automatic Non-Volatile *STORE* on Power Loss**
- **Non-Volatile *STORE* Under Hardware Control**
- **Automatic *RECALL* to SRAM on Power Up**
- **Unlimited RECALL Cycles**
- **1 Million *STORE* Cycles**
- **100-Year Non-volatile Data Retention**
- **Single 5.0V ±10% Operation**
- **Commercial, Industrial, and Military Temperatures**
- **28-Pin 300 mil SOIC or 330 mil SOIC (RoHS-Compliant)**

DESCRIPTION

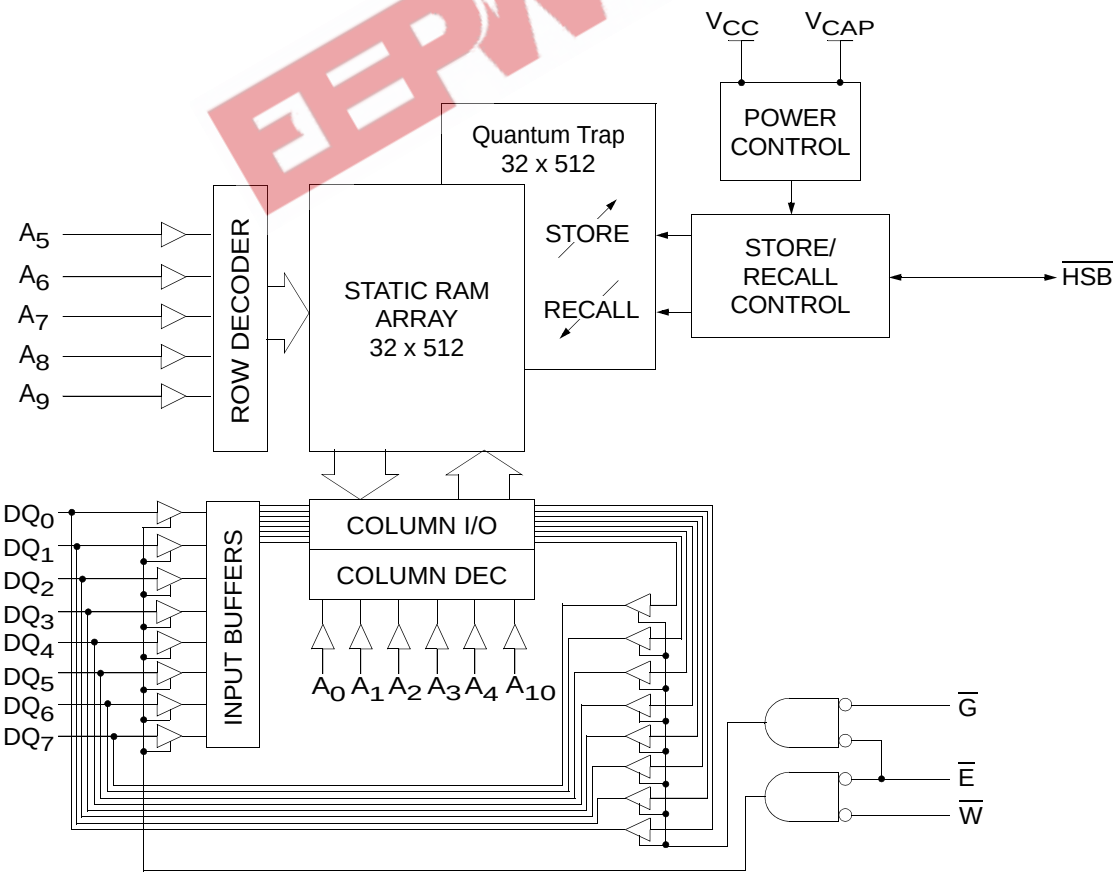
The Simtek STK22C48 is a 16Kb fast static RAM with a nonvolatile Quantum Trap storage element included with each memory cell.

The SRAM provides the fast access & cycle times, ease of use, and unlimited read & write endurance of a normal SRAM.

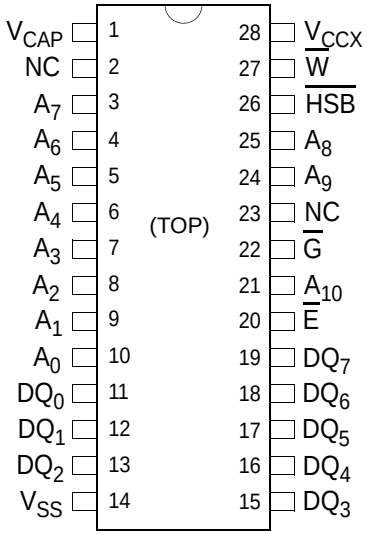
Data transfers automatically to the non-volatile storage cells when power loss is detected (the *STORE* operation). On power-up, data is automatically restored to the SRAM (the *RECALL* operation). Both *STORE* and RECALL operations are also available under software control.

The Simtek nvSRAM is the first monolithic non-volatile memory to offer unlimited writes and reads. It is the highest-performance, most reliable non-volatile memory available.

BLOCK DIAGRAM



PIN CONFIGURATIONS



28-pin 300 mil SOIC

28-pin 330 mil SOIC

PIN DESCRIPTIONS

Pin Name	I/O	Description
A_{10}-A_0	Input	Address: The 11 address inputs select one of 2,048 bytes in the nvSRAM array
DQ_7-DQ_0	I/O	Data: Bi-directional 8-bit data bus for accessing the nvSRAM
$\overline{E}$	Input	Chip Enable: The active low $\overline{E}$ input selects the device
$\overline{W}$	Input	Write Enable: The active low $\overline{W}$ enables data on the DQ pins to be written to the address location latched by the falling edge of $\overline{E}$
$\overline{G}$	Input	Output Enable: The active low $\overline{G}$ input enables the data output buffers during read cycles. De-asserting $\overline{G}$ high caused the DQ pins to tri-state.
V_{CC}	Power Supply	Power: 5.0V, ±10%
V_{SS}	Power Supply	Ground

ABSOLUTE MAXIMUM RATINGS[a]

Voltage on Input Relative to Ground . . . . . –0.5V to 7.0V
Voltage on Input Relative to V_{SS} . . . . . –0.6V to (V_{CC} + 0.5V)
Voltage on DQ_{0-7} or $\overline{HSB}$ . . . . . –0.5V to (V_{CC} + 0.5V)
Temperature under Bias . . . . . –55°C to 125°C
Storage Temperature . . . . . –65°C to 150°C
Power Dissipation 1W
DC Output Current (1 output at a time, 1s duration) 15mA

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Package Thermal Characteristics - See Website at http://www.simtek.com

DC CHARACTERISTICS

(V_{CC} = 5.0V ± 10%)[e]

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC1}[b]	Average V_{CC} Current		85 65		90 65	mA mA	t_{AVAV} = 25ns t_{AVAV} = 45ns
I_{CC2}[c]	Average V_{CC} Current during *STORE*		3		3	mA	All Inputs Don't Care, V_{CC} = max
I_{CC3}[b]	Average V_{CC} Current at t_{AVAV} = 200ns 5V, 25°C, Typical		10		10	mA	$\overline{W} \geq (V_{CC} - 0.2V)$ All Others Cycling, CMOS Levels
I_{CC4}[c]	Average V_{CAP} Current during AutoStore Cycle		2		2	mA	All Inputs Don't Care
I_{SB1}[d]	Average V_{CC} Current (Standby, Cycling TTL Input Levels)		25 18		26 19	mA mA	t_{AVAV} = 25ns, $\overline{E} \geq V_{IH}$ t_{AVAV} = 45ns, $\overline{E} \geq V_{IH}$
I_{SB2}[d]	V_{CC} Standby Current (Standby, Stable CMOS Input Levels)		1.5		1.5	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ All Others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current		±1		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off-State Output Leakage Current		±5		±5	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}, $\overline{E}$ or $\overline{G} \geq V_{IH}$
V_{IH}	Input Logic "1" Voltage	2.2	V_{CC} + .5	2.2	V_{CC} + .5	V	All Inputs
V_{IL}	Input Logic "0" Voltage	V_{SS} – .5	0.8	V_{SS} – .5	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	I_{OUT} = –4mA except $\overline{HSB}$
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	I_{OUT} = 8mA except $\overline{HSB}$
V_{BL}	Logic "0" Voltage on $\overline{HSB}$ Output		0.4		0.4	V	I_{OUT} = 3mA
T_A	Operating Temperature	0	70	–40	85	°C	
V_{CAP}	Storage Capacitance	61	220	61	220	µF	5 Volt rated, 68 µF+20%/-10% Nom.

Note b: I_{CC1} and I_{CC3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
Note c: I_{CC2} and I_{CC4} are the average currents required for the duration of the respective *STORE* cycles (t_{STORE}).
Note d: $\overline{E} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out.
Note e: V_{CC} reference levels throughout this datasheet refer to V_{CC} if that is where the power supply connection is made, or V_{CAP} if V_{CC} is connected to ground.

AC TEST CONDITIONS

Input Pulse Levels. . . . . 0V to 3V
Input Rise and Fall Times . . . . . ≤ 5ns
Input and Output Timing Reference Levels. 1.5V
Output Load . . . . . See Figure 1

CAPACITANCE[f] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	8	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

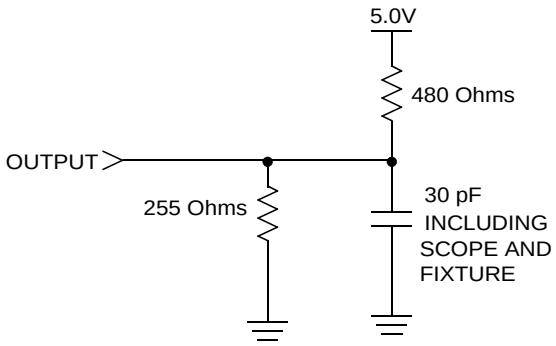


Figure 1: AC Output Loading

Note f: These parameters are guaranteed but not tested.

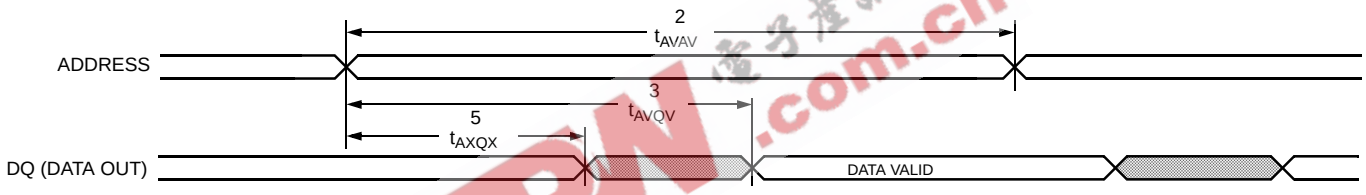
SRAM READ CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)[e]

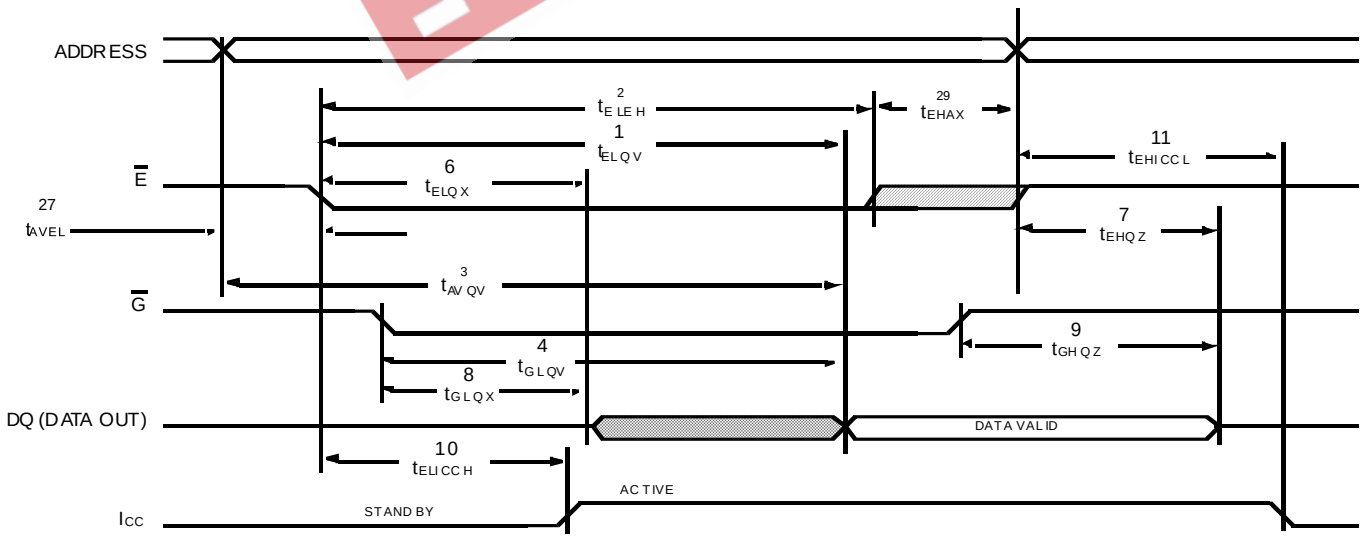
NO.	SYMBOLS		PARAMETER	STK22C48-25		STK22C48-45		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		45	ns
2	t_{AVAV}[g], t_{ELEH}[g]	t_{RC}	Read Cycle Time	25		45		ns
3	t_{AVQV}[h]	t_{AA}	Address Access Time		25		45	ns
4	t_{GLQV}	t_{OE}	Output Enable to Data Valid		10		20	ns
5	t_{AXQX}[h]	t_{OH}	Output Hold after Address Change	5		5		ns
6	t_{ELQX}	t_{LZ}	Address Change or Chip Enable to Output Active	5		5		ns
7	t_{EHQZ}[i]	t_{HZ}	Address Change or Chip Disable to Output Inactive		10		15	ns
8	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		ns
9	t_{GHQZ}[i]	t_{OHZ}	Output Disable to Output Inactive		10		15	ns
10	t_{ELICCH}[f]	t_{PA}	Chip Enable to Power Active	0		0		ns
11	t_{EHICCL}[f]	t_{PS}	Chip Disable to Power Standby		25		45	ns

Note g: $\overline{W}$ and $\overline{HSB}$ must be high during SRAM READ cycles.
Note h: Device is continuously selected with $\overline{E}$ and $\overline{G}$ both low.
Note i: Measured ± 200mV from steady state output voltage.

SRAM READ CYCLE #1: Address Controlled[g, h]



SRAM READ CYCLE #2: $\overline{E}$ and $\overline{G}$ Controlled[g]



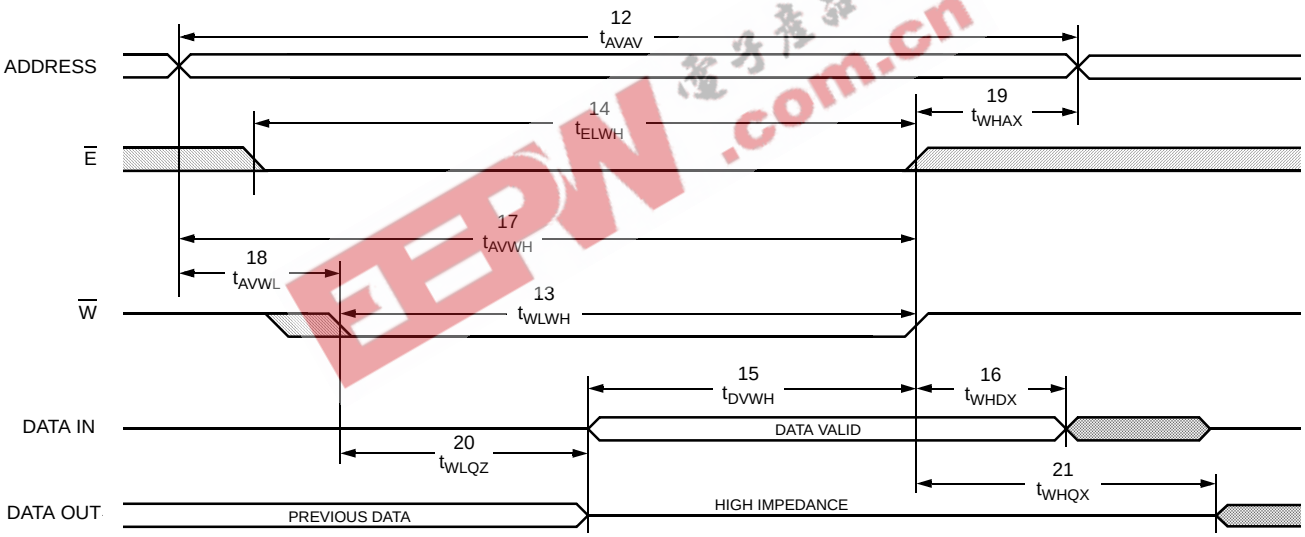
SRAM WRITE CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)[e]

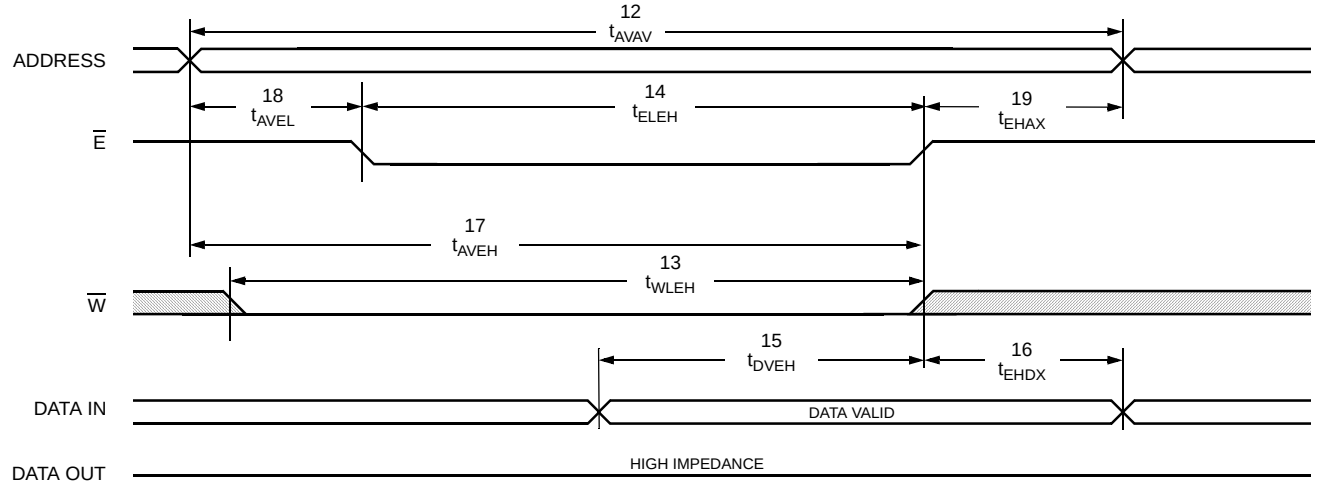
NO.	SYMBOLS			PARAMETER	STK22C48-25		STK22C48-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	25		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	20		30		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		30		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	10		15		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold after End of Write	0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		30		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold after End of Write	0		0		ns
20	t_{WLQZ} [i, j]		t_{WZ}	Write Enable to Output Disable		10		15	ns
21	t_{WHQX}		t_{OW}	Output Active after End of Write	5		5		ns

Note j: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high-impedance state.
Note k: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note l: $\overline{HSB}$ must be high during SRAM WRITE cycles.

SRAM WRITE CYCLE #1: $\overline{W}$ Controlled[k, l]



SRAM WRITE CYCLE #2: $\overline{E}$ Controlled[k, l]



HARDWARE MODE SELECTION

$\overline{E}$	$\overline{W}$	$\overline{HSB}$	A_{12} - A_0 (hex)	MODE	I/O	POWER	NOTES
H	X	H	X	Not Selected	Output High Z	Standby	
L	H	H	X	Read SRAM	Output Data	Active	n
L	L	H	X	Write SRAM	Input Data	Active	
X	X	L	X	Nonvolatile *STORE*	Output High Z	I_{CC2}	m

Note m: $\overline{HSB}$ *STORE* operation occurs only if an SRAM write has been done since the last nonvolatile cycle. After the *STORE* (if any) completes, the part will go into standby mode, inhibiting all operations until $\overline{HSB}$ rises.
Note n: I/O state assumes $\overline{G} \leq V_{IL}$. Activation of nonvolatile cycles does not depend on state of $\overline{G}$.

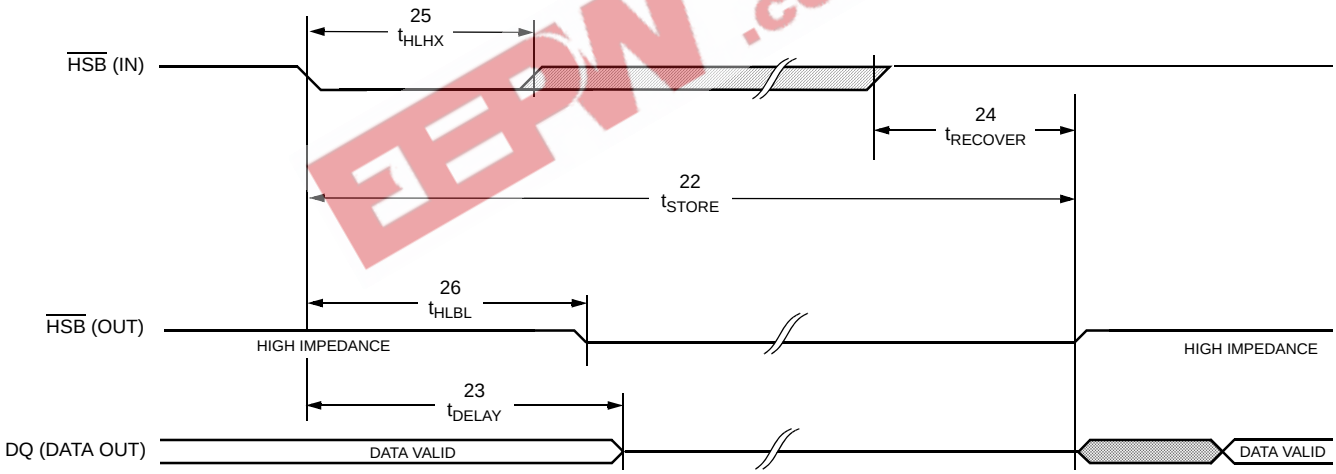
HARDWARE *STORE* CYCLE

(V_{CC} = 5.0V ± 10%)[e]

NO.	SYMBOLS		PARAMETER	STK22C48		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
22	t_{STORE}	t_{HLHZ}	*STORE* Cycle Duration		10	ms	i, o
23	t_{DELAY}	t_{HLQZ}	Time Allowed to Complete SRAM Cycle	1		µs	i, p
24	$t_{RECOVER}$	t_{HHQX}	Hardware *STORE* High to Inhibit Off		700	ns	o, q
25	t_{HLHX}		Hardware *STORE* Pulse Width	15		ns	
26	t_{HLBL}		Hardware *STORE* Low to Store Busy		300	ns	

Note o: $\overline{E}$ and $\overline{G}$ low for output behavior.
Note p: $\overline{E}$ and $\overline{G}$ low and $\overline{W}$ high for output behavior.
Note q: $t_{RECOVER}$ is only applicable after t_{STORE} is complete.

HARDWARE *STORE* CYCLE



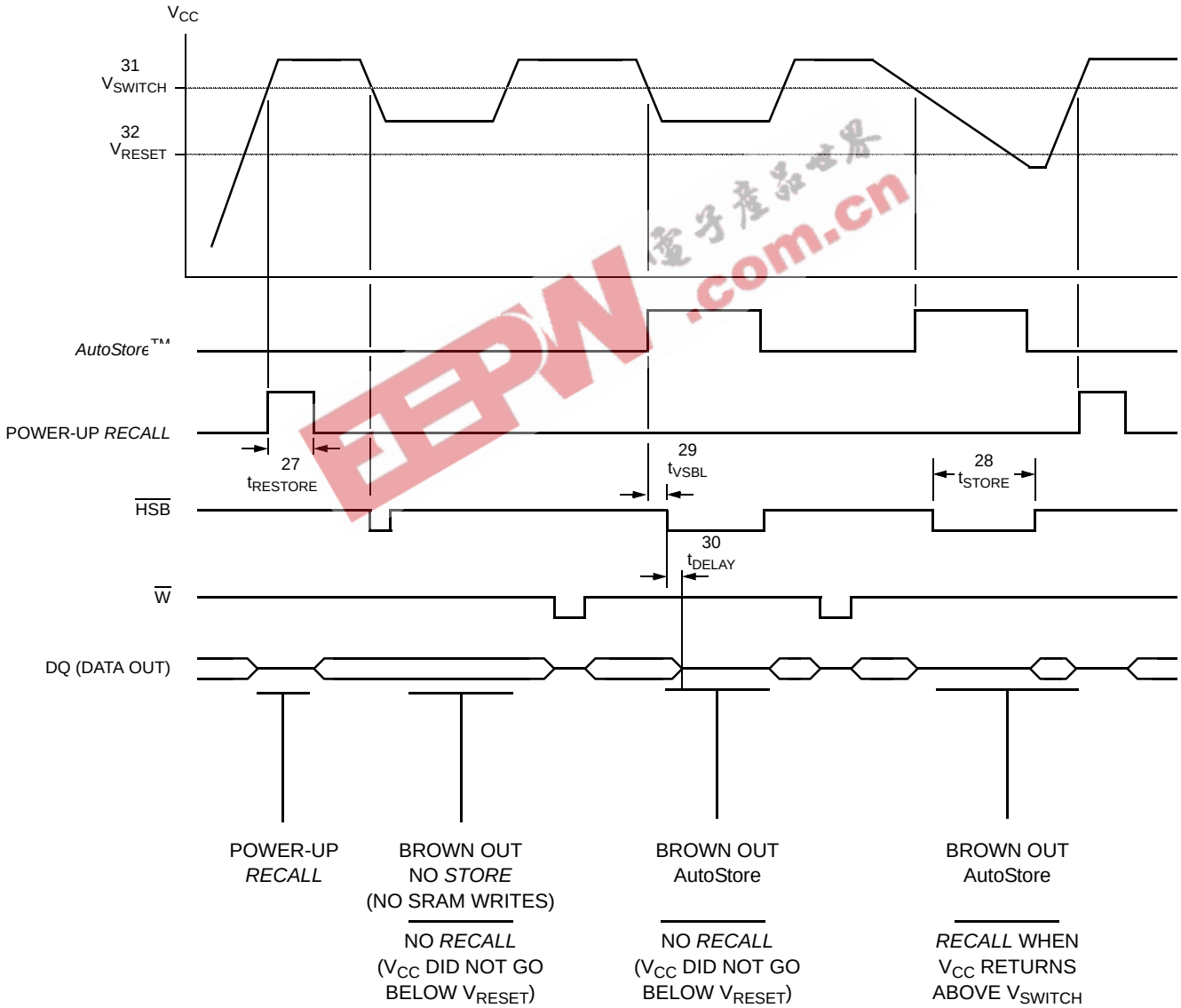
AutoStore™/POWER-UP RECALL

(V_{CC} = 5.0V ± 10%)[e]

NO.	SYMBOLS		PARAMETER	STK22C48		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
27	$t_{RESTORE}$		Power-up *RECALL* Duration		550	µs	r
28	t_{STORE}	t_{HLHZ}	*STORE* Cycle Duration		10	ms	p, s
29	t_{VSBL}		Low Voltage Trigger (V_{SWITCH}) to $\overline{HSB}$ Low		300	ns	l
30	t_{DELAY}	t_{BLQZ}	Time Allowed to Complete SRAM Cycle	1		µs	o
31	V_{SWITCH}		Low Voltage Trigger Level	4.0	4.5	V	
32	V_{RESET}		Low Voltage Reset Level		3.6	V	

Note r: $t_{RESTORE}$ starts from the time V_{CC} rises above V_{SWITCH}.
Note s: $\overline{HSB}$ is asserted low for 1µs when V_{CAP} drops through V_{SWITCH}. If an SRAM write has not taken place since the last nonvolatile cycle, $\overline{HSB}$ will be released and no *STORE* will take place.

AutoStore™/POWER-UP RECALL



nvSRAM OPERATION

The STK22C48 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as a standard fast static RAM. In nonvolatile mode, data is transferred from SRAM to Nonvolatile Elements (the *STORE* operation) or from Nonvolatile Elements to SRAM (the *RECALL* operation). In this mode SRAM functions are disabled.

NOISE CONSIDERATIONS

The STK22C48 is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1µF connected between V_{CAP} and V_{SS}, using leads and traces that are as short as possible. As with all high-speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

SRAM READ

The STK22C48 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are low and $\overline{W}$ and $\overline{HSB}$ are high. The address specified on pins A_{0-10} determines which of the 2,048 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ cycle #1). If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at t_{ELQV} or at t_{GLQV}, whichever is later (READ cycle #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought high, or $\overline{W}$ or $\overline{HSB}$ is brought low.

SRAM WRITE

A WRITE cycle is performed whenever $\overline{E}$ and $\overline{W}$ are low and $\overline{HSB}$ is high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ goes high at the end of the cycle. The data on the common I/O pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept high during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\overline{G}$ is left low, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{W}$ goes low.

POWER-UP *RECALL*

During power up, or after any low-power condition (V_{CAP} < V_{RESET}), an internal *RECALL* request will be latched. When V_{CAP} once again exceeds the sense voltage of V_{SWITCH}, a *RECALL* cycle will automatically be initiated and will take $t_{RESTORE}$ to complete.

If the STK22C48 is in a WRITE state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected either between $\overline{W}$ and system V_{CC} or between $\overline{E}$ and system V_{CC}.

AutoStore MODE

The STK22C48 can be powered in one of three modes.

During normal AutoStore operation, the STK22C48 will draw current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge will be used by the chip to perform a single *STORE* operation. After power up, when the voltage on the V_{CAP} pin drops below V_{SWITCH}, the part will automatically disconnect the V_{CAP} pin from V_{CC} and initiate a *STORE* operation.

Figure 2 shows the proper connection of capacitors for automatic store operation. A charge storage capacitor having a capacity of between 68µF and 220µF (± 20%) rated at 6V should be provided.

In system power mode, both V_{CC} and V_{CAP} are connected to the + 5V power supply without the 68µF capacitor. In this mode the AutoStore function of the

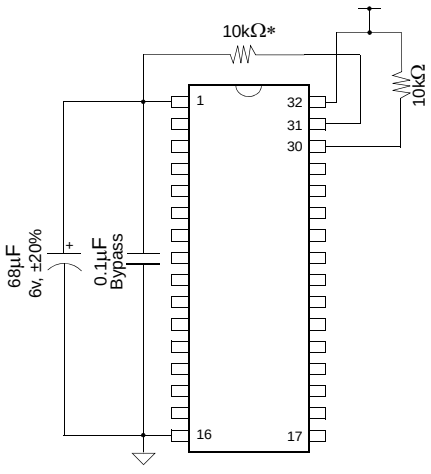


Figure 2: AutoStore Mode
***If $\overline{HSB}$ is not used, it should be left unconnected.**

STK22C48 will operate on the stored system charge as power goes down. The user must, however, guarantee that V_{CC} does not drop below 3.6V during the 10ms *STORE* cycle.

AutoStore INHIBIT MODE

If an automatic *STORE* on power loss is not required, then V_{CC} can be tied to ground and + 5V applied to V_{CAP} (Figure 3). This is the AutoStore Inhibit mode, in which the AutoStore function is disabled. If the STK22C48 is operated in this configuration, references to V_{CC} should be changed to V_{CAP} throughout this data sheet. In this mode, *STORE* operations may be triggered with the $\overline{HSB}$ pin. To enable or disable AutoStore using an IO port pin, see “PREVENTING STORES” on page 9.

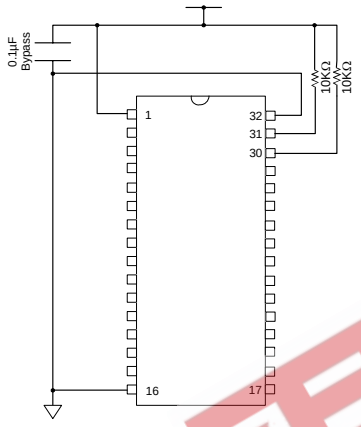


Figure 3: AutoStore Inhibit Mode

In order to prevent unneeded *STORE* operations, automatic *STORE*s as well as those initiated by externally driving $\overline{HSB}$ low will be ignored unless at least one WRITE operation has taken place since the most recent *STORE* or *RECALL* cycle.

If the power supply drops faster than 20 µs/volt before V_{CC} reaches V_{SWITCH}, then a 2.2 ohm resistor should be inserted between V_{CC} and the system supply to avoid momentary excess of current between Vcc and Vcap.

$\overline{HSB}$ OPERATION

The STK22C48 provides the $\overline{HSB}$ pin for controlling and acknowledging the *STORE* operations. The $\overline{HSB}$ pin is used to request a hardware *STORE* cycle. When the $\overline{HSB}$ pin is driven low, the STK22C48 will conditionally initiate a *STORE* operation after t_{DELAY}; an actual *STORE* cycle will only begin if a WRITE to the SRAM took place since the last *STORE* or *RECALL* cycle. The $\overline{HSB}$ pin has a very resistive pullup and is internally driven low to indicate a busy condition while the *STORE* (initiated by any means) is in progress. Pull up this pin with an external 10K ohm resistor to V_{CAP} if $\overline{HSB}$ is used as a driver.

SRAM READ and WRITE operations that are in progress when $\overline{HSB}$ is driven low by any means are given time to complete before the *STORE* operation is initiated. After $\overline{HSB}$ goes low, the STK22C48 will continue SRAM operations for t_{DELAY}. During t_{DELAY}, multiple SRAM READ operations may take place. If a WRITE is in progress when $\overline{HSB}$ is pulled low it will be allowed a time, t_{DELAY}, to complete. However, any SRAM WRITE cycles requested after $\overline{HSB}$ goes low will be inhibited until $\overline{HSB}$ returns high.

The $\overline{HSB}$ pin can be used to synchronize multiple STK22C48s while using a single larger capacitor. To operate in this mode the $\overline{HSB}$ pin should be connected together to the $\overline{HSB}$ pins from the other STK22C48s. An external pull-up resistor to + 5V is required since $\overline{HSB}$ acts as an open drain pull down. The V_{CAP} pins from the other STK22C48 parts can be tied together and share a single capacitor. The capacitor size must be scaled by the number of devices connected to it. When any one of the STK22C48s detects a power loss and asserts $\overline{HSB}$, the common $\overline{HSB}$ pin will cause all parts to request a *STORE* cycle (a *STORE* will take place in those STK22C48s that have been written since the last nonvolatile cycle).

During any *STORE* operation, regardless of how it was initiated, the STK22C48 will continue to drive the $\overline{HSB}$ pin low, releasing it only when the *STORE* is complete. Upon completion of the *STORE* operation the STK22C48 will remain disabled until the $\overline{HSB}$ pin returns high.

If $\overline{HSB}$ is not used, it should be left unconnected.

PREVENTING STORES

The *STORE* function can be disabled on the fly by holding $\overline{HSB}$ high with a driver capable of sourcing 30mA at a VOH of at least 2.2V, as it will have to overpower the internal pull-down device that drives $\overline{HSB}$ low for 20µs at the onset of a *STORE*. When the STK22C48 is connected for AutoStore operation (system V_{CC} connected to V_{CC} and a 68µF capacitor on V_{CAP}) and V_{CC} crosses V_{SWITCH} on the way down, the STK22C48 will attempt to pull $\overline{HSB}$ low; if $\overline{HSB}$ doesn't actually get below V_{IL}, the part will stop trying to pull $\overline{HSB}$ low and abort the *STORE* attempt.

HARDWARE PROTECT

The STK22C48 offers hardware protection against inadvertent *STORE* operation and SRAM WRITEs during low-voltage conditions. When $V_{CAP} < V_{SWITCH}$, all externally initiated *STORE* operations and SRAM WRITEs are inhibited.

AutoStore can be completely disabled by tying V_{CCX} to ground and applying + 5V to V_{CAP}. This is the AutoStore Inhibit mode; in this mode *STORE*s are only initiated by explicit request using the $\overline{HSB}$ pin.

LOW AVERAGE ACTIVE POWER

The STK22C48 draws significantly less current when it is cycled at times longer than 50ns. Figure 4 shows the relationship between I_{CC} and READ cycle time. Worst-case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, V_{CC} = 5.5V, 100% duty cycle on chip enable). Figure 5 shows the same relationship for WRITE cycles. If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled. The overall average current drawn by the STK22C48 depends on the following items: 1) CMOS vs. TTL input levels; 2) the duty cycle of chip enable; 3) the overall cycle rate for accesses; 4) the ratio of READs to WRITEs; 5) the operating temperature; 6) the V_{CC} level; and 7) I/O loading.

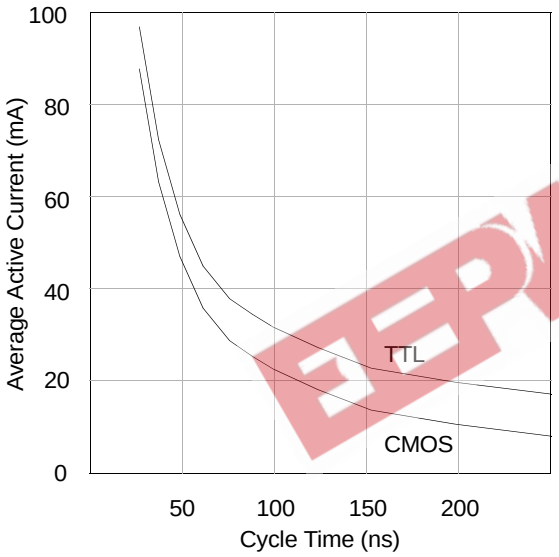


Figure 4: Icc (max) Reads

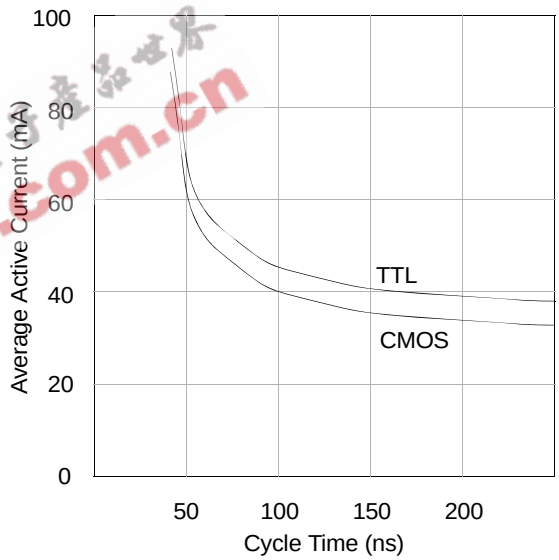


Figure 5: I_{cc} (max) Writes

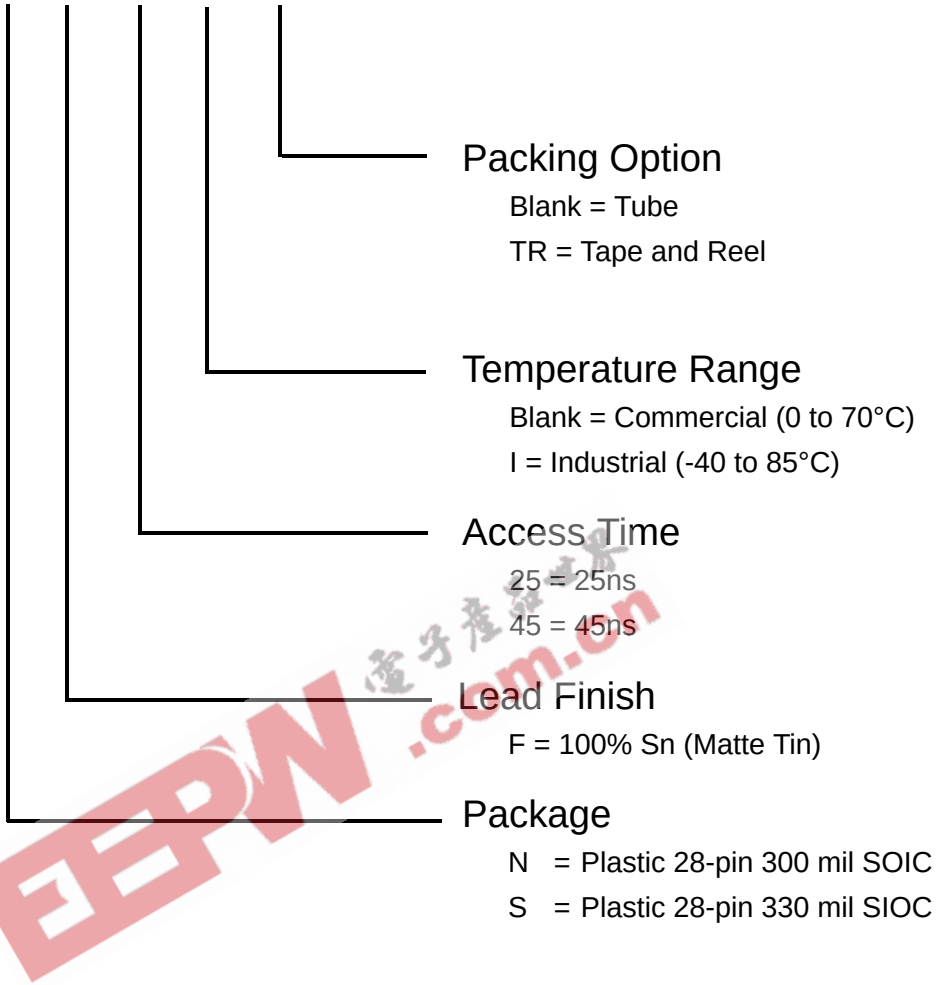
BEST PRACTICES

nvSRAM products have been used effectively for over 15 years. While ease-of-use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

- The non-volatile cells in an nvSRAM are programmed on the test floor during final test and quality assurance. Incoming inspection routines at customer or contract manufacturer's sites will sometimes reprogram these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. End product's firmware should not assume an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration, cold or warm boot status, etc. should always program a unique NV pattern (e.g., complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.
- Power up boot firmware routines should rewrite the nvSRAM into the desired state. While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently (program bugs, incoming inspection routines, etc.).
- The V_{cap} value specified in this datasheet includes a minimum and a maximum value size. Best practice is to meet this requirement and not exceed the max V_{cap} value because the higher inrush currents may reduce the reliability of the internal pass transistor. Customers that want to use a larger V_{cap} value to make sure there is extra store charge should discuss their V_{cap} size selection with Simtek.

ORDERING INFORMATION

STK22C48 - N F 45 I TR

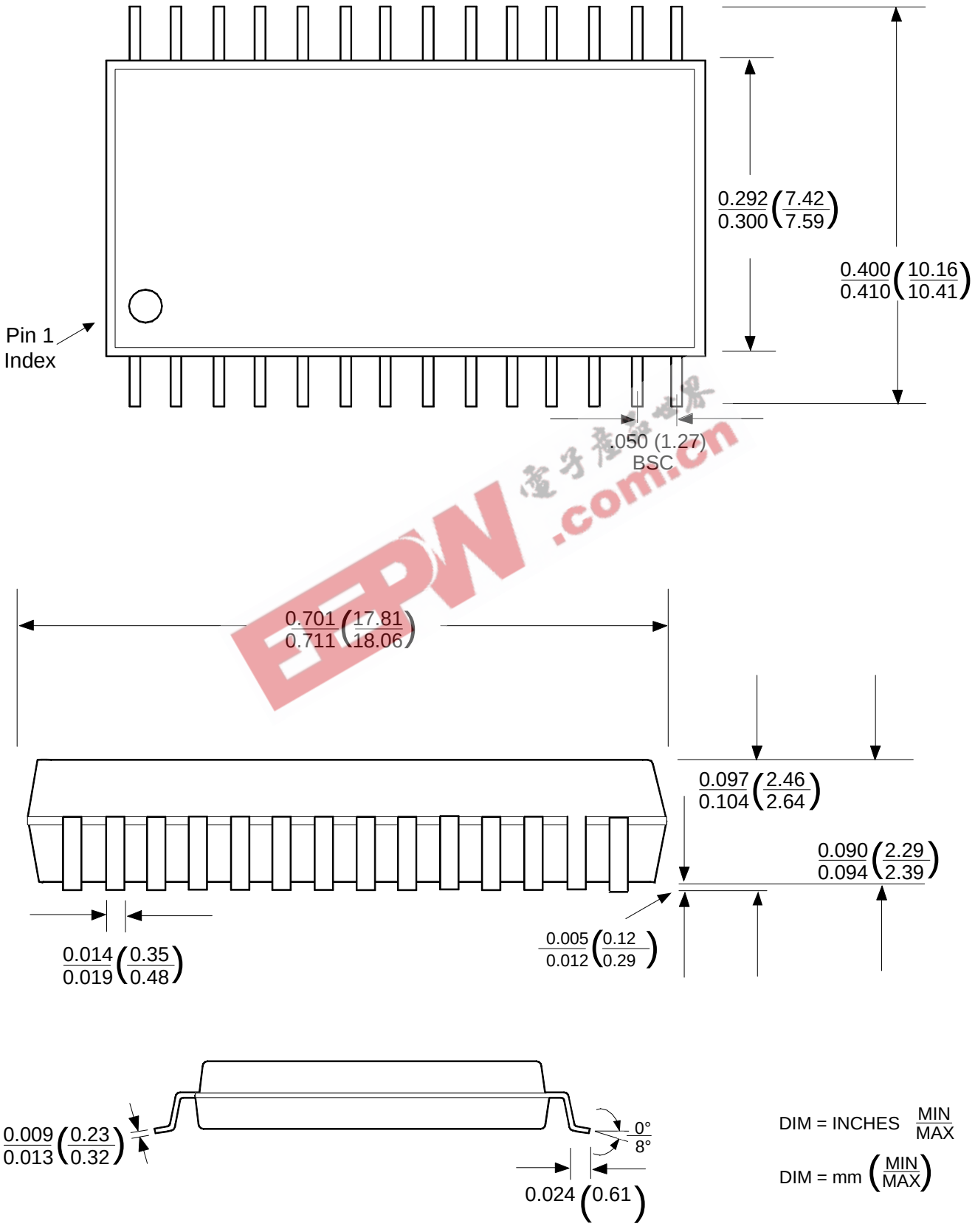


Ordering Information

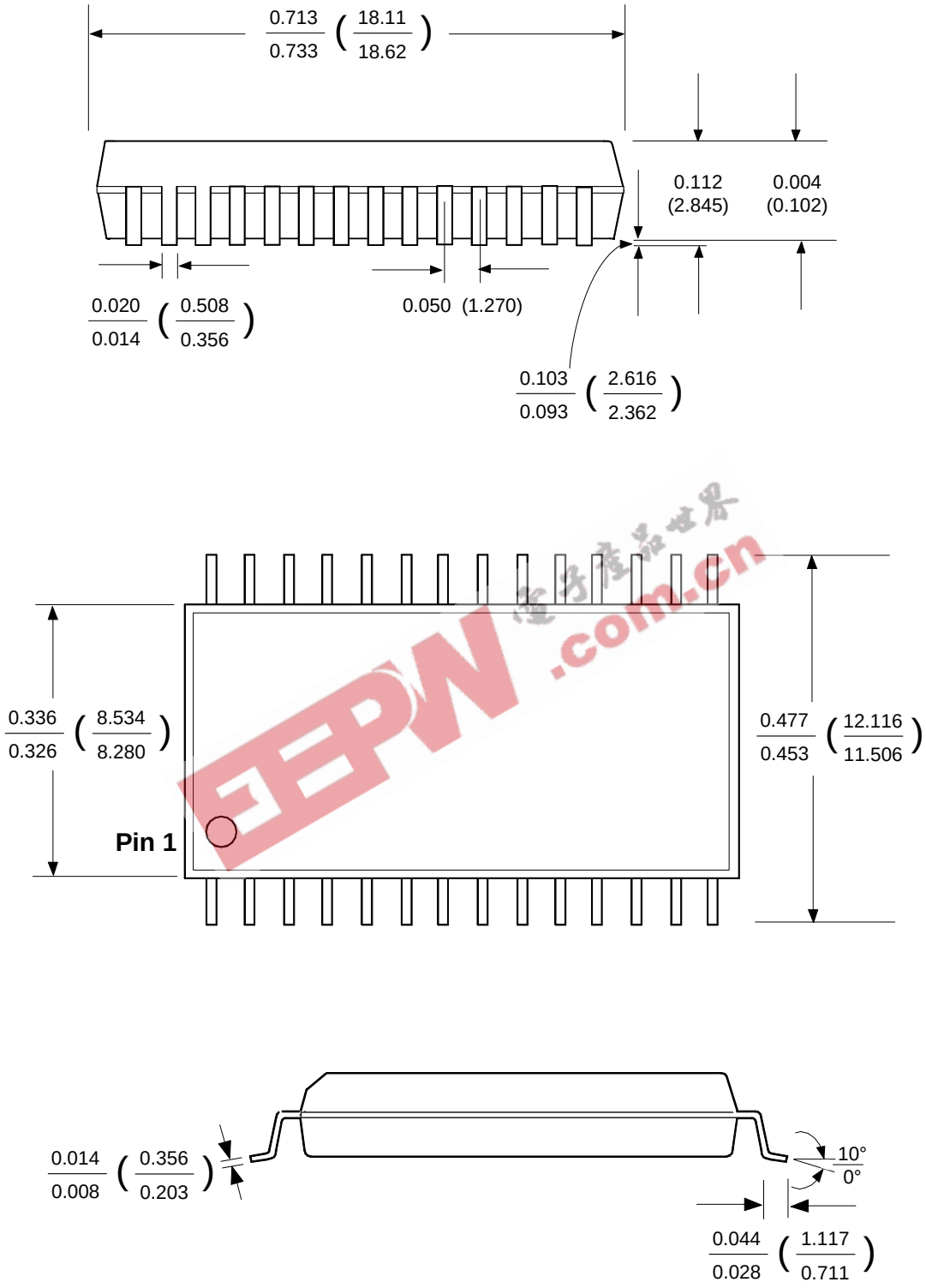
Item Number	Item Name	Access Times	Temperature
STK22C48-NF25	5V 2Kx 8 AutoStore nvSRAM SOP28-300	25 ns access time	Commercial
STK22C48-NF45	5V 2Kx 8 AutoStore nvSRAM SOP28-300	45 ns access time	Commercial
STK22C48-SF25	5V 2Kx 8 AutoStore nvSRAM SOP28-330	25 ns access time	Commercial
STK22C48-SF45	5V 2Kx 8 AutoStore nvSRAM SOP28-330	45 ns access time	Commercial
STK22C48-NF25TR	5V 2Kx 8 AutoStore nvSRAM SOP28-300	25 ns access time	Commercial
STK22C48-NF45TR	5V 2Kx 8 AutoStore nvSRAM SOP28-300	45 ns access time	Commercial
STK22C48-SF25TR	5V 2Kx 8 AutoStore nvSRAM SOP28-330	25 ns access time	Commercial
STK22C48-SF45TR	5V 2Kx 8 AutoStore nvSRAM SOP28-330	45 ns access time	Commercial
STK22C48-NF25I	5V 2Kx 8 AutoStore nvSRAM SOP28-300	25 ns access time	Industrial
STK22C48-NF45I	5V 2Kx 8 AutoStore nvSRAM SOP28-300	45 ns access time	Industrial
STK22C48-SF25I	5V 2Kx 8 AutoStore nvSRAM SOP28-330	25 ns access time	Industrial
STK22C48-SF45I	5V 2Kx 8 AutoStore nvSRAM SOP28-330	45 ns access time	Industrial
STK22C48-NF25ITR	5V 2Kx 8 AutoStore nvSRAM SOP28-300	25 ns access time	Industrial
STK22C48-NF45ITR	5V 2Kx 8 AutoStore nvSRAM SOP28-300	45 ns access time	Industrial
STK22C48-SF25ITR	5V 2Kx 8 AutoStore nvSRAM SOP28-330	25 ns access time	Industrial
STK22C48-SF45ITR	5V 2Kx 8 AutoStore nvSRAM SOP28-330	45 ns access time	Industrial

Package Diagrams

28-Lead, 300 mil SOIC Gull Wing



28-Lead, 330 mil SOIC Gull Wing



DIM = INCHES $\frac{\text{MIN}}{\text{MAX}}$

DIM = mm $\left(\frac{\text{MIN}}{\text{MAX}}\right)$

Document Revision History

Revision	Date	Summary
0.0	December 2002	Removed 20 nsec device.
0.1	September 2003	Added lead-free lead finish
0.2	March 2006	Obsolete: 35ns speed grade, Plastic DIP packages and Leaded Lead Finish
0.3	February 2007	Add Fast Power-Down Slew Rate Information Add Tape Reel Ordering Options Add Product Ordering Code Listing Add Package Drawings Reformat Entire Document
2.0	January 2008	In the block diagram and elsewhere in this data sheet, removed the "x" from V_{ccx}. Page 4: in SRAM Read Cycles #1 & #2 table, revised description for t_{ELQX} and t_{EHQZ} and changed Symbol #2 to t_{ELEH} for Read Cycle Time. Page 4: updated SRAM Read Cycle #2 timing diagram and changed title to add $\overline{G}$ controlled. Page 9: under $\overline{HSB}$ Operation, revised first paragraph to read "The $\overline{HSB}$ pin has a very resistive pullup..." Page 11: added best practices section. Page 13: added access times to Ordering Information table.